Leading zero blanking

This 'add on' circuit for any 3-digit electronic display that uses a 74C926 4-digit/decoder/driver IC, improves the appearance and efficiency of the 3-digit display by automatically blanking any leading zeros.

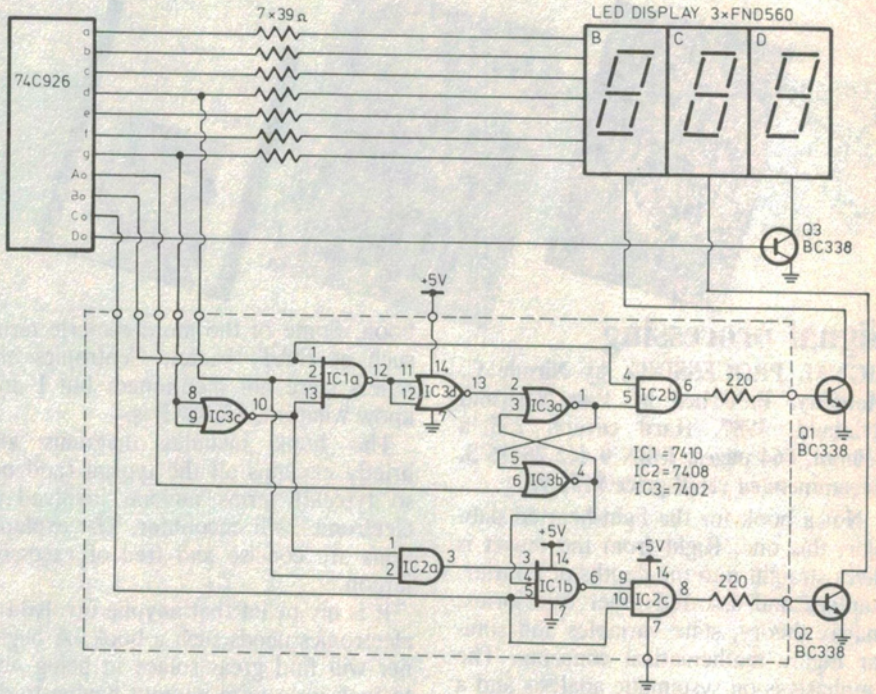
Because the 74C926 uses multiplexed outputs to drive the 7-segment displays, it is not so easy to blank out the leading zeros. The circuit within the dotted lines operates like this:

Display B needs to be blanked when Bo and the code for numeral zero is present at the a to g outputs of the 74C926. The simplest way to detect a zero character is to sense if segment d is on, and segment g is off.

Therefore, if Bo and d are a 1, and g is a logic 0, the output of IC3d will be a 1, setting the RS latch (IC3a and IC3b) so that pin 1 (output of IC3a) becomes low. As a result, the output of IC2b is driven low, turning off Q1 and blanking display B.

Display C is blanked when Co is high, segment d is on and segment g is off. However, pin 4 of IC3b (other output of the RS latch) must also be high, indicating that display B has been blanked. If all these conditions are true, pin 6 of ICIb goes low, driving pin 8 of IC2c low, turning off Q2 and blanking display C.

Note that Q1 is held off by the RS latch, which must be reset after all outputs Ao to Do of the 74C926 have cycled once. This is why Ao is connected to the Reset input of the RS latch.



This circuit was added to an already constructed digital speedo by building it on a 30 x 65mm PCB, and mounting it behind the speedo PCB, connected with ribbon cable.

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