Frequency Divider with 50% Duty Cycle

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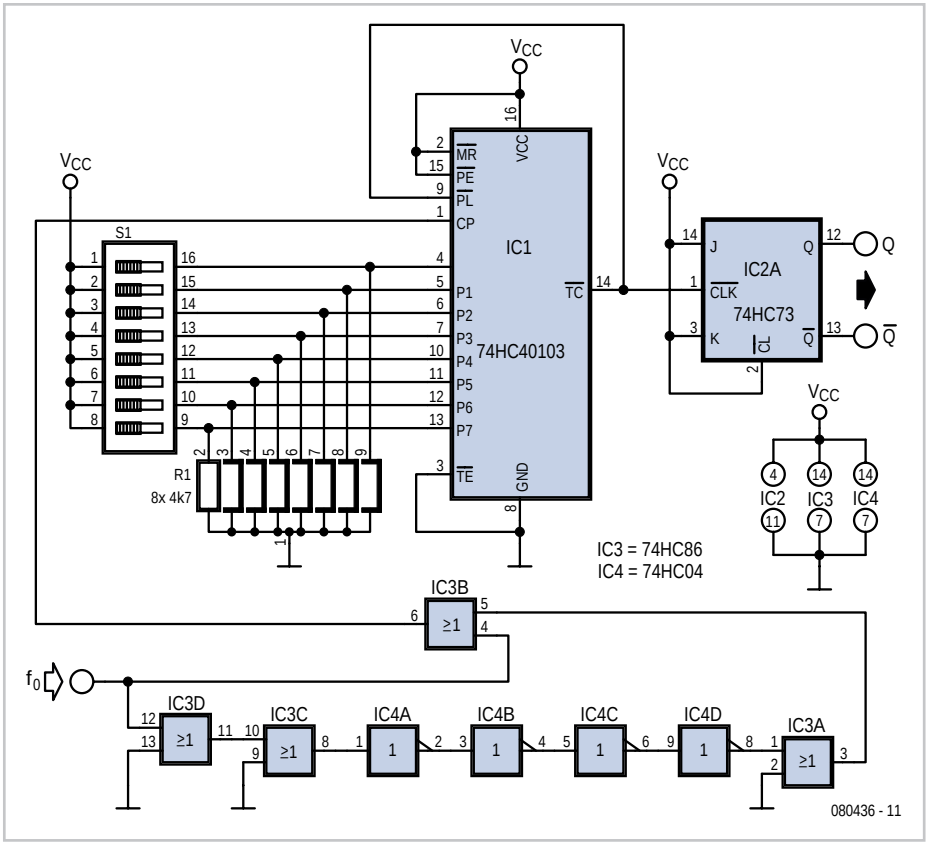
In digital circuit design, especially in microprocessor or measuring applications, it is often necessary to produce a clock signal by dividing down a master clock. The 4-chip solution suggested here is very versatile; it takes a 50% duty cycle input clock and outputs a 50% duty cycle clock selectable (via an 8-way DIP switch) for every divisor from 1 to 255.



The most complex chip in this design is IC1, an 8-bit down-counter which is 'programmed' by the binary value set up on the eight DIP switches. An edge detector circuit made up of IC3 and IC4 produces a pulse at every rising and falling edge of the input clock f_0. Each time the counter reaches zero a flip flop is toggled to produce a 50:50 mark/space ratio output signal.

It does not matter if the gates used in the edge detector circuit are inverting or non-inverting; the only important points are that the correct number of gates are used and the delay time produced by each gate. The total propagation delay through seven HC type gates will be enough to generate a pulse of sufficient width to reliably clock the counter. Propagation delay is the time taken for a signal at a gate's input pin to affect the output, and this is given in the data sheet. The edge detector produces a pulse on both the positive and negative edges of the input clock signal.

The down-counter decrements its value each time it receives a clock impulse on CP. Whenever the counter reaches zero the terminal count pin ($\overline{TC}$) generates a negative pulse, reloading the counter (via parallel load $\overline{PL}$) with the binary switch setting. The counter continues counting down from this value.

The JK flip flop IC3 is configured as a toggle type flip flop (both inputs J and K wired to a '1') the outputs Q and $\overline{Q}$ change state (toggle) on each rising edge of the $\overline{TC}$ output of IC1. The DIP switches are used to set up the division ratio, to divide the clock by 23 for example, set the DIP switches to the binary value of 23 i.e. 00010111 (setting P4, P2, P1 and P0 to high).

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