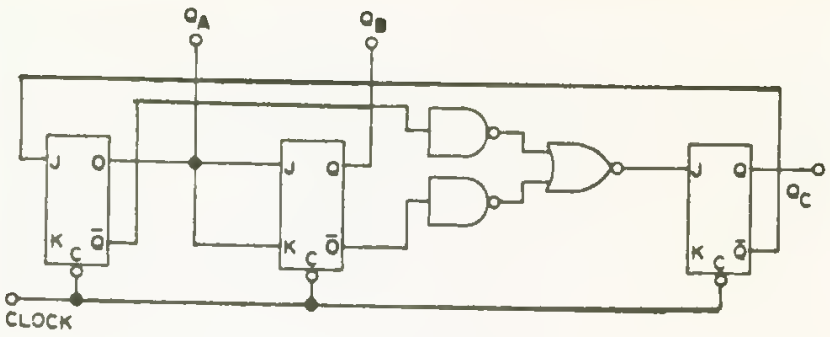
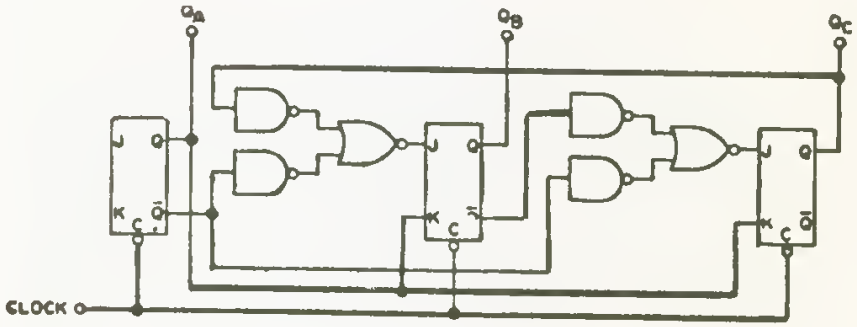


STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1

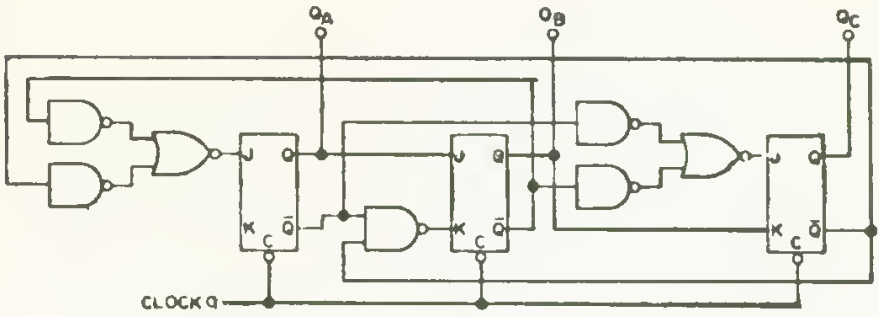
Fig. 31-9. Synchronous divide-by-5 up counter.



STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1

(1)C3050P
(1-1/2)C3073P

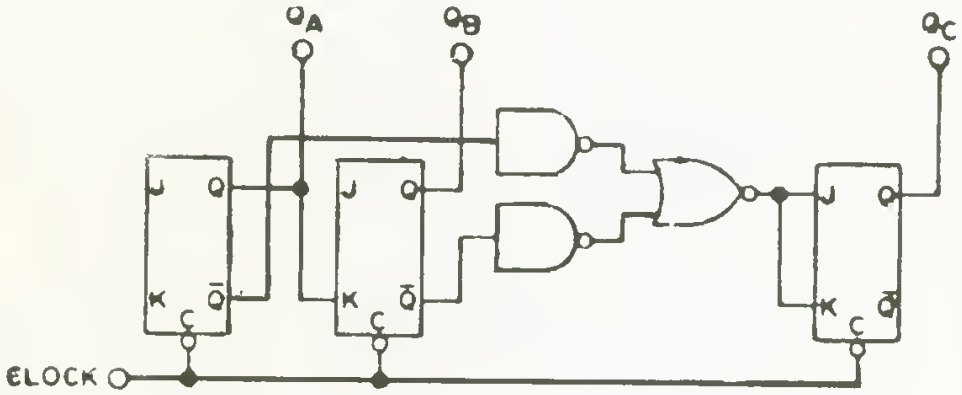
Fig. 31-10. Synchronous divide-by-6 up counter.



STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1

(1/4)C3000P
(1)C3050P
(1-1/2)C3073

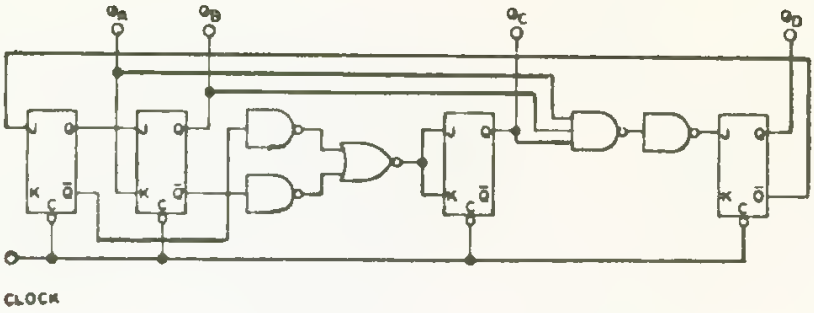
Fig. 31-11. Synchronous divide-by-7 up counter.



STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1

(1/2)C3050P
(1-1/2)C3073P

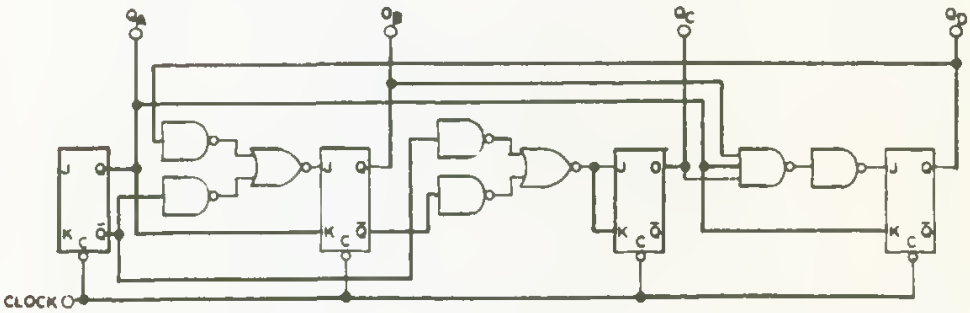
Fig. 31-12. Synchronous divide-by-8 up counter.



STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1

(1)C3020P
(1/2)C3050F
(2)C3073P

Fig. 31-13. Synchronous divide-by-9 up counter.



STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1

(1)C3020P
(1)C3050P
(2)C3073P

Fig. 31-14. Synchronous divide-by-10 up counter.