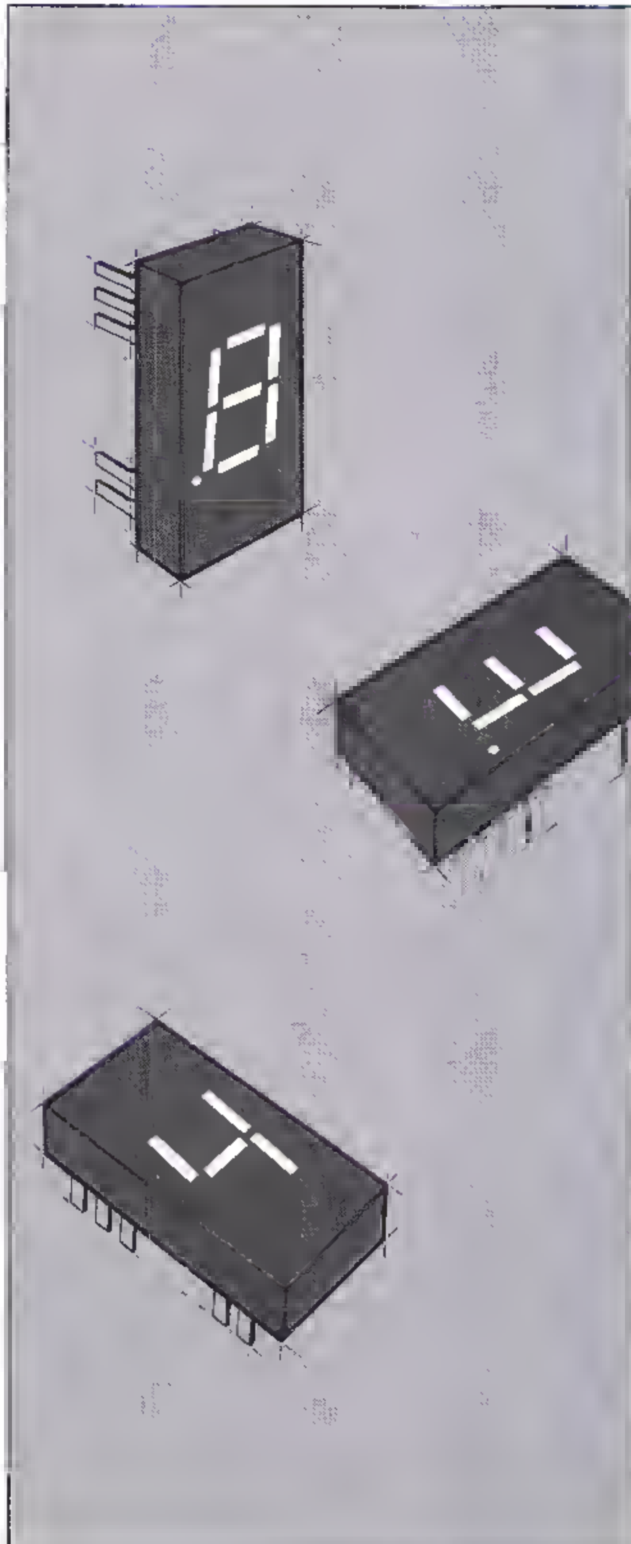


Application Note 941

5082–7700 Series Seven Segment LED Display Applications

5082–7700 Series
Seven Segment LED Display Applications

INTRODUCTION

The HP 5082-7700 series of LED displays are available in both common anode and common cathode configurations. The large 0.3" high character size generates a bright, continuously uniform seven segment display of both numeric and selected alphabetic information.

Designed for viewing distances of up to 10 feet, these single digit displays have been engineered to provide a high contrast ratio and a wide viewing angle.

The 7700 series utilizes a standard 0.3" dual-in-line package configuration that allows for easy mounting on PC boards or in standard IC sockets. Requiring a forward voltage of only 1.7 volts, the displays are inherently IC compatible, allowing for easy integration into electronic systems.

The 5082-7730 and the 5082-7731 are common anode displays employing a left hand or a right hand decimal point respectively. Typical applications would be found in electronic instrumentation, computer systems, and business machines. The 5082-7740 is the common cathode version featuring a right hand decimal point for applications that include electronic calculators and business terminals such as credit card verifiers.

This Application Note begins with DC drive techniques and circuits. Next is an explanation of the strobe drive technique and the resultant increase in device efficiency. This is followed by general strobing circuits and some typical applications such as clocks, calculators and counters.

Finally, information is presented on general operating conditions, including intensity uniformity, light output control as a function of ambient, contrast enhancement and device mounting.

DC DRIVE

In DC or non-strobed drive the display is operated with each character continuously illuminated, usually with one decoder per character. This technique is commonly used for short character strings where the cost of the decoders for DC drive is less than that for the timing and drive circuits for strobed operation. The LEDs are more efficient when strobed; however, in DC operation the drivers need not handle high current levels. The DC drive circuit for the common anode display is shown in Figure 1a. The current level, set here at 20mA per segment, is determined by the relation

$$R = \frac{V_{CC} - V_{LED} - V_{CE}}{I_{SEGMENT}}$$

where V_{CC} = voltage supply potential,
V_{LED} = forward voltage of LED at $I_{SEGMENT}$
V_{CE} = "ON" voltage of segment switch.

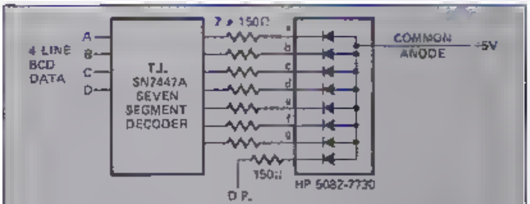


Figure 1a. Direct Drive Circuit for the 5082-7730/7731 Common Anode Display.

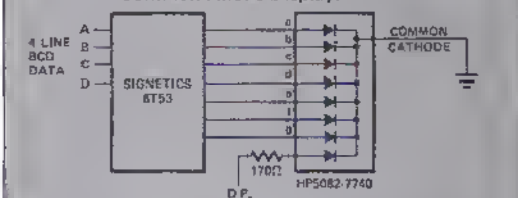


Figure 1b. Direct Drive Circuit for the 5082-7740 Common Cathode Display.

An analogous circuit is shown in Figure 1b for a common cathode DC drive system utilizing a current sourcing decoder/driver instead of a standard decoder/driver and external resistors.

See Table I for a list and comparative ratings of some of the commercially available seven segment decoder/driver circuits.

STROBING DRIVE CIRCUITS

In strobing, the decoder is timeshared among the digits in the display, which are illuminated one at a time. The digits are electrically connected with like segments wired in parallel. This forms an 8 (7 segments and decimal point) x N (number of digits) array. In operation, the appropriate segment enable lines are activated for the particular character to be displayed. At the same time a digit enable line is selected so that the character appears at the proper digit location. The strobe then progresses to the next digit position, activating the proper segments and digit enable line for that position.

Since the eye is a relatively slow sensor, a viewer will perceive as continuous a repetitive visual phenomena which occurs at a rate in excess of about 60 events per second. Therefore, if the refresh rate for each digit is maintained at 100 times or more per second, the perceived display will appear flicker-free and easy to read. In displays subject to vibration, a minimum strobe rate of 5 times the vibration frequency should be maintained.

In addition to reducing the number of decoders and drivers, strobing requires less power than DC drive to achieve the same display intensity. This is due to a basic property of GaAsP where luminous efficiency (light output/unit current) increases with the peak current level (see Figure 2a). Thus, for the same average current, use of lower duty cycles (and higher peak current levels) results in increased light output (see Figure 2b). For example, from Figure 2b, a typical device operated at 10mA DC would produce a luminous intensity of approximately 120 microcandelas. The same device operated at 50mA peak, 20% duty cycle (as if in a 5 digit strobed display) will produce approximately 145 mcd time averaged luminous intensity.

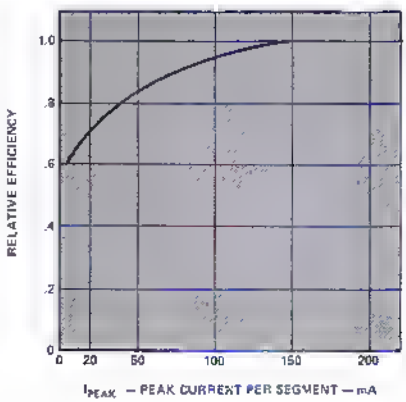


Figure 2a. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

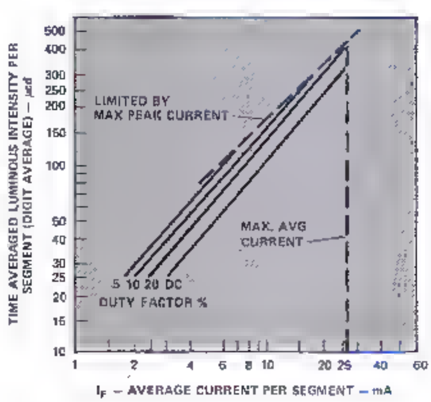


Figure 2b. Typical Time Averaged Luminous Intensity per Segment versus Average Current.

For common decoder/driver circuits, a series resistor is placed in each segment enable line to limit the light emitting diode current. They are placed in the segment enable lines to prevent uneven current distribution among segments, commonly referred to as "current hogging". The resistive current limiting approach for LEDs outlined above is compact and easy to implement. However, the resistor consumes power.

Various techniques for driving LED displays from energy storage devices (such as inductors or capacitors) are quite practical though generally somewhat higher in cost and bulkier. However, power savings of as much as 50% over the resistive drive techniques are attainable. SCR switches may be attractive in circuits utilizing energy storage devices.

Figures 3 and 4 illustrate two possible memory buffer and display drive techniques used in strobed applications. Both memory techniques assume a bit-parallel/character-serial data entry format. If the system memory is available to supply data to the decoder, the buffer portion of these circuits may be deleted.

Figure 3 depicts a 5-digit strobed display employing a recirculating shift register memory. One shift register is used for each bit of the 4-bit BCD code. Four lines of data from the shift registers drive an SN7447A seven-segment decoder. The value of the current limiting resistors is calculated to provide 40mA per segment peak drive current. The resistor value may be calculated using the following formula:

$$R = \frac{V_{CC} - V_{LED} - V_{CE1} - V_{CE2}}{N\ I_{AVE}}$$

where V_{CC} = voltage supply potential,
V_{LED} = forward voltage of LED at peak $I_{SEGMENT}$ ($N\ I_{AVE}$), V_{CE1} = "ON" voltage of segment switch at peak $I_{SEGMENT}$,
V_{CE2} = "ON" voltage of digit switch at 8 times peak $I_{SEGMENT}$, I_{AVE} = desired average operating current per segment, and N = number of digits in the display.

Data for each digit of the display is sequentially shifted to the OE output of the shift register by the display scan clock. The scan clock also drives an SN7496 shift register set up as a ripple scanner. The scan shift register outputs are buffered to source the 320mA peak digit current. Data entry to the storage registers is controlled by the system clock of the data source. During data entry, the display is blanked and the scan shift register is reset to the

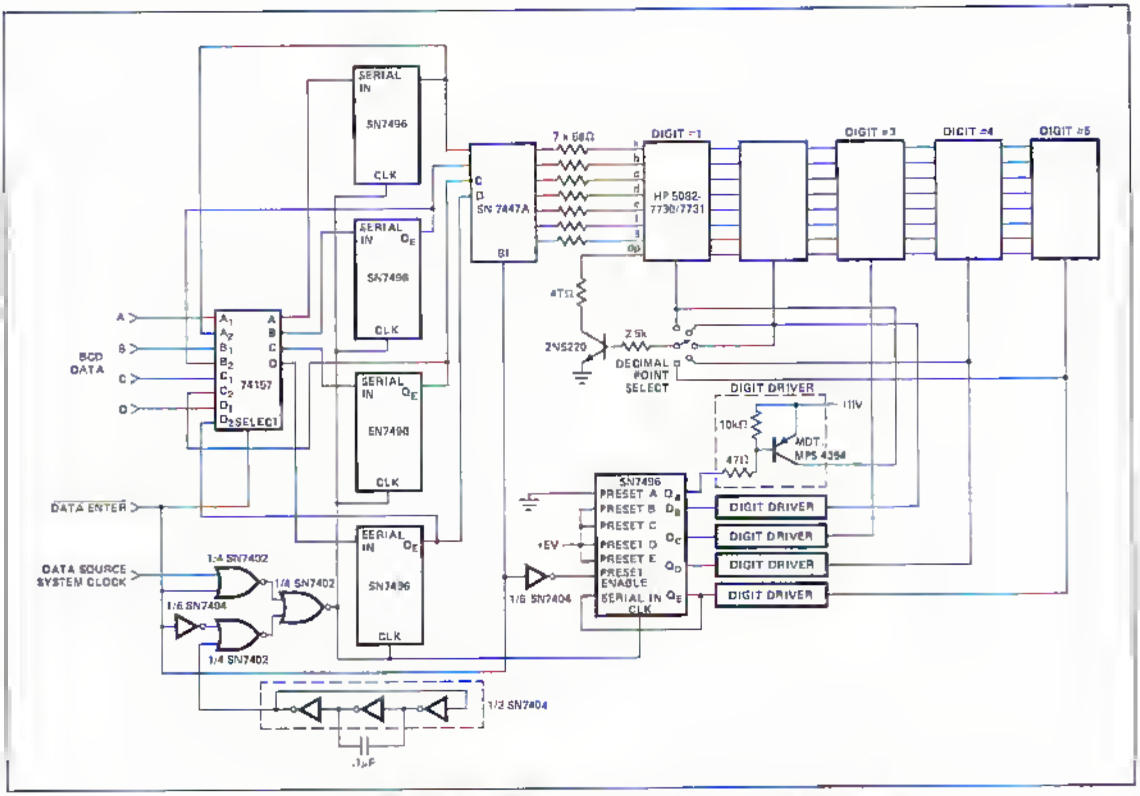


Figure 3. Five Digit Strobed Display with Recirculating Shift Register Memory.

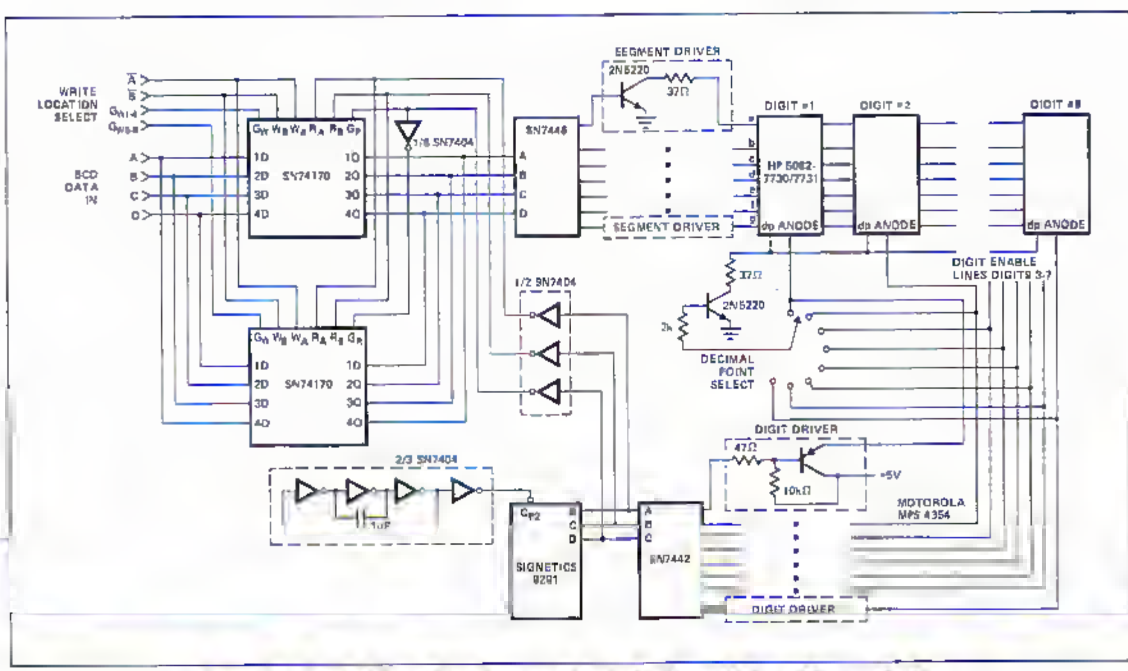


Figure 4. Strobed Eight Digit Common Anode Display with Static Memory Buffer.

first digit position by a logic "0" at $\overline{\text{DATA ENTER}}$. The DATA SOURCE SYSTEM CLOCK and the external BCD lines are also enabled by $\overline{\text{DATA ENTER}}$. The 5 digits of new data will be entered into the shift registers on each positive transition of the system clock. After data entry, $\overline{\text{DATA ENTER}}$ is returned to a high state, and scanning begins at position "A" under control of the SCAN CLOCK.

Figure 4 depicts an eight digit strobed display employing a static 4 x 8 bit memory. Data from the memory buffer is selected by the read lines under the control of the scan counter. This data is decoded by an SN7448 to drive the display segment lines. In this case the 80mA per segment peak current is beyond the current sinking capability of any common decoder/driver so an output buffer transistor must be used. Current limiting resistor values are calculated as before. The digit scan counter uses a Signetics 8281 binary counter in the divide by 8 mode. Data entry to the memory buffer can occur simultaneously with data read and any one of the eight digits may be selected or written independently.

The display length illustrated in either of the above schemes may be changed by simply providing the additional memory requirements and extending the capacity of the digit scanner. Displays of up to 16 digits are practical.

Numerous manufacturers are now supplying transistor arrays and buffer drivers which offer the advantages of lower costs and improved packing densities over discrete segment and digit drivers. See Table II for a list of some of the presently available products. See Table III for other useful display circuits.

CALCULATORS

The display circuit for a 10-digit calculator is given in Figure 5. A MOSTEK MK5010P single chip calculator circuit provides the calculating, decoding, and timing for a four function (+, –, x, ÷), 10-digit calculator. The displays are strobed at 100mA peak on a 1 of 10 duty cycle. The Darlington segment drivers source 100mA while the digit drivers sink 800mA peak. The MOS output transistor connecting the output to V_{SS} is "OFF" when the segment (or digit) is to be activated. In this state, the pull-down resistor connected to V_{GG} sinks the current necessary to turn on the PNP drive stage. When the MOS transistor is "ON", the 1mA output current through the pull-down resistor biases the PNP drive stage "OFF".

There are a variety of calculator chips for 8, 10, and 12-digit applications with varying voltage supply requirements and features. These include circuits from companies such as AMI, Cal-Tex, MOSTEK, NORTEC, Rockwell Int'l., and TI. Output stages vary although the P-channel, open-drain approach used in the MK5010P example is the most common.

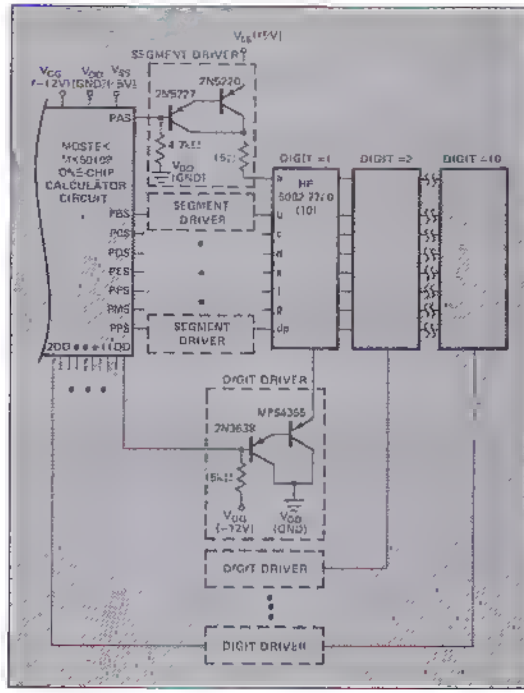


Figure 5. Typical Single Chip Calculator Circuit

CLOCKS

Figures 6 and 7 depict the complete circuitry for 6-character digital clocks using monolithic clock chips from two different manufacturers. Both clocks use the 60Hz AC line as a time base and derive power from unregulated bridge rectifier power supplies.

Figure 6 illustrates a 6-digit clock circuit using the National Semiconductor NM5314 clock chip. This chip uses a strobed technique with all scanning logic and memory buffers on board. Scan frequency is established by an external RC network and should be maintained between 60Hz and 10kHz. The values shown should generate approximately a 1kHz scan rate. Each of the P-channel MOS outputs is buffered to provide adequate drive current to the individual segment and digit enable lines.

Figure 7 illustrates a 6 digit clock radio circuit using the MOSTEK MK5010PAN clock chip and HP 5082-7740 common cathode displays. Since the MK5010P series chips provide a 12.85% duty cycle digit enable, the component values shown will supply approximately 10mA average or 77mA peak current to each segment of the strobed display. The base inputs of the MPSA-13 segment drivers and the MPSU 45 digit drivers each have series current limiting resistors and pull-down resistors to limit maximum drain current and assure cut-off in the "OFF" state. In this circuit, the digit drive lines are multiplexed to accept input data for alarm set, time set, and other functions.

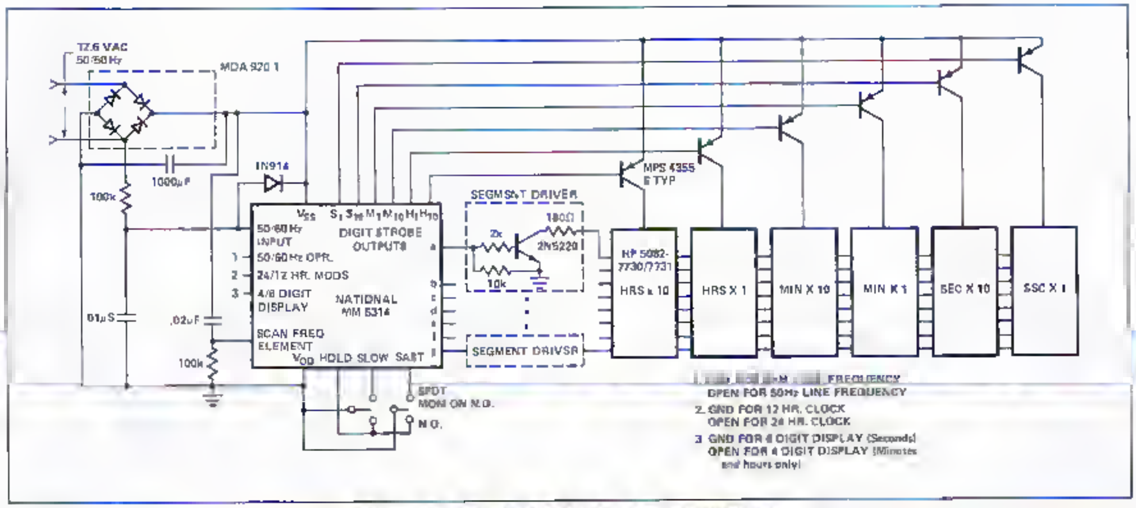


Figure 6. Strobed Drive for a Six Digit Clock.

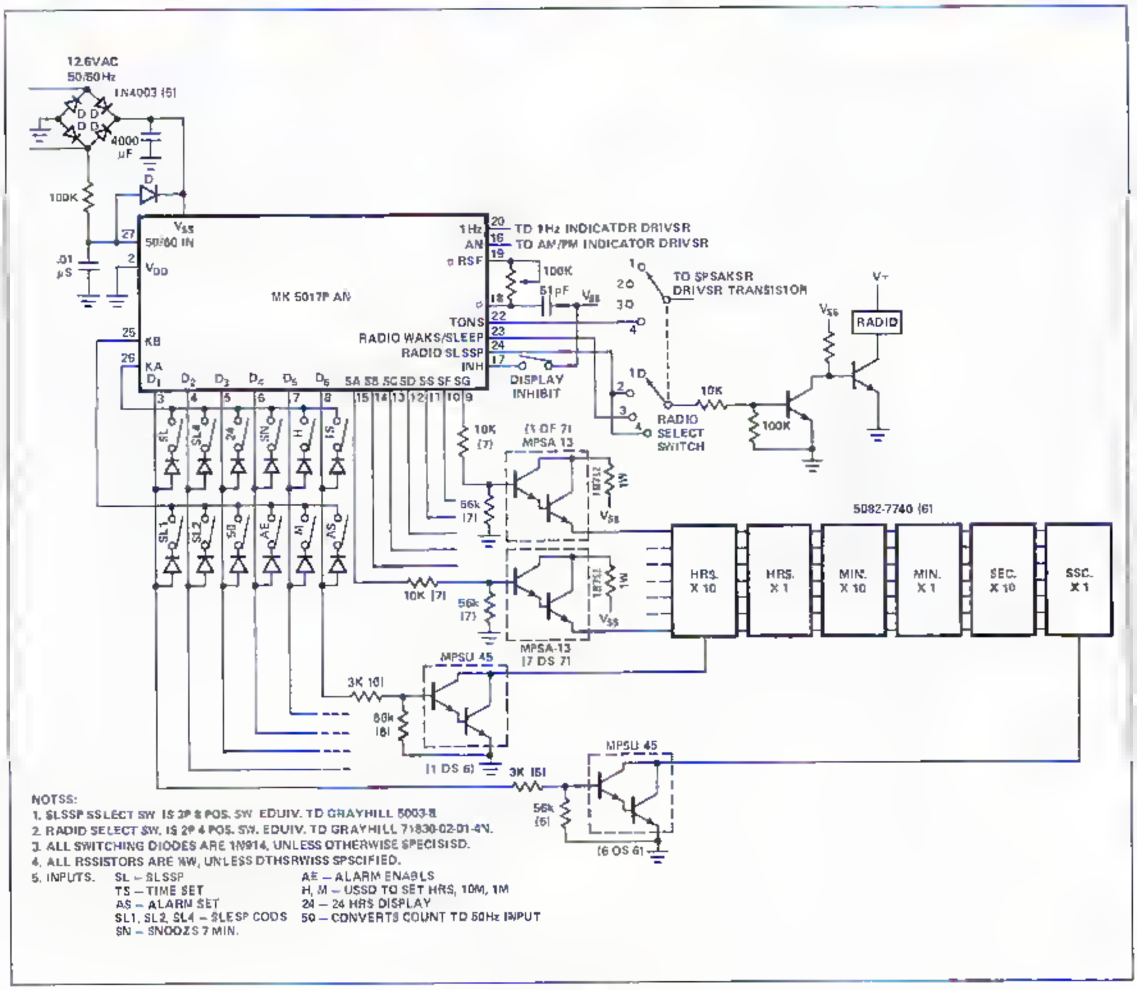


Figure 7. Six Digit Clock Radio.

APPLICATION

COUNTERS

The strobe display circuit for a 4½ digit counter is shown in Figure 8 utilizing the 7730 common anode display (left hand decimal point) and the MOSTEK MK5007P four decade counter. Available in a 16-pin package, this circuit is a less expensive version of the familiar MK5002P, and includes latches, decoding and multiplexing functions. In addition to counting, this circuit can be used with its internal clock for DVM, timer and other measuring applications. In this example, the MK5007P's BCD outputs are converted to a seven segment format by the SN7447A decoder/driver which can sink 40 mA per segment. A flip-flop is used to implement an overflow digit "1", providing a 4½ digit display. The average light level of the display is controlled by two factors. First, R controls the peak current per segment, set here for 40 mA. The second factor is the duty cycle of the counter's SCAN INPUT signal. The internal multiplexing circuit for scanning the digits is triggered on the falling edge of the scan clock. While this signal is low, the segment and digit outputs are blanked.

Therefore, a duty cycle greater than 80% of the SCAN INPUT signal is desirable for efficient operation. In this circuit, use has been made of the MK5007P's internal scan clock; a timing capacitor at the SCAN INPUT sets the frequency. The MOSTEK units can be cascaded for greater than 4 decades of readout. Similar circuits in function are General Instrument's AY-5-4007 series, which have the additional feature of a 25 mA sourcing capability at each segment output line.

A DC drive circuit for a 5 digit counter is outlined in Figure 9. This combines the -7730 common anode display (left hand decimal point) with the TI SN74143, a 4-bit counter/latch/decoder having 15 mA constant current outputs. For applications requiring counting up to 12 MHz, the use of this circuit greatly reduces the component count (even the current limiting resistors are eliminated). The LATCH STROBE INPUT allows the display to operate in a data sampling mode while the counter continues to function. The BLANKING INPUT allows total suppression or intensity modulation of the display. The stored BCD data is available for driving other logic via the LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D). For higher current drives, the SN74144 with its open-collector outputs can sink 25 mA per segment.

INTENSITY UNIFORMITY

The 5082-7700 series devices are categorized for light output intensity to minimize the variation between digits or segments within a digit. Luminous intensity categories are designated by a letter located on the right hand side of the package. Display appearance will be optimized when a group of display digits uses devices from a single category.

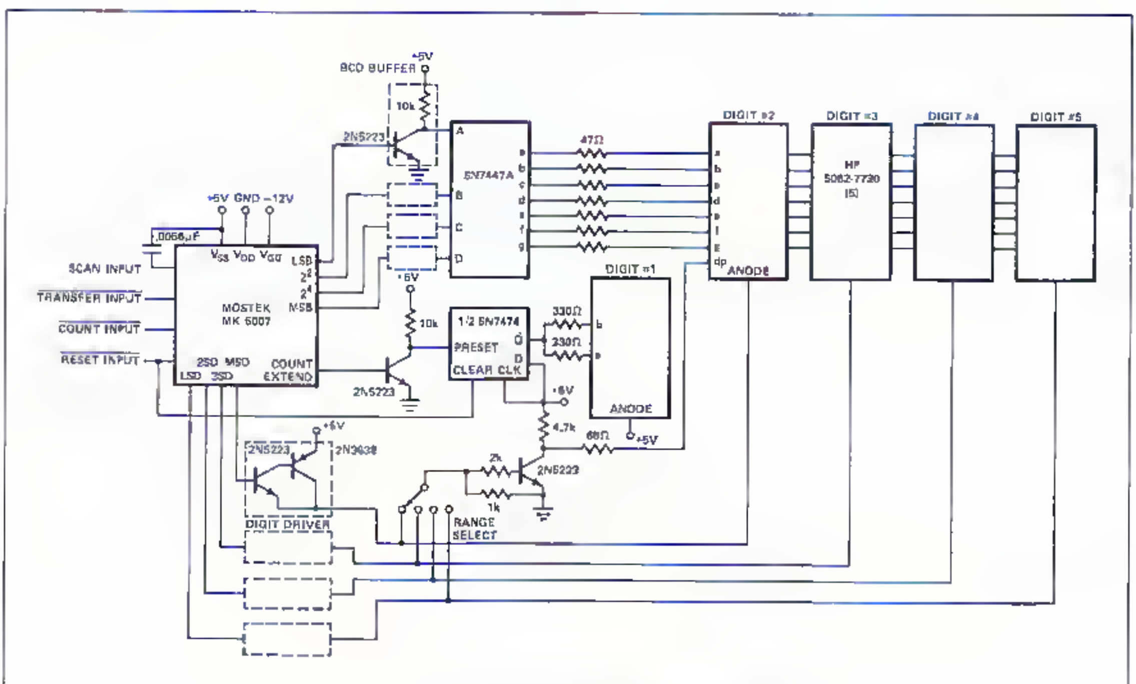
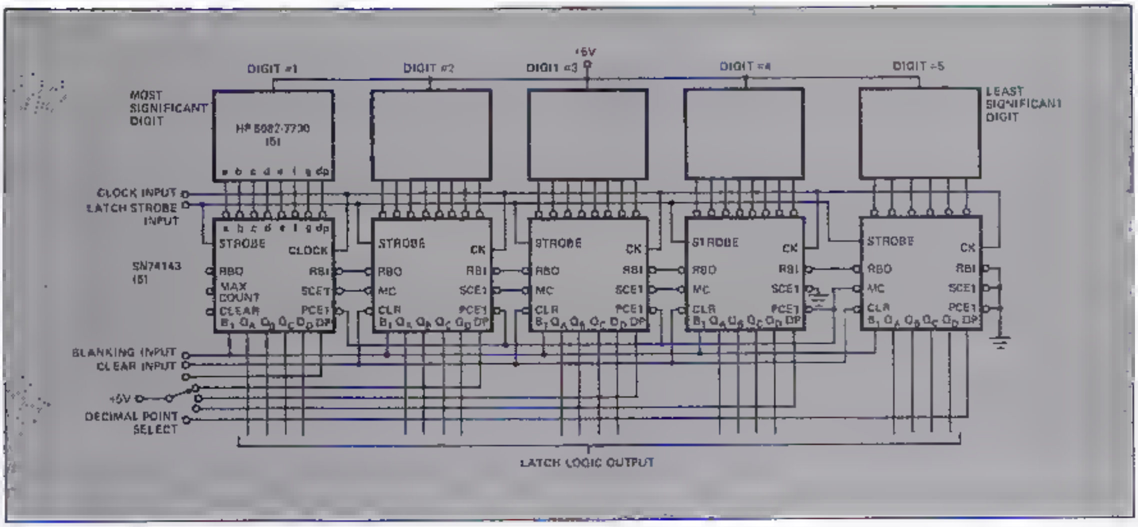


Figure 8. Four and One-half Digit Strobed Counter



INTENSITY MODULATION

It is often desirable to vary the intensity of a display to provide improved readability under varying ambient lighting conditions. Intensity control can be achieved using either amplitude or pulse width modulation techniques. The latter is recommended for broad dynamic range of intensity control. Pulse width modulation offers the advantage of good tracking between segments as the intensity is decreased, and also allows the LEDs to operate with a high peak current where they are more efficient. Figures 10 and 11 illustrate two possible techniques of control.

In Figure 10 a monostable multivibrator is triggered by the scan clock. Photo-resistor R_1 tracks with ambient light intensity and causes the monostable multivibrator to produce an output pulse width proportional to ambient lighting. This method will provide duty cycles ranging from approximately 20% to 100%.

Figure 11 depicts another intensity modulation technique. The scan clock input square wave is integrated by R_1 and C_1 to form a triangular wave. Ambient light is monitored by a phototransistor and an amplified output voltage proportional to ambient lighting is produced by A_1. These two signals are presented to the comparator A_2. The output of A_2 will be true only as long as the triangle wave voltage is greater than the ambient light signal. The LM311 amplifier used in this circuit can be replaced with any medium to high gain amplifier which will give adequate swing with a single 5 volt supply. This technique offers a 0 to 100% dynamic range of modulation.

In both of the above examples, the pulse width modulated signal is connected to the blanking input

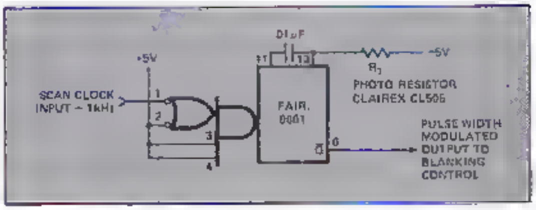


Figure 10. Multivibrator Modulation Circuit.

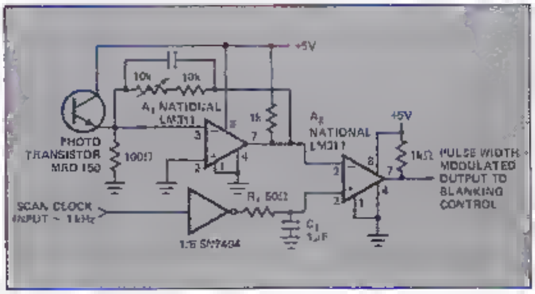


Figure 11. Wide Dynamic Range Intensity Control Circuit.

of the display driver. The display duty cycle is then controlled by the modulated signal which is proportional to the ambient intensity. If the scan frequency is substantially greater or less than 1 kHz in either of the above circuits, timing and integrating component values will have to be changed to produce satisfactory results.

CONTRAST ENHANCEMENT

The quality of the perceived display is a function not only of light intensity but also of contrast to the background. To improve display contrast, the entire front surface of the display, except for the light emitting areas, is finished in a uniform flat black. The plastic encapsulant in the light emitting areas contains a red dye to further reduce the reflected ambient light. The display's background and the type of contrast enhancing filter used affect the display quality. Typically, PC board mounting and an inexpensive red filter (e.g., Plexiglass 2423 or materials having similar transmission characteristics) are used. Under strobe drive conditions of 10 mA/segment average, the display is easily readable to distances of ten feet and will retain good contrast under relatively high ambient lighting conditions.

There are several additional contrast enhancing measures that can be implemented to allow lower display intensity and power levels. With respect to PC board design, keep as many metallized lines as possible out of the normal viewing area. These surfaces reduce contrast by reflecting ambient light. Whenever possible, the lines running to the displays should be placed out of sight on the board's back side. You can also hide metal traces by placing them beneath the display package. To minimize the light reflected from the PC board, the area surrounding the display can be darkened either through use of a screened black epoxy ink (e.g., WORNOW W-O-N black ink) or a black piece of material cut as a collar to fit around the display. Circular polarizing filters (such as Polaroid HRCP-red) or 3M Display Film are particularly effective in enhancing contrast in high ambient light although they may be more expensive. Antiglare coatings are available from firms such as Panelgraphic Corp. to reduce front filter reflections. An antiglare surface finish may also be incorporated into the molds used to manufacture the filters.

MOUNTING CONSIDERATIONS

The 5082-7700 series devices are constructed utilizing a lead frame in a standard DIP package. In addition to easy PC board mounting, the standard pin spacing of 0.100" between pins and 0.300" between pin rows allows use of the familiar 14-pin IC sockets. See Table IV for a list of some of the available display sockets. The displays may be end-stacked as close as 0.400" center-to-center. The lead frame has an integral seating plane which holds the package approximately 0.035" above the PC board during standard soldering and flux removal operations. The devices can be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). To optimize device performance, materials are used that are limited to certain solvents for flux removal. It is recommended that only Freon TE, Freon TE-35, Freon TF, Isopropanol, or soap and water be used for cleaning operations.

Note: See following pages for Tables I, II, III and IV.

Table I. Decoder/Driver Circuits for Seven Segment Displays

Manufacturer's Product No.	Manufacturer	Common Anode or Common Cathode	Rated Maximum Output Current [mA]	Other Features	Other Manufacturers
7447	Texas Instr.	CA	40		National Semi, Fairchild, Motorola, Signetics
7448	Texas Instr.	CC	4*		National Semi, Fairchild, Motorola, Signetics
9307	Fairchild	CC	5.6*		
9317 B/C	Fairchild	CA	40/20		
9357	Fairchild	CA	40		
9368	Fairchild	CC	19***	Quad Latch	
9369	Fairchild	CC	50		
9370	Fairchild	CA	25	Quad Latch	
9660	Fairchild	CC	5-50**	Pgmbl Current and Decimal Pt. Drive	
MC 14511	Motorola	CC	25	CMOS	
MC 4039	Motorola	CA	20		
N8T51 B N8T59 B	Signetics	CA, CC		MOS Compatible Inputs	
N8T74 B N8T75 B	Signetics	CA, CC		Quad latch MOS Compatible Inputs	
8140	Harris	CA	40	Quad latch	
1001/1002	SCS Microsystems		120*	Quad latch, some versions available w/resistors on board	

*with external pull-up resistance **constant current supply ***current limit resistors on board

Table II. Driver Arrays for LED Displays

Manufacturer and Product No.	Maximum Output Current	Drivers Per Package	Typical Application
ITT Semiconductor			
502	200mA Sink	6	Digit Drive
503	34mA Source	4	Segment Drive
National Semiconductor			
DM8861	50mA Source or Sink	5	Segment Drive
DM8863	500mA Sink	8	Digit Drive
Sprague Electronics			
ULN 2031A	80mA Sink	7	Segment Drive
ULN 2032A	80mA Source	7	Segment Drive
Series 400	250mA Sink	4	Digit Drive
Texas Instruments			
SN75491*	50mA Source or Sink	4	Segment Drive
SN75492*	250mA Sink	6	Digit Drive

APPLICATION

Table III. Circuits for Seven Segment Displays

Manufacturer and Product No.	Description	Comments
Texas Instruments		
SN74143	BCD Counter/4 Bit Latch/BCD-7 Segment Decoder/15mA Constant Current Driver	Ideal for Counting Applications (Time or frequency measurements, A-D Converters).
SN74145	BCD to Decimal Decoder (1 of 10 Decoder)/Driver	Capable of sinking 80mA per line making it ideal for a digit scanner.
SN74144	Same as SN74143 except output driver can sink up to 25mA per line	Need current limiting resistor for each segment.
SN74142	BCD Counter/4 Bit Latch/BCD to Decimal Decoder (1 of 10 Decoder) Driver	Useful for digit scanner. Need only a clock signal since counter is in circuit.
National 8551 TI SN74173 Signetics 8T10	Tri-State Quad Latches (Also known as "Bus Buffers")	Allows bussing of data lines eliminating numerous gates.
Mostek		
MK5002, 5007, 5005	4 Decade Counter/BCD-7 Segment Decoder/4 Digit Scanner in 1 package, 3 options	Provides all counting and timing signals for a 4 Decade Strobed Counter Display (can be end stacked for 8 decades, ...)
GI		
AY-5-4007 Series	4 Decade Counter/BCD-7 Segment Decoder/4 Digit Scanner/LED Driver	Similar in function to Mostek 5002 series but adds 25mA LED drivers for strobed display.

Table IV. 14 Pin DIP Sockets for 7700 Series Displays

Manufacturer and Product No.	Termination	Description
Amphenol-Barnes		
821-20011-144	Solder	Nylon, Low Profile
821-20013-144	Wire Wrap	Nylon, Low Profile
821-25011-144	Solder	Full Sized Body
821-25012-144	Wire Wrap	Full Sized Body
Augut		
314-AG50-2R	Solder	Full Sized, Phenolic
Clinch		
14-W-DIP	Wire Wrap	Low Profile, Nylon
14-DIP	Socket	Phenolic
Cambion		
3777-01-0312	Solder	Nylon
3897-01-0316	Wire Wrap	DAP Plastic