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# Maximizing EOS and ESD immunity in high-performance serial buses

PROTECTING PRODUCTS FROM ELECTROSTATIC HAZARDS MAY SEEM TO INVOLVE BLACK MAGIC, BUT IT DOESN'T. A LAYERED STRATEGY OF DEFENDING AGAINST THE HAZARDS MAXIMIZES PRODUCTS' IMMUNITY AND MINIMIZES THE IMPACT ON PART COSTS AND PROJECT SCHEDULES.

EOS (electrical overstress) and ESD (electrostatic discharge) are the main causes of failures in semiconductors. Although EOS often takes the blame, ESD may sometimes accompany EOS. Did the assembly machinery zap the part? Did the handling procedures take the proper ESD precautions? Did the test equipment do something to the part? Or did the end user zap the part while crawling on a rug to reach a connector in back of a computer so he could plug in a cable? Figuring out the cause of device failures can present significant challenges. Eliminating the detective work by avoiding the failures is the most cost-effective approach. This article shows how to make pc boards as tolerant as possible of ESD and EOS.

ESD is a high-voltage external event that can get into your product and destroy the silicon. Typically, the discharges are common-mode-type events, which can result from many things, including insulation failures that you can detect only by careful scanning with an electronic microscope, sneak paths through internal protection diodes, and short circuits that enable conduction from a power rail to melt holes in the device. Because of their multiple causes, EOS problems don't yield to a single mitigation approach. EOS prevention is much like the defend-in-depth philosophy of medieval-castle builders: First, keep the ESD energy from getting in. (Keep the enemy out!) Second, dissipate the energy that does get in. (Make life hard for an enemy who gets through the first gate.) Third, make the silicon as resistant as possible to energy that does get in. (Put armor on your soldiers.)

The following recommendations are for high-speed serial buses, such as FireWire, USB, and, with extra care, PCIe (Peripheral Component Interconnect Express). Note that any hole in the chassis serves as an entry point for ESD. A high-speed serial bus may not be the problem. In fact, it may be the solution. By combining many outside connections, a single serial-bus connection can eliminate entry points for ESD (making it necessary to defend only one gate to the castle).

## KEEP THE ENEMY OUT!

First, if possible, do not let ESD energy get to the silicon. The best way to accomplish this objective is with a Faraday cage. Ideally, a continuous conducting surface—typically, chassis ground—completely surrounds the internal electronics and connects to the green wire or earth ground. A good example of this approach is a PC's metal-tower case, a conducting enclosure that surrounds all the internal electronics. However, the high-speed serial bus requires a hole in that continuous surface to mount the connector to allow the electrical signals to enter. Well-designed serial buses have an overall external shield around the signal conductors and a metal shield on the pc-board connector. If a low-impedance connection connects the overall shield to the pc-board-connector shield and if a

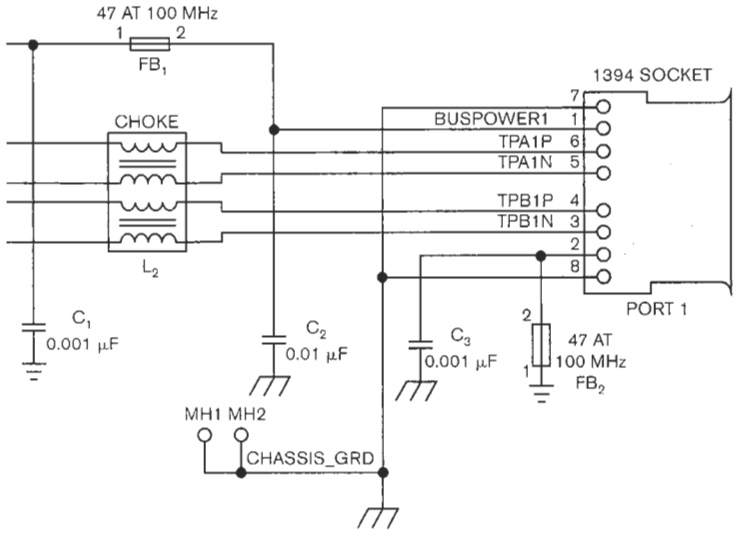


Figure 1 Carefully selected and located ferrite beads and capacitors as well as careful connector mounting maximize the immunity of the IEEE 1394 FireWire bus to electrostatic damage.

$FB_1$, in series with the power connection. The ferrite presents a resistance to signals at high frequencies. At these higher frequencies, the bead exhibits higher impedance than that of the capacitor. The high-frequency edges are ESD's most damaging components. This combination of capacitor and ferrite aids in eliminating these edges.

With a small addition, this circuit becomes an effective EMI filter. The EMI filter is the converse of the ESD filter. The ESD filter tries to keep energy out, and the EMI filter tries to keep energy in. For EMI, the capacitor, $C_3$, next to the ferrite bead connects to the same ground as the transceiver, not to chassis ground. The idea is to return energy to its source, the transceiver chip. On the schematic, this arrangement now looks like a classic pi filter with the capacitors forming the legs and the ferrite at the top. Pay attention to the layout; it is important. To keep ESD out, the ESD capacitor should be as close as possible to the source of the ESD, the connector. But the EMI capacitor should be as close as possible to the source of the EMI, the transceiver chip. You should place the ferrite closer to whichever is the bigger problem. Place the bead close to the connector if ESD is the larger concern or close to the transceiver if EMI from the transceiver is more serious. If you lack enough information to decide, place the ferrite close to the connector. There, it will still keep EMI from the various sources from escaping the system and will do the most to prevent damage from ESD.

## TRICKY GROUND CONNECTION

The ground connection is much trickier. Both FireWire and USB use common-mode signaling that requires a low-impedance return path—that is, the ground-return path through the cable's ground wire. For this reason, don't place a ferrite bead in series with the ground wire unless you have no other way to meet the ESD/EMI requirements. If you must use a bead, you should test it extensively to ensure that it works. However, you can aid ESD suppression by connecting a capacitor from signal ground to chassis ground as close as possible to the connector. This capacitor produces a current divider, and most of the current passes through the signal-to-ground connection. Some goes through the capacitor to chassis ground, however—with luck, enough to make a difference.

Trickiest are the high-speed signal lines, which you must treat equally. Anything you do to one of the lines you should do to both lines of the differential pair. The best approach is usually a common-mode choke for the technology you are using. The common-mode choke presents a high impedance to signals common to both conductors and lets differential signals pass. This approach works well for both ESD and EMI because both are typically common-mode phenomena. Again, component placement involves trade-offs. Placing the choke near the connector has the greatest effect on ESD. A position near the transceiver does the most to mitigate transceiver EMI. For the same reasons as those for ferrites, place the choke near the connector unless transceiver EMI is the dominant reason for adding the choke. For FireWire with two differential pairs, a single device with a common core uses less pc-board area. However, using a separate choke for each pair reduces crosstalk between the two pairs, which is often a good reason to use separate chokes despite the pc-board-area penalty.

You should take several issues into account and exercise caution concerning them. First, do not put capacitors on the high-speed, twisted-pair signal lines. In all cases, the frequencies present will cause any capacitance greater than a few picofarads to present signal-integrity problems. Although the product under test might at first seem to work, the bit-error rate can be high. Also, do not use common-mode chokes except those explicitly designed for the technology you are using. FireWire Version A (IEEE 1394a) uses a common-mode-signaling mechanism to determine the speed at which it can transfer packets. If a common-mode choke on the signal lines does not pass this common-mode signal, the higher speed packets will fail, even though the 98.304-Mbps packets work.

You also should avoid using a two-sided board. At the frequencies at which these serial buses operate, the loop impedance, which includes the outgoing-signal path plus ground-return path, determines the signal integrity and the amount of radiated EMI. Having a solid ground plane underneath traces and not using vias on these traces greatly

eases the layout job. Introducing vias hurts signal integrity, and you must then worry about connecting image planes to minimize the signal-path loop area; the layout quickly becomes excessively complex. Use a four-layer board with a solid ground plane underneath the twisted-pair signal lines from transceiver to connector pins. Use a solid flood for a chassis-ground plane that connects to the connector shell and provides a connection point for the components that connect to chassis ground. When laying out such a board, give higher priority to placing a solid signal-ground plane under the complete length of the signal lines than to achieving a simple shape for the chassis-ground flood.

## ARMOR YOUR SOLDIERS

If ESD gets past the dissipation defenses, the situation is as if enemy soldiers have gotten into the keep; now you must fight. You must protect the devices from any energy that gets beyond the defenses you have set up. All silicon devices have built-in ESD protection of some sort; check the data sheet. But, almost always, you can do more on the pc board. Your goal is to keep anything from upsetting the silicon's function. The first things to check are any reset pins. You must protect them from accidentally changing state. If the reset pin's threshold is referenced to ground, as most are, place a capacitor from the reset pin to ground. The capacitor helps to keep the reset pin from changing state during a ground-bounce event. In this case, an event changes the level of the ground reference; if it changes too much, the silicon can execute a reset. During brief ground bounces, a capacitor from the reset pin to ground helps to hold constant the nominal voltage between the pin and ground. During longer events, the capacitor's charge drains off, allowing the voltage to change, maybe to the point of exceeding the threshold. For this reason, make the value of this capacitor as large as possible. If the reset pin is almost a dc signal, put a greater-than-1-μF capacitor on it. Use a lower value capacitor if it places too much of a load on the driving signal or too greatly limits the frequency, but, in this case, bigger is nearly always better. This same reasoning applies to all of the inputs that could be disruptive to the silicon. In the case of FireWire physical layers, take special care with the reset and LPS (link-power-status) pins.

For other pins that could encounter an ESD strike, every little bit of resistance that you can add between the silicon and the ESD strike helps to protect the silicon. For example, placing a 10Ω resistor in series with a signal as close as possible to the silicon without seriously affecting it increases the device's ESD tolerance. Adding these elements is like equipping your soldiers with armor. Knights in armor or chain mail are more formidable for combat than those in fabric clothing.

## HOW MUCH DEFENSE?

Are all of these measures necessary? It depends. If you are building only a few boards, by all means spend the extra money and time to make them as robust as possible. When you design a high-speed serial bus into a product, the money and time you spend on design and parts are two of the best risk trade-offs you can make. The cost of an extra run through the EMI and ESD ranges is more than that of the components and design time to put them on the pc board and build a hundred or so boards. It is also well worth the cost if the schedule is critical and a second or third run through the ESD and EMI ranges would cause you to miss a critical window. When board volumes are higher, the balance can change. Building thousands of boards and saving a dollar per board would pay for several runs through the ESD and EMI ranges. Remember, though, that it costs little to design a board to accommodate many protective items that may later prove superfluous. To manage the costs, if a component turns out to be unnecessary, you can remove it from the bill-of-materials cost or replace it with an inexpensive, 0Ω resistor. This exercise constitutes a classic balancing of risk, and each designer must do it. EDN

## AUTHOR'S BIOGRAPHY

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