General-purpose components implement USB-based data-acquisition system

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Figure 1 presents a Design Idea for a USB-based data-acquisition system that uses a serial ADC employing general-purpose components, such as D flip-flops, a binary counter, and a shift register. Using the DLP-USB245M FIFO-to-USB-converter module from DLP Design (www.

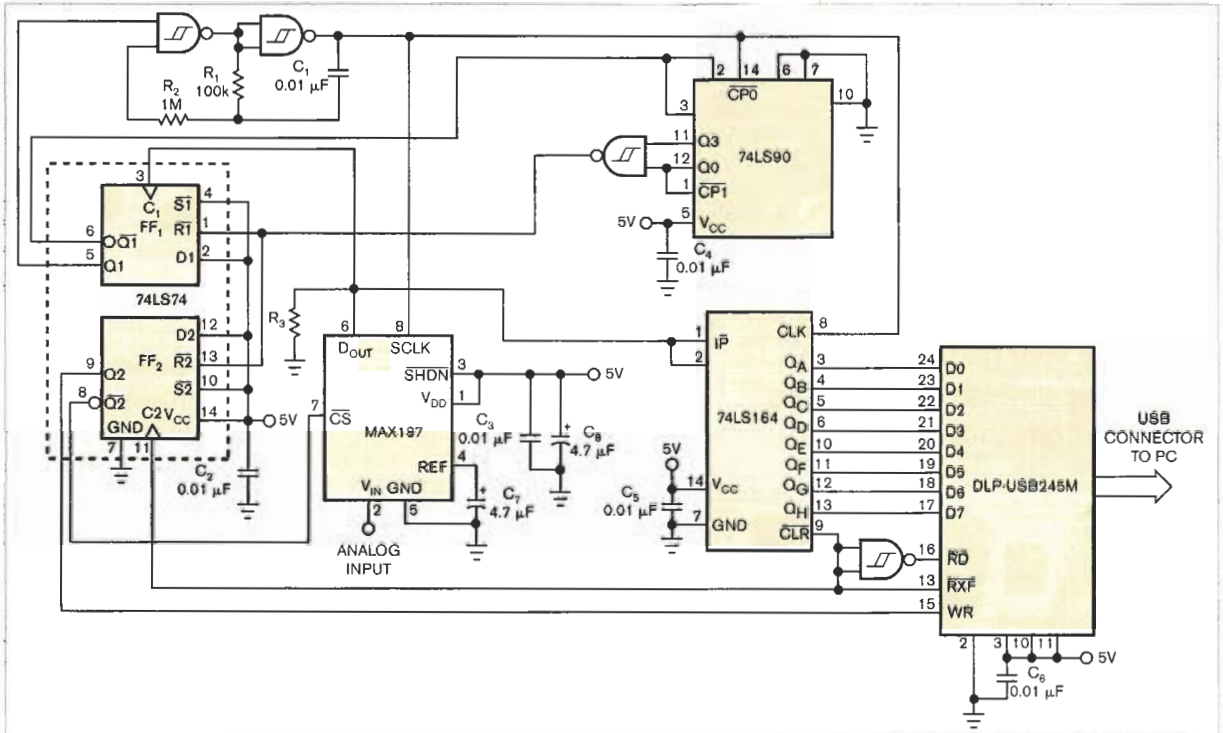

Figure 1 This circuit performs a serial-to-parallel conversion of serial-ADC data and transfers the data to the USB port of a PC.

dlpdesign.com), you can communicate with the peripheral device through the USB port of a host computer. You can write your own program to read and write the data through this module or simply download free test-application software available from DLP's Web site. Additionally, you could download National Instruments' (www.ni.com) LabView serial-read and-write VIs (virtual instruments).

Writing a dummy block of data from the host computer to the buffer of the DLP-USB245M generates a spike at the module's $\overline{RXF}$ pin, which triggers the D flip-flop, FF_2 of the 74LS74. The flip-flop's $\overline{Q2}$ pin initiates the conversion cycle of the MAX187 serial ADC from Maxim (www.maxim-ic.com) by pulling down its chip-select pin. The ADC's end-of-conversion cycle causes a low-to-high transition from its D_{OUT} pin, which triggers the other D flip-flop, FF_1 of the 74LS74, to generate a gating pulse, Q1, for the serial-clock pulses that read the data from the same D_{OUT} pin of the ADC. The 74LS90 binary counter counts the serial-clock pulses. When the count reaches nine, the counter resets the gating pulse for the serial clock and pushes back the chip-select signal to a high level by resetting both FF_1 and FF_2, ending the ADC's acquisition cycle.

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The system acquires the data at the falling edge of the MAX187's SCLK pin and shifts it into the 74LS164 serial-to-parallel shift register at the rising edge of the next SCLK. The MAX187 needs nine serial-clock pulses to shift valid 8-bit data. This circuit uses only 8 bits of the 12-bit ADC. If the circuit requires all 12 bits, then you must connect all NAND gates at the appropriate outputs of the binary counter to generate a reset signal by its 13th clock pulse, and you must make the shift register larger.

The serial data from the ADC converts to parallel data in the serial-to-parallel shift register; a WR (write) signal to the DLP-USB245M then transfers this data to the PC. This action is a complement of the $\overline{CS}$ signal from Q2 of the 74LS74. The DLP-USB245M's $\overline{RXF}$ pin generates a trigger to initiate the conversion cycle and clears the previous data of the shift register. EDN