Fast-settling synchronous-PWM-DAC filter has almost no ripple

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An inexpensive way to implement high-resolution digital-to-analog conversion is to combine microcontroller-PWM (pulse-width-modulated) outputs with precision analog-voltage references, CMOS switches, and analog filtering (**Reference 1**). However, PWM-DAC design presents a big design problem: How do you adequately suppress the large ac-ripple component inevitably present in the switch's outputs? The ripple problem becomes especially severe when you use typical 16-bit microcontroller-PWM peripherals for DAC control; such high-resolution PWM functions usually have long cycles because of the large 2^{16} countdown modulus of 16-bit

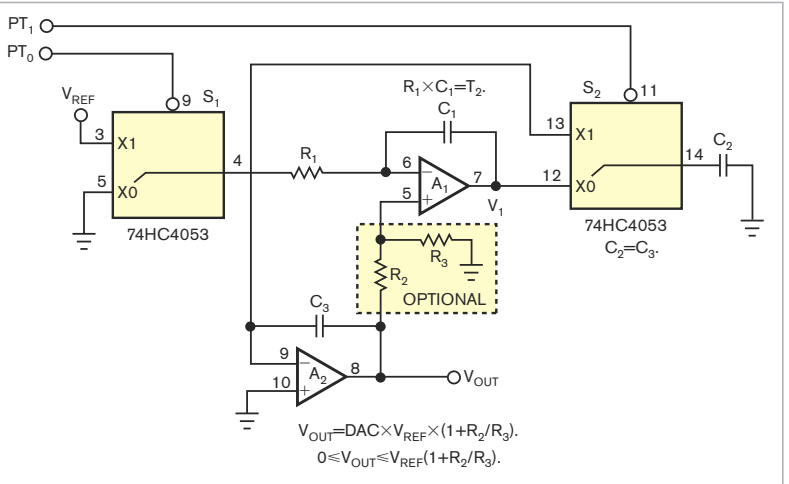

Figure 1 This DAC ripple filter combines a differential integrator, A_1, with a sample-and-hold amplifier, A_2, in a feedback loop operating synchronously with the PWM.

timers and comparators. This situation results in ac-frequency components as inconveniently slow as 100 or 200 Hz. With such low ripple frequencies, if you employ enough ordinary analog lowpass filtering to suppress ripple to 16-bit—that is, −96-dB—noise levels, DAC settling can become a full second or more.

The circuit in **Figure 1** avoids most of the problems of lowpass filtering by combining a differential integrator, A_1, with a sample-and-hold amplifier, A_2, in a feedback loop operating synchronously with the PWM cycle, T_2 in **Figure 2**. If you make the integrator time constant equal to the PWM cycle time—that is, $R_1 \times C_1 = T_2$—and, if the sample capacitor, C_2, is equal to the hold capacitor, C_3, then the filter can acquire and settle to a new DAC value in exactly one PWM-cycle time. Although this approach hardly makes the resulting DAC exactly "high speed," 0.01-sec settling is still 100 times better than 1-second settling. Just as important as speed, this improvement in settling time comes without compromising ripple attenuation. Ripple suppression of the synchronous filter is, in theory, infinite, and the only limit in practice is nonzero-charge injection from S_2 into C_3. The choice of a low-injected-charge switch for S_2 and an approximately 1-μF capacitance for C_3 can easily result in ripple amplitudes of microvolts.

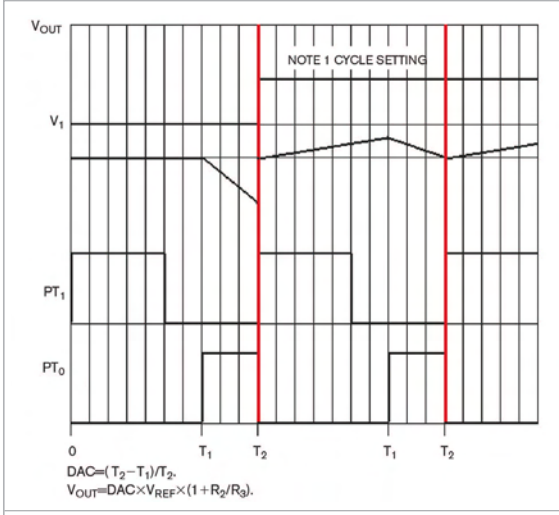

Figure 2 The DAC output settles within one cycle.

Optional feedback-voltage divider R_2/R_3 provides flexibility in a DAC-output span with common voltage references. For example, if $R_2=R_3$, then a 0 to 10V output span will result from a 5V reference. An additional advantage of this method of span adjustment is that output ripple remains independent of reference amplification. EDN

REFERENCE

1 Woodward, Steve, "Combine two 8-bit outputs to make one 16-bit DAC," *EDN*, Sept 30, 2004, pg 85, www.edn.com/article/CA454640.