Deglitcher circuit refines d-a-converter output

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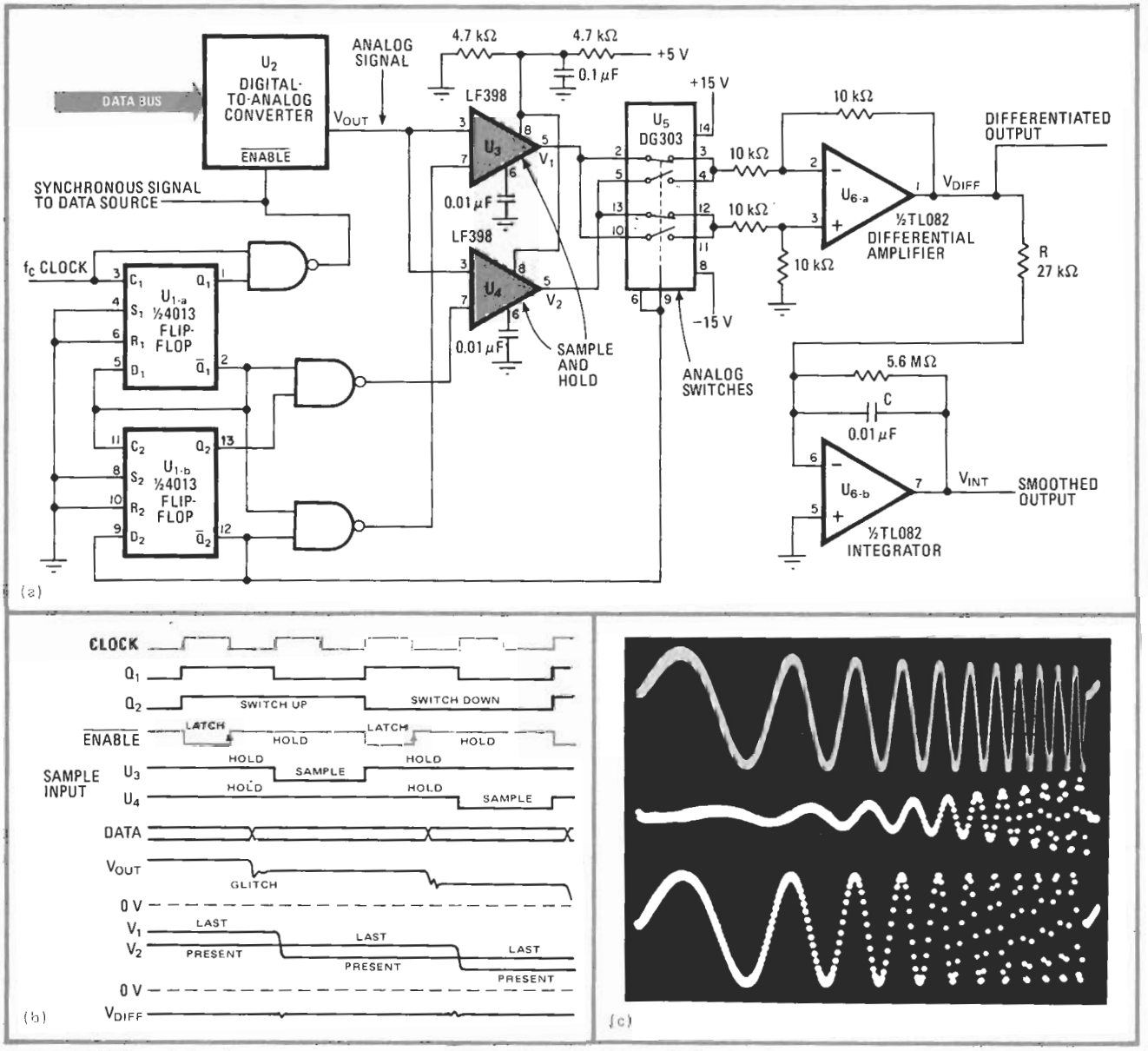
The output of a digital-to-analog converter is often distorted and requires filtering. This deglitcher-differentiator design suppresses unwanted pulses and thus smooths a d-a-converter's output. Alternatively, the circuit offers an efficient means of differentiating low-frequency analog signals, an improvement over a previous circuit [*Electronics,* Jan. 27, 1983, p. 112].

Successive d-a-converter outputs or continuous analog signals are alternately sampled by sample-and-hold circuits U_3 and U_4 at half the clock's frequency (a). D-type flip-flop $U_{1\text{-}b}$ stretches the pulses supplied by flip-flop $U_{1\text{-}a}$ by one clock cycle and directs them to the sample inputs of U_3 and U_4 while latching data into converter U_2 on the rising edge of every second clock cycle (b). A synchronizing signal generated by $U_{1\text{-}a}$ informs the data source that new data must be loaded once it goes high.

To allow glitches to settle, U_3 and U_4 sample the d-a-converter output a half clock cycle after new data is latched in. U_3 and U_4 alternately hold the current and preceding outputs while analog switch U_5 sends the inputs to the differential amplifier $U_{6\text{-}a}$ in sync with the sampling frequency. Thus the differential-amplifier output (V_{diff}) becomes ($V_{present}$–V_{last}). This output is integrated



Polished. This linear interpolator-differentiator circuit (a) samples, differentiates, and integrates the analog output of a d-a converter to provide a smooth digital-to-analog-converter output. The sample-and-hold circuits U_3 and U_4 sample the d-a-converter output at a sampling frequency of $f_c/2$ and feed the differential amplifier $U_{6\text{-}a}$ through analog switch U_5. The differential output (b) is further integrated to obtain a smooth output. The oscilloscope photo (c) shows the response of an exponentially swept sine wave, the smooth output being shown at the top.

to obtain a smooth analog output V_{int}, which is a linear interpolation between successive converter outputs. The RC time constant is adjusted to make the output equal in amplitude to the converter's output. The photo (c) shows the circuit's response to an exponentially swept sine wave. The top wave is a smooth output, the next one represents a differential output, and the last response is the output of the d-a converter. □