BY BONNIE BAKER

Comparing DAC architectures

Entry-level engineers know ADC topologies so well that during interviews, most job seekers can draw and explain fundamental block diagrams. The same situation does not hold true for DAC topologies. In this case, applicants can tell me only the basics: Digital goes in, and analog comes out.

DACs you find in high-precision control-loop applications typically use the R2R (resistor ladder) MDAC (multiplying DAC, **Figure 1a**). This architecture can achieve high-voltage output. MDAC manufacturers can design high-resolution (16-bit) devices with ±1 LSB INL (integral-nonlinear) and DNL (differential-nonlinear) specifications. MDACs require an external current-to-voltage operational amplifier but exhibit fast settling time (less than 0.3 µsec) with a multiplying bandwidth that can be greater than 10 MHz.

The R2R-back DAC is most appropriate for industrial applications (**Figure 1b**). With this DAC, each update involves switching the 2R legs to either the voltage reference high, V_{REF-H} or the voltage reference low, V_{REF-L}. This architecture can be relatively simple to manufacture. The R2R architecture has a parallel data-input bus. For devices with a serial interface, the multibit DAC uses a serial-to-parallel register internally before latching the data to the DAC. In either case, gate-switch timing skews manifest themselves at the DAC's output as glitches. The R2R-back DAC, like the MDAC, typically has excellent low noise, INL, and DNL performance, with medium settling-time capability.

The string DAC suits portable-instrumentation, closed-loop-servo-control, process-control, and data-acquisition systems (**Figure 1c**). The **figure** shows a model of a 3-bit-resistor string DAC. Here the digital-input code is 101b, which decodes to $5/8V_{REF}$. The output-stage buffer isolates the internal resistive elements from the output load. The string DAC is a low-power option that guarantees monotonicity with good DNL performance across the input-code range. The glitch energy is typically lower than that with other types of DACs; however, the INL performance is sensitive to chip layout and depends on resistive-array matching. The noise of string DACs is also relatively high and again depends on the resistive-string-array impedance. EDN

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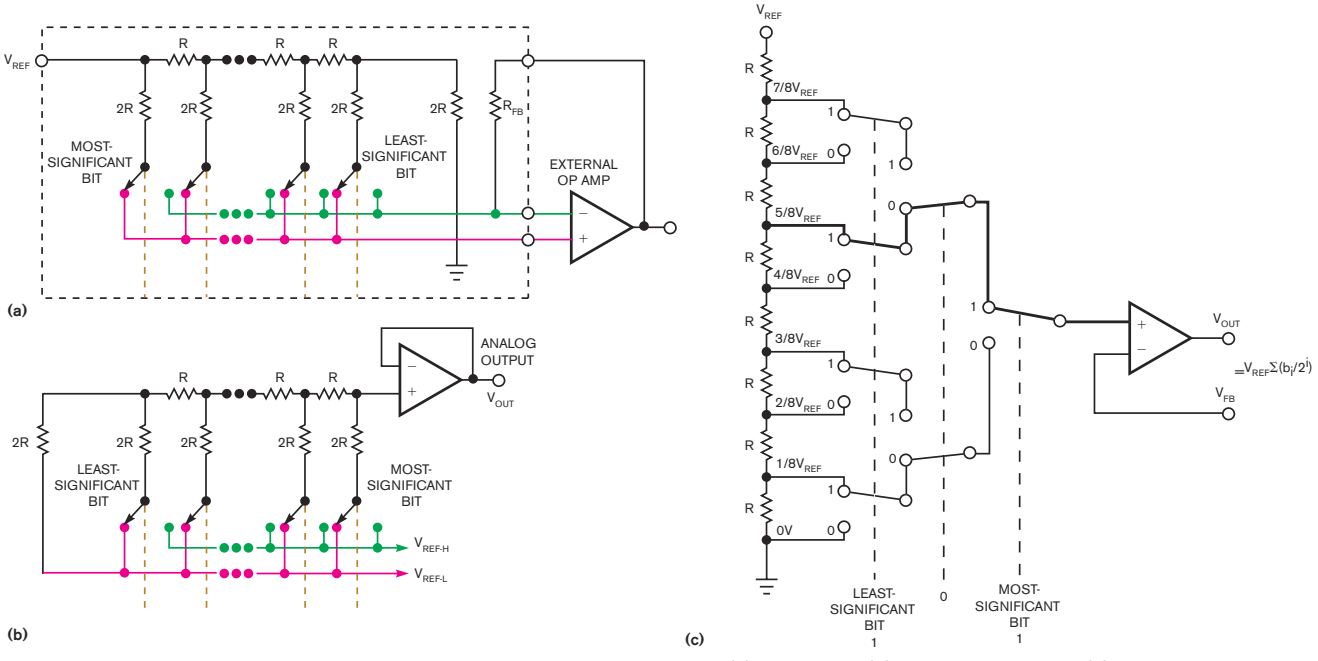

Figure 1 Typical topologies of popular DACs include R2R-multiplying (a), R2R-back (b), and resistor-string (c) architectures.