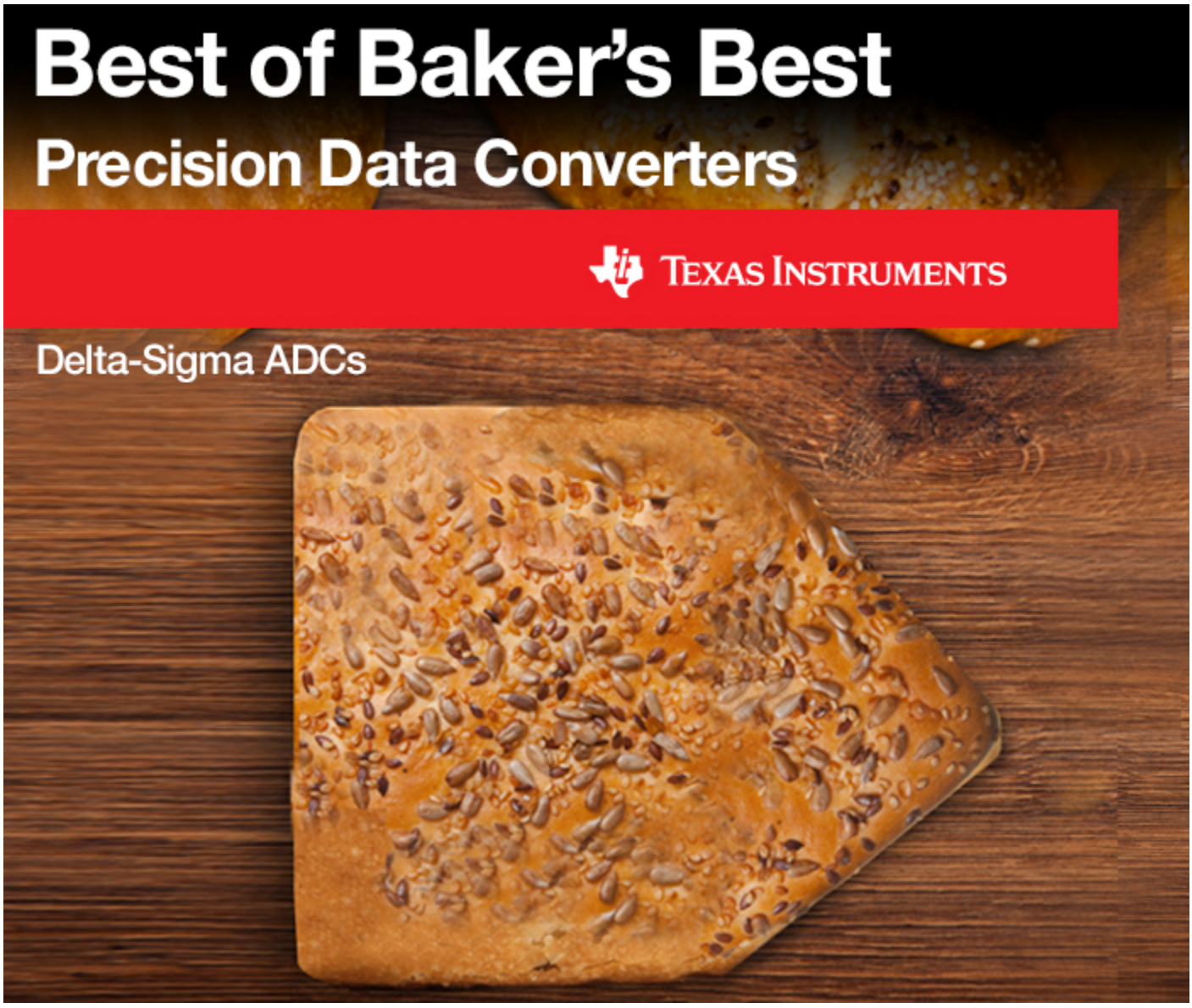

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Introduction

The Best of Baker's Best – *Delta Sigma ADCs*

Introduction by Bonnie Baker

Data converters bridge the space between the analog and digital domains in your circuits. This feat is done with analog-to-digital and digital-to-analog converters. With this book chapter, the definition of delta-sigma analog-to-digital converter (ADC) targets the precision space where millivolts, linearity, and noise matter. The delta-sigma ADC is the most recent data converter topology on the market today. This topology, more than any other topology, exploits digital functions with programmable entities.

The following excerpts from the EDN Baker's Best column represent the best of my delta-sigma ADC short articles. They have been complied for your convenience. Please enjoy your read through and let me know what you think!

P.S. Want to learn more about data converters? We have even more information about data converters on our TI website and in the Precision Hub blog on the TI E2E™Community.

Delta-sigma ADCs

In the semiconductor industry, delta-sigma analog-to-digital converters (ADCs) arrived after the SAR-ADC. The delta-sigma ADC tackled and absorbed a lot of analog issues. With this type of data converter, the analog amplification accomplished by the operational and instrumentation amplifier was replaced with the delta-sigma's digital gain. If you don't know what digital gain is or if you want to know more about the delta-sigma data converter, read on.

1. Delta-sigma ADCs in a nutshell, part 1

Delta-sigma analog-to-digital converters (ADCs) are ideal for converting signals over a wide range of frequencies from DC to several megahertz with very-high-resolution results. **Figure 1** shows the basic topology, or core, of a delta-sigma ADC, which has an internal delta-sigma modulator in series with a digital filter. As you explore delta-sigma ADCs, you will find that, although they have a variety of other features, they all possess this basic structure. This article and the next three *Baker's Best* articles explore the basic topology and functions of these two modules.

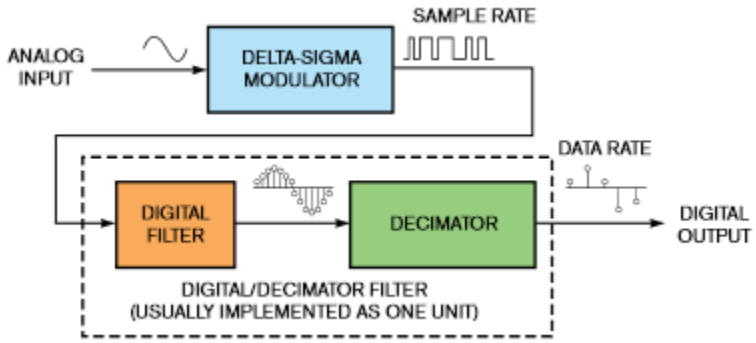

Figure 1. The core functions inside any delta-sigma ADC are a delta-sigma modulator and a digital/decimator filter.

The input signal to the delta-sigma ADC is an AC or DC voltage. This and the next three *Baker's Best* articles use a single cycle of a sine wave as the input signal. Using a 1-bit internal ADC, the internal data converter modulator in **Figure 1** samples the input signal, producing a coarse, quantized output. The modulator converts the analog-input signal into a high-speed, pulse-wave representation. The ratio of ones to zeros in the modulator's output pulse train mirrors the input-analog voltage. Although the modulator produces a noisy output, future articles will show that the circuit "shapes" this noise into the higher frequencies of the output spectrum. This action paves the way for a low-noise, high-resolution conversion at the output of the digital filter.

At the modulator output, the digital filter addresses high-frequency noise and high-speed-sample-rate issues. Because the signal now resides in the digital domain, you can apply a lowpass digital filter to attenuate the higher frequency noise and a decimator filter to slow down the output-data rate. The digital/decimator filter samples and filters the modulator's stream of 1-bit codes and creates a slower multibit code.

Although most data converters have only one sample rate, delta-sigma ADCs have two: the input sampling rate, and the output-data rate. The ratio of these two meaningful variables defines the system's decimation ratio. A strong relationship exists between the decimation ratio and the data converter's effective resolution. A future article will examine how the modulator, digital/decimator filter, and adjustable decimation ratio work.

References

1. Baker, R Jacob, *CMOS Mixed-Signal Circuit Design: Volume II*, John Wiley & Sons, 2002, ISBN: 0471227544.
2. Video: The nuts and bolts of the delta-sigma.

2. Delta-sigma ADCs in a nutshell, part 2: the modulator

A delta-sigma analog-to-digital converter (ADC) uses many samples from the modulator to produce a stream of 1-bit codes. The delta-sigma ADC accomplishes this task by using an input-signal quantizer running at a high sample rate. Like all quantizers, the delta-sigma modulator takes an input and produces a stream of digital values that represents the voltage of the input. You can look at the delta-sigma modulator in the time or in the frequency domain. If you look at a time-domain representation, you can see the mechanics of a first-order modulator (**Figure 1**).

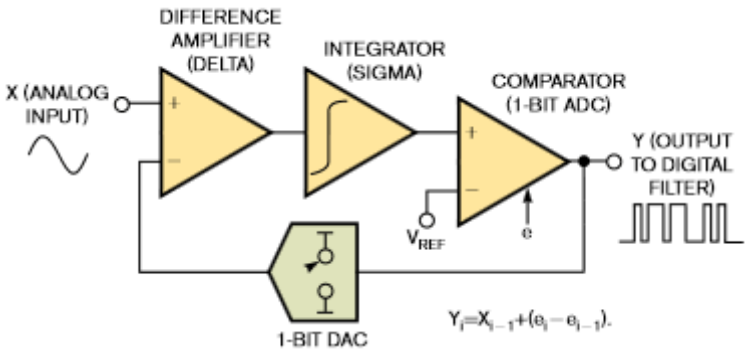

Figure 1. A time-domain representation shows the mechanics of a first-order modulator.

The modulator measures the difference between the analog-input signal and the analog output of a feedback digital-to-analog converter (DAC). An integrator then measures the analog-voltage output of the summing junction and presents a sloping signal to the 1-bit ADC. The 1-bit ADC converts the integrator's output signal to a digital one or zero. Using the system clock, the ADC sends the 1-bit digital signal to the modulator's output, as well as back through the feedback loop, where a 1-bit DAC is waiting.

The 1-bit ADC digitizes the signal to a coarse output code that has the quantization noise (e^i) of the converter. The modulator output is equal to the input plus the quantization noise, (e^i–e_{i-1}). As this formula shows, the quantization noise is the difference of the current error (e^i) minus the previous error (e_{i-1}) of the modulator. The time-domain output signal is a pulse-wave representation of the input signal at the sampling frequency, fS. If you average the output-pulse train, it equals the value of the input signal.

The frequency-domain diagram tells a different story (**Figure 2**). The time-domain output pulses in the frequency domain appear as the input signal (or spur) and shaped noise. The noise characteristic in **Figure 2** is the key to the modulator’s frequency operation.

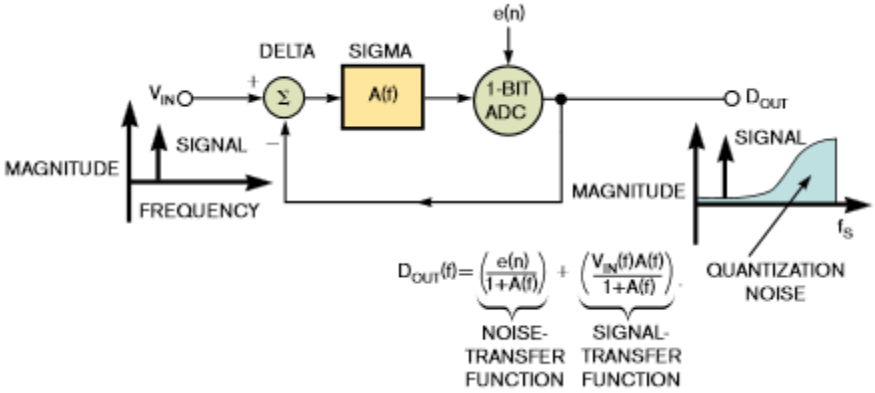

Figure 2. In a frequency-domain representation, the noise characteristic is key to the modulator's frequency operation.

Unlike most quantizers, the delta-sigma modulator includes an integrator that shapes the quantization noise. The noise spectrum at the modulator output is not flat. More important, in a frequency analysis, you can see how the modulator shapes the noise to higher frequencies, facilitating the production of a higher resolution result.

The modulator output in **Figure 2** shows that the quantization noise of the modulator starts low at 0 Hz, rises rapidly, and then levels off at a maximum value at the modulator sampling frequency.

Integrating twice with a second-order modulator, instead of just once, is a great way to minimize low-frequency quantization noise. Most delta-sigma modulators are of a higher order. For instance, the designs of the more popular delta-sigma ADCs include second-, third-, fourth-, fifth, or sixth-order modulators. Multi-order modulators shape the quantization noise even harder to higher frequencies.

References

1. Baker, Bonnie, Delta-sigma ADCs in a nutshell, *EDN*, Dec 14, 2007.
2. Baker, RJ, *CMOS mixed-signal circuit design*, Wiley & Sons, ISBN 0471227544, May 2002.
3. Video: The nuts and bolts of the delta-sigma.

3. Delta-sigma ADCs in a nutshell, part 3: the digital/decimator filter

Following the modulator in the delta-sigma analog-to-digital converter (ADC) is a digital/decimator circuit. This circuit samples and filters the modulator stream of 1-bit codes. At the modulator output, high-frequency noise and high-speed sample rates are problems. However, because the signal now resides in the digital domain, you can apply a digital-filter function to attenuate the noise and a decimator function to slow the output data rate. Designers often intertwine the digital filter and decimator functions in the same silicon.

Figure 1 shows the signal as it travels through the digital/decimator-filter functions. The digital-filter function operates at the same rate as the modulator sampling rate (**Figure 1a**). Notice that the 24-bit code-train resembles the original signal (*reference 1* and *reference 2*). In the time domain, it looks like the digital-filter function is responsible for the low noise and high resolution of the delta-sigma ADC. However, this function provides a second-order impact on the system noise by rejecting higher frequency noise, where the noise shaping from the modulator dominates noise reduction in the lower frequency band (**Figure 1b**).

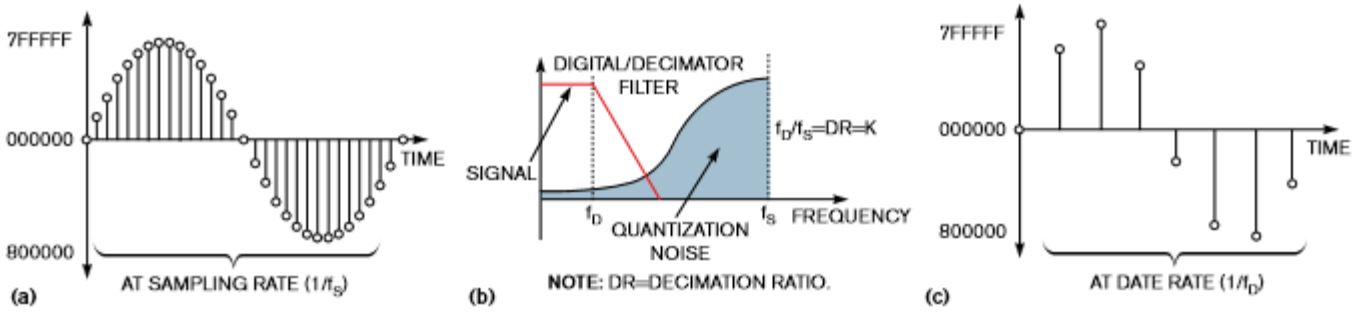

Figure 1. The digital-filter output function produces a high-resolution result (a), while rejecting high-frequency noise (b). The decimator function slows the output data rate (c).

The digital-filter function provides a digital version of the input, but the data rate is still too fast to be useful. Although it might appear that you have an abundance of high-quality, multibit samples at a high sampling rate, you don't need most of this data.

The second function of the digital/decimator filter is the decimator. Decimation is the process of reducing a digital signal's output rate to the system's Nyquist frequency. One simple way to implement a decimating function is to average together groups of 24-bit codes (**Figure 1c**). The decimator accumulates these high-resolution data words, averages several words together, outputs the average results, and dumps the data for the next average. A more economical way to implement a low-power decimator function is to simply pick out a 24-bit word every Kth sample without performing additional averaging. (K is equal to the oversampling or decimation ratio.)

Almost all delta-sigma ADCs incorporate a class of averaging filters called sinc or FIR filters, named for their frequency response. Many delta-sigma ADCs use other filters with sinc filters for two-stage decimation. Low-speed industrial delta-sigma ADCs usually use only a sinc filter.

In the frequency domain, you can see that this digital/decimator filter simply applies a lowpass filter to the signal (**Figure 1c**). In so doing, the digital/decimator filter has attenuated the higher frequency-modulator quantization noise. With the reduced quantization noise, the signal re-emerges in the time domain.

References

1. Baker, Bonnie, Delta-sigma ADCs in a nutshell, *EDN*, Dec 14, 2007.
2. Baker, Bonnie, Delta-sigma ADCs in a nutshell, part 2: the modulator, *EDN*, Jan 24, 2008.
3. Baker, R Jacob, *CMOS Mixed-Signal Circuit Design*, J Wiley & Sons, ISBN 0471227544.
4. Video: The nuts and bolts of the delta-sigma.

4. Delta-sigma ADCs in a nutshell, part 4: noise versus data rate

This article is the last in a brief overview of the inner workings of delta-sigma analog-to-digital converters (ADCs). You have seen how the modulator operates in the time and the frequency domains and how it shapes the conversion-quantization noise into higher frequencies. The modulator implements an oversampling system that has an integrator and negative feedback. You've also read about the inner workings of the digital/decimator filter. This filter reduces the high-frequency noise in the digital 1-bit stream from the modulator while passing the digitized input signal to the data converter output at a reduced data rate. The combination of these two modules yields a high-resolution ADC (*references 1, 2, and 3*).

With any data converter, the actual resolution is equal to the number of bits the ADC transmits. "Effective resolution" describes the useful bits from an analog-to-digital conversion as they relate to signal noise. Effective resolution is equivalent to the ADC's effective number of bits. The ratio of the modulator's F_S (sampling rate) and F_D (output-data rate) define the decimation, or oversampling, ratio, which directly impacts effective resolution. The decimation ratio, whose value ranges from four to 32,768, equals the number of modulator samples per data output.

Consider the frequency spectrum in **Figure 1**. Suppose that you make the output data rate a small fraction of the modulator's sampling frequency (**Figure 1a**). The input frequencies from zero to F_D are in the output-signal band. The effective resolution is high because the noise level is low. A higher frequency for F_D increases the data converter's output-data rate and decreases the effective resolution. Most of the noise from the modulator is in the higher frequencies, but you still have a lower effective resolution (**Figure 1b**). **Figure 1c** shows an example of the relationship between decimation ratio and effective resolution of a sampling ADC.

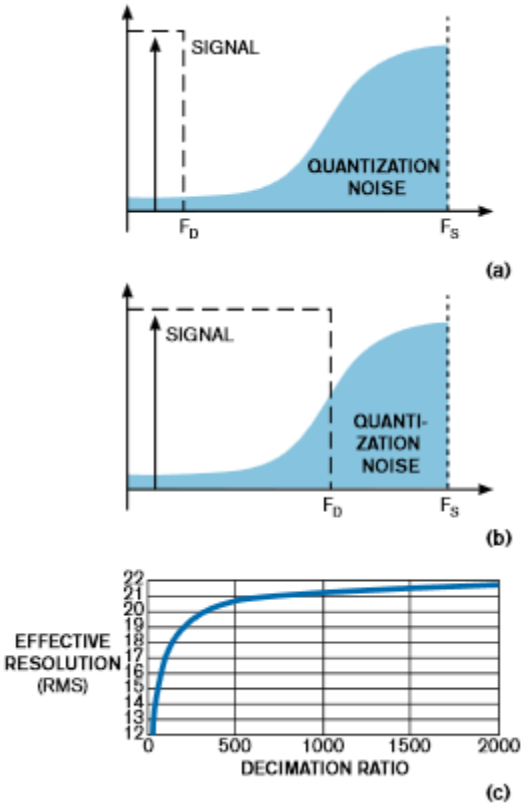

Figure 1. Decreasing the output data rate (a) or increasing the decimation ratio (b) produces a conversion with a higher effective resolution (c).

One way to increase the output-data-rate speed without changing the effective resolution is to increase the modulator-sampling rate. You can increase this rate by increasing the master clock rate to the delta-sigma ADC. With a constant decimation ratio, both the sampling rate and the power consumption increase. Also, most converters have a practical limit for the sampling rate, beyond which they do not function properly. A strong relationship exists between the decimation ratio and effective resolution. Keeping the sample rate constant and lower data rates gives you high effective resolution at the output of the data converter (*references 4 and 5*).

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1. Baker, Bonnie, Delta-sigma ADCs in a nutshell, *EDN*, Dec 14, 2007.
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6. Video: The nuts and bolts of the delta-sigma.

5. Photo-sensing circuits: The eyes of the electronic world are watching

Silicon photo sensors have been in electronic circuits since the inception of the era of silicon electronics. More than likely, scientists quickly discovered the photo-sensing characteristics of silicon in the lab, as they worked from the daylight hours into the evening. To this day, IC designers regularly cover their wafers under test to shield out extraneous light. Although the light sensitivity of silicon is an undesirable by-product of the silicon, system designers have exploited this transfer of light into electrical energy in various systems. Consequently, a wide variety of applications use silicon to sense the intensity and characteristics of light.

In these systems, a silicon sensor converts light into charge or an electrical current. These silicon sensors are the "eyes" in the electronics world that users can employ to analyze blood, search noninvasively for tumors, detect smoke, position equipment, or perform chromatography, to name a few applications. Basically, system designers understand how to convert light into a current,

but the real challenge is determining how to convert the low-level currents from the photo sensor into a useful electrical representation. To further exacerbate the difficulty of the design, the required accuracy in these applications continues to increase.

The traditional design topology of the transimpedance amplifier captures this low-level signal in a hybrid approach that starts with an amplifier and a high-value resistor in the feedback loop. The circuit design uses resistance to provide a real-time, linear representation of the light source. This circuit places the photodiode across the amplifier's inverting input and ground of the operational amplifier. A resistor with a value of 100 kΩ to 10 MΩ connects the inverting input of the amplifier to the output. You then connect the noninverting input to ground (**Figure 1**). Light excitement on the photo sensor generates charge. The only path of escape for this charge is through the high-value resistor in the amplifier's feedback loop.

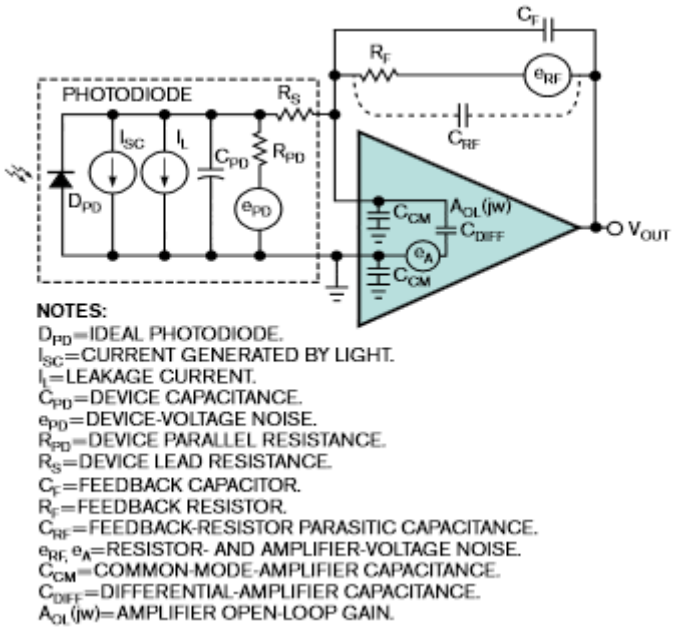

Figure 1. A transimpedance photo-sensing circuit is not without its design challenges.

The simplistic approach in **Figure 1** is not without its design challenges. The operational amplifier must have relatively low-picoampere input-bias currents and low input capacitance. An appropriate amplifier for this circuit would have a FET- or a CMOS-input stage with low-voltage noise and microvolt-offset specifications. In the end, the designer optimizes the stability, bandwidth, low-noise performance, and layout of this transimpedance-amplifier circuit.

The final design method is not always intuitively obvious. The photo sensor, operational amplifier, amplifier-feedback element, and these parts' parasitics combine to create quite a rat's nest of formulas for consideration. The signal after the transimpedance amplifier requires a multipole analog filter. In this manner, combining the input and filtering stages separates the signal of interest from the noise floor. A sampling ADC digitizes the signal after the analog filter.

Photo-sensing circuits have changed over the years. The first approach was purely analog, using the transimpedance amplifier and following it with a lowpass filter. From the classic transimpedance amplifier, the switched integrator has gained favor. The switched integrator was the first step toward bringing the digital portion of the circuit closer to the signal source. The migration of the photo-sensing-application product has moved on to totally integrated systems, such as the charged digitizing ADC.

6. Delta-sigma antialiasing filter with a mode-rejection circuit

The approach to the antialiasing-filter design for the delta-sigma analog-to-digital converter (ADC) is significantly different from the approach you would use for a successive-approximation register (SAR) or pipeline (high-speed) ADC. With SAR and pipeline ADCs, you have systems that evaluate one sample at a time. In both cases, the analog signal is "grabbed" and stored on the data converter's input capacitor array. These data converters evaluate the stored signal and provide a digital representation of that single sample. With both devices, the target frequency for the multiorder, antialiasing filter is the converter's Nyquist frequency.

The delta-sigma ADC's input modulator samples the input analog signal numerous times at a high sample rate (F_S, *reference 1*). The following sinc digital filter resamples and converts a group of these modulator samples to an output digital representation. The conversion process from the modulator's string of samples to a 24-bit digital code is significantly slower (F_D, *reference 1*)

than the sample rate of the delta sigma's input structure. Consequently, the delta-sigma ADC has two sample rates (F_S, F_D). The first-order antialiasing filter's target frequency, however, is the output data rate, F_D. You can find the fundamental antialiasing-filter design concepts for a delta-sigma ADC in *reference 1*.

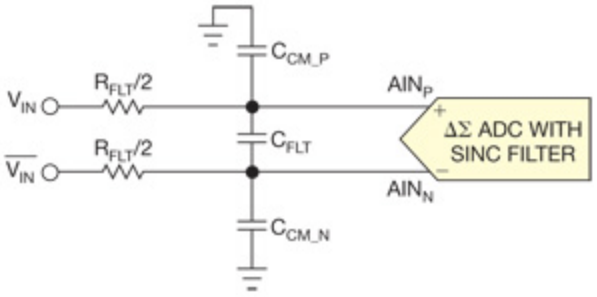

Figure 1. This complete filter attenuates differential noise with R_{FLT} adn C_{FLT} and common-mode noise with C_{CM_P} and C_{CM_N}.

Once you establish the target antialiasing frequency of F_D, you can quickly define the theoretical design formulas, as *reference 2* discusses. The calculation for this theoretical evaluation takes into account resistor noise and converter bits. To determine the theoretical filter resistance (**Figure 1**), use the following equation:

$$R_{FLT(MAX)}=\frac{10^{-(ER\times 0.602)}}{4\times k\times T\times F_D},$$

where ER is the specified effective resolution from the ADC manufacturer's datasheet, k is Boltzmann's constant, and T is the temperature in Kelvin. To determine the theoretical filter capacitance, use the following equation:

$$C_{FLT}=\frac{1}{2\times\pi\times R_{FLT}\times F_D}.$$

Note that the circuits and the discussions presented in *references 1 and 2* address only the reduction of differential noise, with no regard to the input impedance of the ADC or common-mode noise.

In terms of the ADC's input impedance, the capacitors of a switched-capacitor-input, delta-sigma ADC are continuously charged and discharged while measuring a voltage between AIN_P and AIN_N (**Figure 2**). These internal capacitors (C_B, C_{A1}, and C_{A2}) are relatively small when compared with the external circuitry. Consequently, the average input impedance appears to be resistive. The data converter's capacitor values and modulator switching rate set this resistive value.

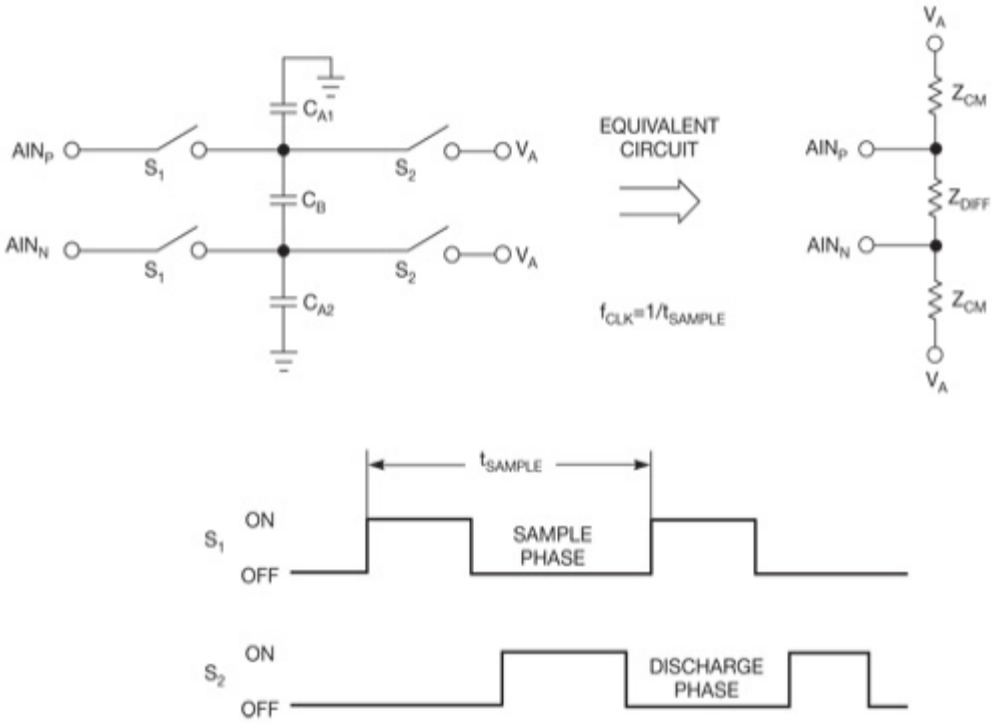

Figure 2. The input impedance of the delta-sigma ADC should be at least 10 times higher than the external filter's resistances.

To measure the common-mode input impedance of the structure in **Figure 2**, tie AIN_P and AIN_N together and measure the average current that each pin consumes during conversion. To measure the differential input impedance, apply a differential signal to AIN_P and AIN_N and measure the average current that flows through the pin to V_A. The common- and differential-mode resistance can range from hundreds of kilohms to hundreds of megohms. Those values depend on the circuitry following the input switching-capacitor structure inside the ADC. The value of $R_{FLT}/2$ must be at least 10 times lower than the data converter's input impedances.

The two common-mode capacitors, C_{CM_P} and C_{CM_N}, attenuate high-frequency common-mode noise. The differential capacitor should be at least an order of magnitude larger than the common-mode capacitors because mismatches in the common-mode capacitors cause differential noise.

If the input signal to any ADC contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, bandlimit the input signals containing noise and interference components. The digital filters in delta-sigma ADCs provide some high-frequency noise attenuation, but the digital sinc filter cannot completely replace an antialiasing filter. When designing an input filter circuit, factor in the interaction between the filter network and the input impedance of the converter.

References

1. Baker, Bonnie, Using an analog filter to inject noise, *EDN*, July 23, 2009.
2. Baker, Bonnie, Analog filter eases delta-sigma ADC design, *EDN*, June 12, 2008.

7. ADCs: Does ENOB tell the whole story?

Near the beginning and end of a total solar eclipse, the thin slice of the sun that's visible appears broken up into beads of light. These lights are called Baily's Beads, after the British astronomer Francis Baily, who first noted the phenomenon in 1836 (*reference 1*). At the moment they occur, you can't see the full picture; much more is going on. For a short time, you cannot see the sun. In same way, the effective-number-of-bits (ENOBs) spec describes only part of an ADC: noise and distortion–rather than providing a precise or accurate description of an ADC.

Be aware of the ENOB pitfalls. It does not describe the ADC's entire operation over the ranges of sampling frequencies and power supplies. Additionally, ENOB numbers exclude DC specifications, such as offset and gain error. Engineers use either an AC or a DC input signal to determine an ADC's ENOB. With an AC input signal, the digital output in a fast-Fourier-transform (FFT) plot shows the fundamental input signal along with the ADC's noise and distortion. In the AC environment, you calculate ENOB from the data converter's signal, noise, and distortion (SINAD), which is the same as total harmonic distortion plus noise (THD+N) or signal-to-noise ratio plus distortion (SNR+D). SINAD is the calculated combination of the SNR and the THD:

$$\text{SINAD (dB)} = -20\log_{10}\sqrt{10^{-SNR/10}+10^{-THD/10}}.$$

THD combines all of the energy from the frequency bins in the FFT that are harmonic multiples of the input signal. To measure SNR, integrate all of the energy in the remaining bins and compare them with the fundamental signal level. Use the following calculation to derive ENOB from SINAD: ENOB=(SINAD–1.76)/6.02. In this simple formula, 6.02 is a multiplier of a 20 $\log_{10}$ of the converter's bits, and 1.76 is the quantization noise.

Using a DC input signal to measure ENOB involves the use of a histogram of the digital output. It shows the average DC value of the input signal and the internal noise of the data converter. The most common measurement for oversampling or delta-sigma ADCs is to calculate the standard deviation, which is equal to the rms noise. If you apply a DC signal to a delta-sigma ADC and record a large number of samples, you can then derive the standard deviation for these codes. The formula for ENOB is: N–log2(σ), where σ is the standard deviation of data and N is the number of converter bits. With delta-sigma ADCs, ENOB, or the effective resolution, changes with adjustments to the oversampling or decimation ratio. Generally, the effective resolution of delta-sigma ADCs decreases with increasing data output rates.

ENOB for AC measurements uses a SINAD calculation, which is a combination of the SNR and THD. The AC measurement is dynamic, requiring a sine-wave input. You use this calculation with data converter architectures, such as successive-approximation-register (SAR), pipeline, flash, and high-speed delta-sigma ADCs. ENOB for DC measurements using rms, or the standard deviation of the noise calculation with a DC input signal. Slower delta-sigma ADCs use this type of measurement.

In both cases, remember that ENOB is a simple although somewhat superficial figure of merit, but it still has its place. So, when you use ENOB to make decisions, take time to look beyond the Baily's Beads in your eclipse. In some cases, the ENOB value may be misleading, when you may have a perfectly usable data converter for your application.

Reference

1. Video: The basics of the effective number of bits.

8. How the SNRs of delta-sigma ADCs differ

When I was a child, my parents bought me a 1-in.-diameter box turtle. I was so excited! To protect the turtle, I was going to put it in my block wagon. This wagon had slots to insert square, triangular, and round pegs. When my mom saw me grab a hammer, she knew it wouldn't be a pretty picture. "You can't fit a square peg–or a turtle–into a round hole," she told me.

That lesson also applies to the basic concept underlying delta-sigma modulators and analog-to-digital converters (ADCs)–a concept that has been around since the 1930s. This converter topology is a bit different from other topologies; however, many engineers still strive to fit this data converter into the standard ADC square hole.

Delta-sigma ADCs go beyond performing a simple analog-to-digital conversion. They have an oversampling mechanism, a modulator, and a digital filter. The oversampling mechanism spreads the noise power across a wider frequency range. The modulator shapes the low-frequency noise or pushes it out to higher frequencies. The digital filter averages the noise and eliminates it in the higher frequencies. The ideal successive-approximation-register and pipeline signal-to-noise ratio (SNR) is 6.02N+1.76 (*reference 1*), where N is the number of data converter bits. The delta-sigma ADC SNR is $6.02(N+N_{INC})+1.76$, where N is the number of modulator bits and N_{INC}, the increase in resolution, is:

$$N_{INC} = \frac{1}{6.02}\left[(20M+10)\log_{10}K - 20\log_{10}\left(\frac{\pi^M}{\sqrt{2M+1}}\right)\right]$$

In this formula, M is the order of the modulator, and K is the oversampling ratio during the conversion.

Ideally, the delta-sigma ADC SNR, with a first order modulator, is $6.02N+1.76–5.17+30\log_{10}OSR$ where OSR is the oversampling rate and N is the number of modulator bits–not data converter bits (**Figure 1**).

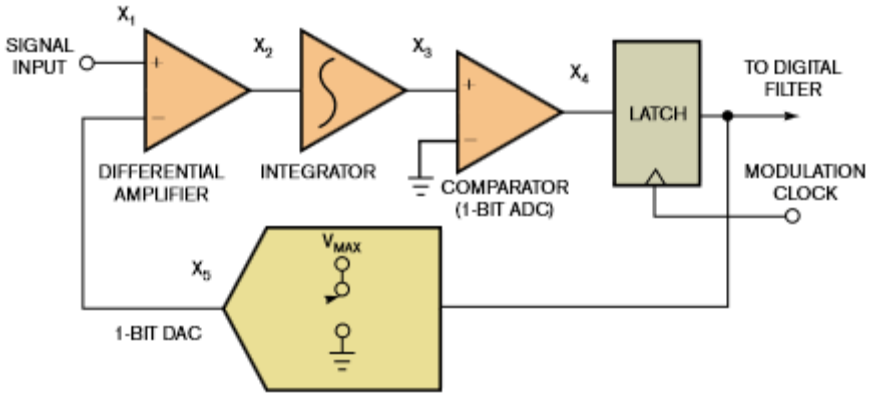

Figure 1. With a first-order modulator at the input of a delta-sigma ADC, the ideal SNR is 6.02N 1 1.76 2 5.17 1 30log$_{10}$ OSR.

These ideal formulas assume that the linearity, noise, and offset errors of the ADC and DAC–usually, 1-bit devices–are ideal and that the digital filter has an ideal brick-wall response. Actual delta-sigma ADCs are not as ideal as you would hope.

With these theories of the ideal, the best approach is still to rely on bench data for your data converter performance. This data gives you a realistic view of the data converter's capabilities. On the bench, you can measure your data converter's rms noise by acquiring a few hundred samples of a DC-input signal. In this circumstance, the formula that describes any ADC SNR is $20\log_{10}(V_{RMS\text{-}FS}/V_{RMS\text{-}NOISE})$.

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9. Jitter and the ins and outs of SNR

When you use a high-speed analog-to-digital converter (ADC), you expect the performance to meet the published datasheet signal-to-noise-ratio (SNR) value. When you test the ADC's SNR, you might attach a low-jitter clock device to the ADC's clock pin and apply a reasonably low-noise input signal. Several sources of noise errors can cause your ADC to fail to meet the publisher specs.

If you are certain that you have a low-noise input signal and a good layout, the combination of the input-signal frequency and the jitter from your clock device is probably the cause of the problem. You will find that low-jitter clock devices are adequate for most ADC applications. However, if both the input-signal frequency to the ADC and the data converter's SNR are high, you may need to improve your clock circuit.

Low-jitter clock devices, at best, have advertised 1-psec jitter specifications, or you can generate an equally inferior clock signal from an FPGA. Issues that contribute to the SNR error of your high-speed ADC include ADC quantization noise, differential-nonlinearity (DNL) effects, the ADC's effective internal input noise, and jitter. You can determine whether jitter is the problem by using the following equation, which provides the ADC's SNR error that the external clock and ADC jitter exclusively generate:

$$SNR_{CLK} = -20\log_{10}(2\pi f_{IN} \times t_{JITTER-TOTAL})$$

where f_{IN} is the input signal's frequency to the ADC and $t_{JITTER-TOTAL}$ is the rms jitter from the clock signal and ADC clock's input circuitry. Note that f_{IN} is not the clock frequency (f_{CLK}). A jitter of 1 psec from the external clock to the ADC is adequate for some but not all high-speed ADC applications (**Figure 1**).

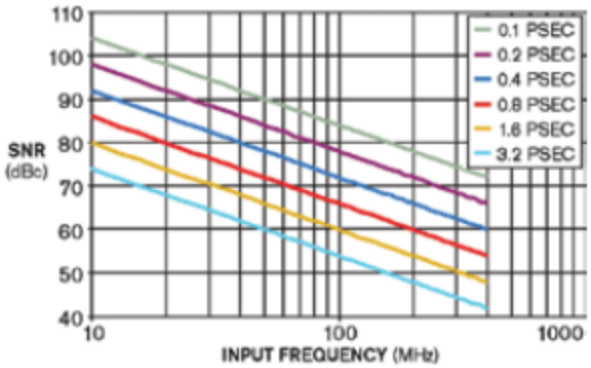

Figure 1. The SNR due to jitter is a function of the input signal's frequency.

The equation allows you to calculate an estimate of the required clock jitter for a given ADC. For instance, with an ADC with a specified 70-dB SNR and a 100-MHz input signal, you can calculate the value of $t_{JITTER-TOTAL}$ as 503 fsec. If the input ADC's aperture jitter is 150 fsec, you can make a high estimate of the external clock-jitter requirements with the following equation:

$$t_{JITTER-CLK} = \sqrt{(t_{JITTER-TOTAL})^2 - (t_{JITTER-ADC})^2}$$

where $t_{JITTER-CLK}$ is the jitter that the clock injects into the ADC and $t_{JITTER-ADC}$ is the ADC's aperture jitter, clock amplitude, and slope. Continuing with the estimate, make $t_{JITTER-ADC}$ equal only to the ADC's internal jitter of 150 fsec and ignore the effects of the clock amplitude and slope. Using this equation, a high estimate of $t_{JITTER-CLK}$ is 480 fsec.

This column only scratches the surface of the issues behind perfecting the clock signal to a high-speed ADC. You need to give further attention to the clock amplitude and slope because they affect the system jitter. Additionally, you must understand how to implement the hardware portion of a low-jitter clock circuit.

For your next clock design, remember that clock jitter affects the ADC's SNR performance in input frequency to the ADC and the actual clock jitter. Additionally, be skeptical of clock-device vendors' claims. Use the evaluation board from the ADC vendor to test your clock sources before you develop your product. You will be happier with the end results.

References

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2. Sanna, Chuck, Using high-IF sampling A/D converters beyond baseband frequencies, *Planet Analog*, Sept 5, 2007.
3. Video: Wu, Lin, Clocking a high-speed ADC, Texas Instruments, 2008.

10. RMS and peak-to-peak noise trade-off

Have you ever noticed that random noise has a predictable pattern? Nature duplicates this pattern in many ways–the gene pool, gambling, and even my driving "habits."

There are two ways to describe random analog noise. The first uses the standard deviation of a collection of data converter digital-output samples. The data's standard deviation is equal to the rms value. The second uses the standard deviation and a constant crest factor to describe an ADC's noise with a peak-to-peak value. Specifications with rms or peak-to-peak descriptors use statistical methods to arrive at a single number that describes the analog device's noise behavior or an analog-to-digital converter (ADC).

You can use rms to describe the system's noise power. 'RMS' may appear with the specified units, or it may be implied. Usually, a noise specification includes the rms term. However, a signal-to-noise ratio (SNR) specification doesn't. SNR uses only decibels for units.

When describing noise with a rms number, you are referring to the positive and negative range of the data's standard deviation. Although the noise's rms value from an ADC is well-defined, you can predict the instantaneous position on the X axis only with the theory of probability. It is possible to create a histogram plot from the DC-output data (**Figure 1a**). By collecting more than 1000 data points, this histogram approaches the shape of a gaussian distribution, or bell-shaped curve. The two standard-deviation or rms lines capture a significant number of the noise occurrences. The probability that the noise from an analog device produces one output value that lands between the two rms lines is approximately 68%.

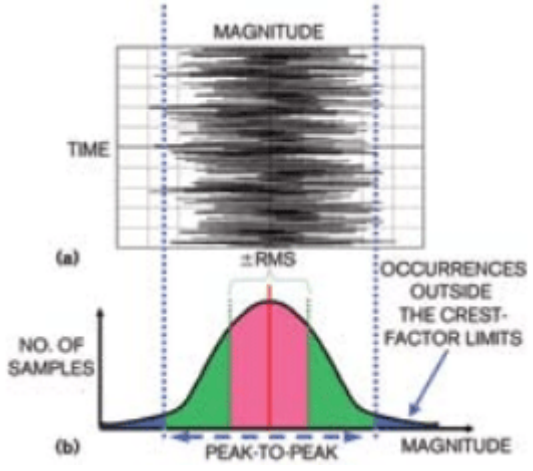

Figure 1. Organize data from a time plot (a) into a histogram to help determine rms and peak-to-peak limits (b).

If you are putting output data from an ADC into a digital display, the peak-to-peak noise representation becomes important. Here, you determine how often and how many display digits can fluctuate, keeping in mind that fluctuating digits create user or customer insecurity. With a histogram plot, the rms limits exclude a considerable amount of data (**Figure 1b**). Multiplying the doubled standard deviation by a crest factor expands the percentage of occurrences underneath the curve. The crest factor for noise occurrences is a statistical estimate that determines the probability that an occurrence of a noisy event will remain within a defined boundary.

Predicting the allowable fluctuation in your data display is relatively simple. After choosing a crest factor, multiply the value of two standard deviations by the selected crest factor. The industry standard is 3.3, which is appropriate for a three-digit display

(Table 1). If you are keeping a five-digit display stable, use a crest factor of 4.4. The lower digits in your display will fluctuate 0.001% of the time.

TABLE 1 DISPLAY FLUCTUATION

Crest factor	Occurrences inside limits (%)
2.6	99
3.3	99.9*
3.9	99.99
4.4	99.999**
4.9	99.9999

*Industry standard
**Stable to five display digits

Table 1. Multiply the crest factor times twice the data's standard deviation to estimate the data peak-to-peak limits.

Use rms or peak-to-peak figures to describe an analog device's input- or output-referred noise. Datasheets and labels may have noise specifications with units such as volts rms or volts peak-to-peak. You can quickly describe the noise power visible at the output of a data converter with the data's standard deviation. Control the fluctuating digits in your display by defining peak-to-peak limits.

11. Analog filter eases delta-sigma ADC design

Delta-sigma analog-to-digital converters (ADCs) with sinc (sinx/x) digital filters change the signal chain's complex antialiasing-filter requirements to a simple, first-order, passive filter. With this "easy-to-design" circuit, you can tackle the major noise contributors around the delta-sigma modulator's sampling frequency. The ADC's characteristics that you use in this filter design are the modulator-sampling rate, F_S, and output-data rate, F_D.

The frequency response of a sinc digital filter looks like a comb (**Figure 1**). The frequency of the first null in this **figure** is equal to the F_D of the ADC. If you look at the frequency response of a sinc filter up to the modulator's sampling rate, you can see that the sampling frequency is much faster than the ADC's output-data rate.

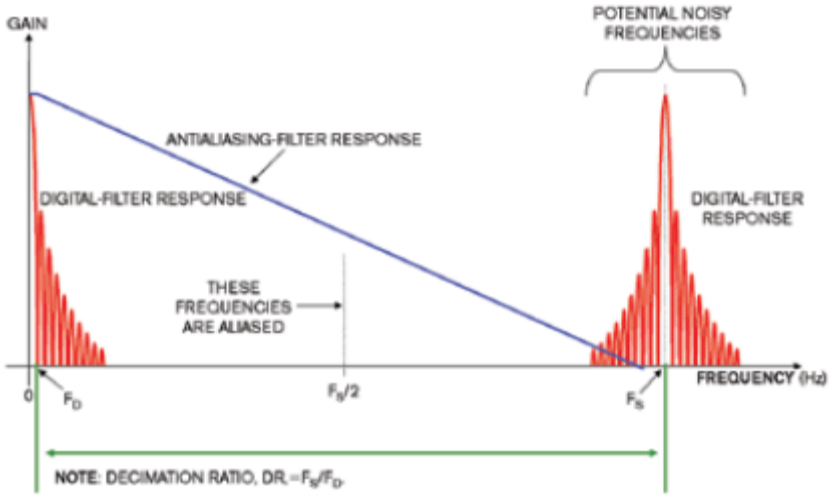

Figure 1. The sinc-digital-filter response is compressed near 0 Hz, and the converter's sampling frequency mirrors and duplicates that response.

Because a delta-sigma ADC is a sampling system, all noise and signals above one-half of the F_S alias back. The sinc digital filter rejects noise over a wide frequency band, but it does not reject system noise around the F_S. The amplitude of the noise and signals hovering around the sampling frequency is small, but noise is a reality. The lower bits may fluctuate because you have a high-resolution ADC.

The corner frequency of your analog filter is equal to the output-data rate, or F_D. Fortunately, this filter has a low-order function, and the appropriate choice is a simple RC filter. If your system has a lot of noise or signals around the region of F_S or if the decimation ratio is less than 100, consider using a second-order, lowpass filter.

Place the analog antialiasing filter before the input of the ADC. **Figure 2** shows the best option for this passive, lowpass filter for a single-channel device, where $F_D=1/(2\pi R_{FLT}\times C_{FLT})$. Because the lowpass filter is a simple RC pair, the values of the filter's resistors (RFLT/2) are easy to choose as long as the resistor noise from DC to the filter's corner frequency is less than one-third of the noise that the delta-sigma ADC generates. The value of the capacitor (C_{FLT}) should be at least 20 times higher than the input capacitance of the ADC. It can be as high as you want, as long as you keep in mind that your filter's corner frequency is equal to or greater than the ADC's output-data rate.

Figure 2. This filter has two equivalent resistors and a capacitor.

If you have extraneous noise in your system, you will be pleased with the results of using this antialiasing filter. You may not find noise in your lab conversions, but make sure you anticipate the location of your system. In the field, extraneous and noisy signals may very well just creep into your ADC.

12. "Muxing" around with delta-sigma ADCs

A multiplexer in your circuit can scan through a number of input channels by sampling each channel in rotation. As a power and cost advantage, multiplexed systems have only one analog-to-digital converter (ADC) that acquires the data from all of the channels. Before starting your design, first look at the types of signals you are trying to digitize. For instance, if you know the highest and lowest frequency as well as the accuracy requirements in all of your system's channels, you may see a need for several ADCs.

In another scenario, the channels may have a unique time relationship to each other, requiring a simultaneously sampling approach that preserves phase information. You achieve this goal with sample-and-hold circuits and a single ADC, or it may be easier to use individual ADCs.

Figure 1 shows a delta-sigma ADC multiplexed circuit with the antialiasing filters on the signal side of the multiplexer. Each channel of this circuit has a near-DC signal at the input of the multiplexed converter. However, a channel-to-channel change can create a step-response signal to the ADC. Thus, it is critical that you use a zero-cycle-latency ADC.

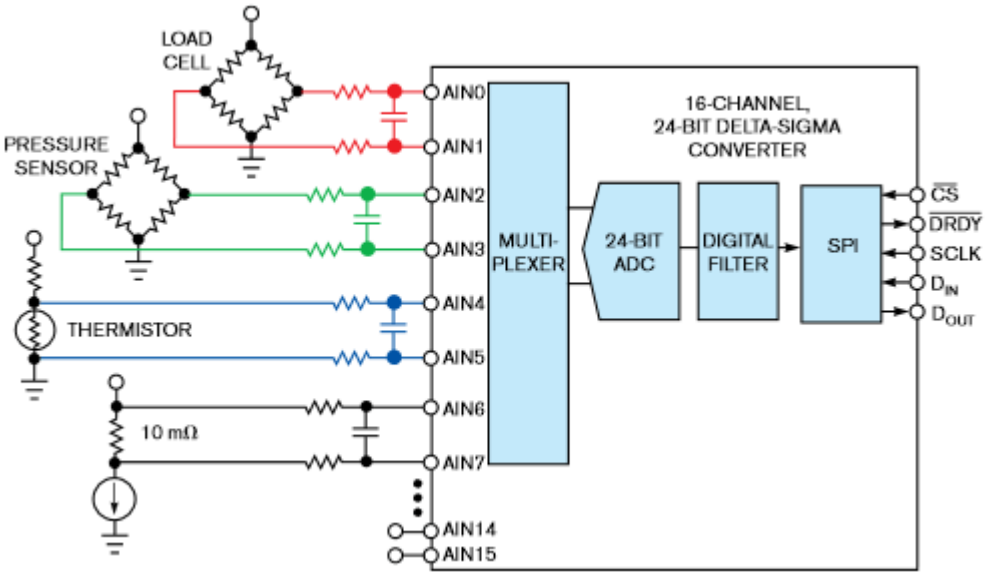

Figure 1. The signal's frequency content at the input delta-sigma ADC is usually slow-moving.

Cycle latency is equal to the number of complete data cycles between the initiation of the input signal conversion and the availability of the corresponding output data. The ADC must be able to generate a fully settled output signal from a step input. If the device completes the conversion before the start of the second cycle, the cycle latency is zero. One possible limitation of multiplexed delta-sigma ADCs is a nonzero cycle latency.

Figure 2 shows the signal-chain dynamics of a multiplexed system with three signals. This system links slices from each input channel. After the multiplexer, the zero-latency delta-sigma ADC sees this merged waveform, which has large and fast transitions as the signal switches from channel to channel. The reaction of the delta-sigma ADC's digital filter to the entire multiplexed waveform means that the fast transitions settle completely within the digital filter.

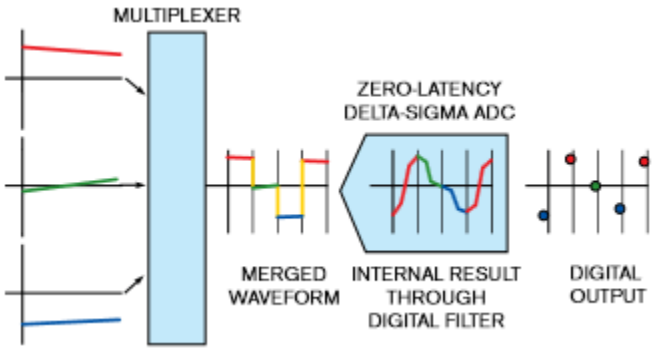

Figure 2. Switching DC signals into the ADC's input can contain high-frequency components.

The appropriate delta-sigma ADC class for multiplexed applications performs the conversion task with a zero-cycle-latency characteristic. These delta-sigma ADCs usually have sinc (sinx/x) digital filters. This class of data converter masks internal-digital-filter results from a designer's view. With a zero-cycle-latency delta-sigma ADC, the first output-data results fully settle.

You can also describe a zero-cycle-latency ADC as having single-cycle settling or a single-cycle conversion. In all cases, however, you will get the right answer from the multiplexed ADC the first time.

13. When is good enough good enough?

If you are having difficulty making product-selection decisions in a consumer circuit, such as the temperature-sensor circuit in **Figure 1**, you can quickly solve this problem by choosing the absolute best performing parts for each socket. Is this statement true or false? Using this type of logic may give you a confident feeling that your circuit will work correctly the first time. However, following such logic goes only so far when you try to justify the cost-versus-performance factors of the products you are using.

In **Figure 1**, note that a 12-bit data converter is at the end of the signal chain. So, are the highest performance analog products in front of the analog-to-digital converter (ADC) appropriate? How do you determine which products are good enough for your system? Avoiding production-floor notifications or field failures may be your definition of "good enough."

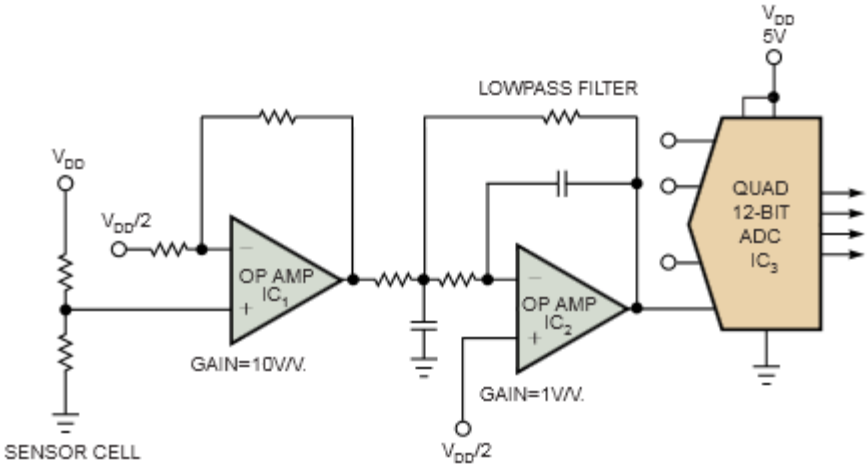

Figure 1. In this typical 12-bit temperature-sensing circuit for consumer applications, the gain of IC_1 is 10 V/V, and the gain of IC_2 is 1 V/V.

Instead of choosing the best products, you can use the root-sum-square (RSS) algebraic approach. One criterion is to keep the signal within the dynamic range of the full-scale range of the ADC. The product characteristics that influence the extent of the dynamic range are the system's cumulative offset and gain errors.

As an example, assume that the maximum offset error of IC_1 and IC_2 is 0.5 µV. The offset error of the ADC is ±1 LSB or ±1.22 µV. (The full-scale range of the ADC is 5V.) The gain error of both the sensor cell and the IC_1 amplifier configuration depends on the ±1% maximum resistor tolerances as well as on a maximum sensor-resistor tolerance of ±2%. The ADC's contributed gain error is 0.098% or equals 4.9 µV maximum at full scale.

To determine the dynamic-range limitations of the circuit, if you combine all of these terms, you would calculate the combined RSS value of offset and gain, bringing these errors to the ADC's input. With the RSS formula, you take the square root of the sum of the squares of several terms that are statistically independent. You cannot use an RSS formula with entities that have correlated variations that are not statistically independent.

For instance, the worst-case sensor-resistive offset error would be ±94 µV×10V/V. The contribution of the amplifier-gain stage, IC_1, is ±500 µV×10, the filter-stage (IC_2) offset error is ±500 µV, and the ADC (IC_3) offset error is ±1.22 µV. The cumulative possible offset error at the ADC's input is:

$$\sqrt{\left(sensor + IC_1^2 + IC_2^2 + IC_3^2\right)} = 940mV$$

This calculation illustrates that the sensor cell contributes the most error with little impact from the amplifiers or the ADC. Using the same logic, you would use the RSS formula to determine gain-error contribution that limits the dynamic range from the four stages in this circuit.

So, during your first consumer-product-selection attempt, you can use RSS calculations. These calculations can assist you in making logical and economical product decisions. Once you take this first step, make sure you use the same evaluation technique in your manufacturing process to quantify the effects of the processes–such as solder reflow–that you impose on these devices and the end-of-life effects due to environmental exposures.

Reference

1. Sandler, Steven M, A Comparison of Tolerance Analysis Methods, AEi Systems LLC, 1998.

14. Throw those bits away!

A high-quality load cell may have a 2-µV/V output-transfer function, meaning that for each volt of excitation you get ±2 µV of the full-scale output signal. With an excitation of 4.096 V and a full sensor deflection, the maximum output is ±8.192 µV. In a 12-bit application, half of full-scale might represent 0 to 250 lbs for a bathroom scale. If you want 0.25-lb resolution, you need 1000 points of measurement output. To look at something that is 1/1000th of the full-scale range, you must distinguish a change of 8.192 µV of the sensor output. You can achieve this distinction by keeping the peak-to-peak sensor noise less than 8.192 µV for 99.999% of the time, using a crest factor of 4.4 (*reference 1*). With this definition, the least-significant bit at the sensor is 8.192 µV, or 931 nV rms.

The load-cell bridge has an excitation voltage of 4.096 V (**Figure 1**). The INA326 instrumentation amplifier follows the load cell with a gain of 250 V/V. The system's full-scale voltage, 250×±8.192 µV, produces a ±2.048 V full-scale signal. The 12-bit ADS7822 digitizes the analog signal.

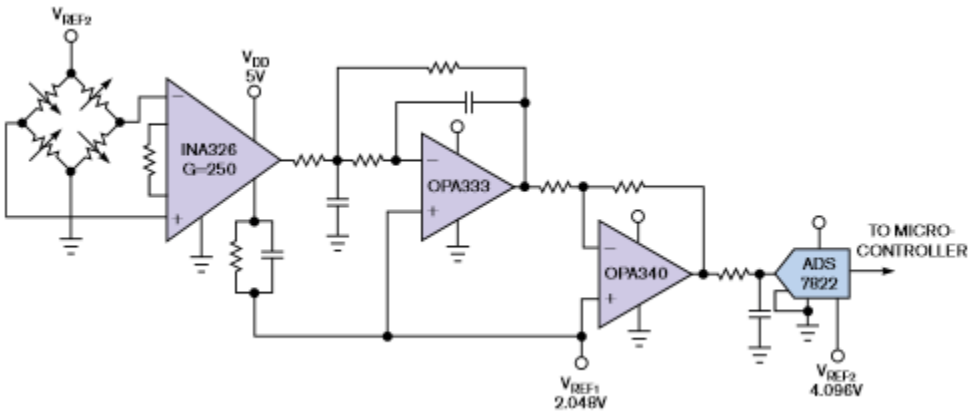

Figure 1. A 12-bit load-cell system achieves accuracy to 0.25 lb.

This 12-bit analog-to-digital converter (ADC) system must have an analog filter. The lowpass OPA333 analog filter's primary function is to remove the high-frequency signal components at the input of the ADC (*reference 2*). Because the load cell in the circuit operates near DC, you limit the bandwidth to 10 Hz. The components in **Figure 1** cost less than $6.

Now, look at load-cell measurement with a 24-bit system. You can simply put the load-cell signal through a first-order lowpass filter and into the delta-sigma ADC (**Figure 2**). The first-order filter in this circuit eliminates high-frequency noise around the ADC's sampling frequency (*reference 3*). The sensor provides the resistor for the filter RC pair.

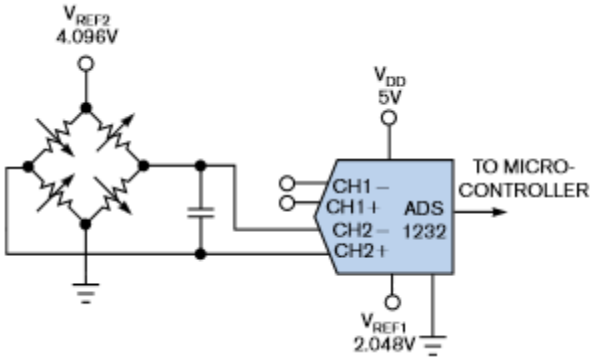

Figure 2. A 24-bit load-cell system has greater-than-0.25-lb accuracy.

Look at the errors for the 24-bit delta-sigma ADC system in **Figure 2**. The ADS1232 produces 3.7 µV p-p of noise, with a crest factor of 4.4. This figure is much lower than the sensor's least-significant bit. Additionally, the full-scale range of the ADC is 4.096 V, whereas the sensor's full-scale output range is ±8.192 µV. As you can guess, you will “throw away” most of the output bits of the delta-sigma ADC. The components in **Figure 2** cost less than $4.

You may find that the 12-bit data converter system ends up costing you more money, real estate, and headaches than the alternative 24-bit system.

References

1. Baker, Bonnie, RMS and peak-to-peak noise trade-off, *EDN*, May 15, 2008.
2. Baker, Bonnie, What's in your SAR-ADC application? *EDN*, Dec 15, 2008.
3. Baker, Bonnie, Analog filter eases delta-sigma-converter design, *EDN*, June 12, 2008.
4. Download datasheets from these product folders: INA326, ADS7822, OPA333, ADS1232.

15. Take a risk; throw away those bits!

When designing an analog-to-digital converter (ADC), your initial approach may be to define the required resolution and select a device that matches your needs. To get the required system precision, you add the necessary analog gain modules and level shifts so that the signal of interest covers the entire full-scale input range of the ADC. As a first step in your design process, you often look at the source's output range. For example, a typical pressure sensor's output full-scale range is in the hundreds of millivolts. You then match the sensor's output range to the ADC's input by inserting an analog gain cell and level-shift circuitry to match the ranges of the sensor/ADC combination.

Suppose that you change your strategy and stop playing it safe. You can create a 12-bit system using a 24-bit ADC and eliminate the need for analog gain and level-shifting circuits. For instance, a true 24-bit ADC is like having 4096 12-bit ADCs across the output range of the ADC. This academic discussion is interesting, but, in reality, you will probably never find a noiseless 24-bit ADC. **Figure 1** shows the relationship between output codes and noisy bits of a realistic 24-bit delta-sigma ADC. The ADC accepts a differential input signal and has an effective resolution of 19.5 bits rms.

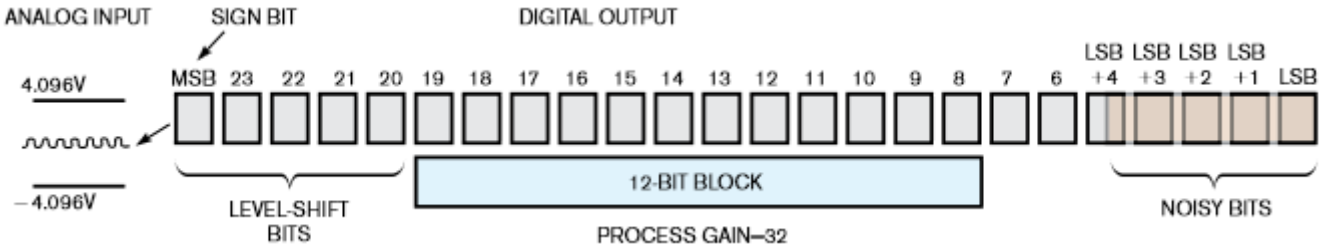

Figure 1. Use delta-sigma ADCs to implement process gain and level-shifting on an analog signal.

You can use the 24 bits of the delta-sigma ADC to substitute the analog functions of gain and level shift into this digital engine. Then, implement an increase in the delta-sigma ADC's process gain by shifting the 12-bit window to the right or toward the data converter's least-significant bit (LSB). Each 1-bit shift to the right is equivalent to doubling the process gain. As in the analog domain, an increase in process gain lessens the input range. In **Figure 1**, the output coding scheme of the delta-sigma ADC is binary two's complement.

This approach also allows you to use the delta-sigma ADC to sense the analog level shift of the circuit. When you ignore a few most-significant bits (MSBs), you actually allow a level shift of the input signal. A process gain of one has a bipolar full-scale analog input range of ±4.096 V, or 8.192 V p-p. A process gain of 32 changes the analog input range to 256 µV, or 8.192 V/32. The value of MSB, MSB-1, MSB-2, MSB-3, and MSB-4 represents the system's average voltage level shift. To sweeten the pot, many 24-bit delta-sigma ADCs have on-chip programmable-gain amplifiers (PGAs). With delta-sigma ADC devices that have on-chip PGAs, you can increase the process gain by another product-specific factor of 64 to 128.

Although the total range of the 24-bit ADC is operational, your sensor might cover only a portion of the ADC's input range and output codes. Some designers dislike throwing away bits, emphatically claiming that they paid money for those bits and so they will use them.

On the other hand, you have the full resolution of 2^{24} codes at your disposal, and you can stand to lose some dynamic range because the goal is to acquire only 12 bits for your measurement. Think about the analog circuitry you have eliminated. By selecting that portion of the ADC range, you can focus on just the area of the signal response. Don't look back. Enjoy throwing away those bits and do so with great pleasure.

About the author

Bonnie Baker is a Senior Applications Engineer with the WEBENCH® team at Texas Instruments and has been involved with analog and digital designs and systems for over 30 years. In addition to her fascination with circuit design, Bonnie has a drive to share her knowledge and experience. She has written hundreds of design and application notes, conference papers, and articles, including a monthly column in *EDN* magazine called "Baker's Best." She has compiled an ebook based on the amplifier articles in the Baker's Best column: Best of Baker's Best – Amplifiers. Additionally, Bonnie has authored a book: "*A Baker's Dozen: Real Analog Solutions for Digital Designers*." Check out her blog series, On Board with Bonnie, where she navigates the ins and outs of signal chain designs. You can reach Bonnie at ti_bonniebaker@list.ti.com.

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