Low-cost, linear A/D conversion uses single-slope techniques

Improvements in components and circuit design have brought back the single-slope converter as a viable performer. Here's how it's done.

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The increasing popularity of voltage-to-frequency (V/F) converters and digital voltmeters using single-slope A/D conversion highlights the return of this low-cost technique to the circuit board. Some early DVM's and data converters used single-slope conversion, but the advent of the dual-slope integrator, with its inherent error-cancellation characteristics, relegated single-slope techniques to a minor role.

Now, however, the single-slope converter is back. Its weaknesses remain the same, but improvements in components and circuit design have achieved significant performance benefits at low cost.

Basic design uses V/F technique

All single-slope converters are basically voltage- or current-to-time converters. A voltage-to-frequency scheme, shown in **Fig 1**, furnishes a model.

Amplifier A_1 integrates the input voltage until its output has the same absolute value as the reference voltage. At this point, A_2, acting as a comparator, trips and causes the one-shot to close the switch across the integrating capacitor. The length of time required to trip the comparator is directly proportional to the input voltage.

Fig 2 shows a more practical incarnation of the same concepts. Here, the comparator and one-shot have been replaced by a unijunction transistor, whose intrinsic standoff ratio and the 1N821 form a reference that determines the reset point of the 301A integrator. That device's output ramps negative until the UJT switches, producing a large imbalance at the integrator's inputs and thus driving the output positive at a high slew rate. Because of the UJT's negative resistance characteristic, the amplifier moves its output all the way to zero before the UJT reverts to its high-resistance state. The positive edge of the 301A output is differentiated by the 2.2k/500 pF network and then level-shifted by the transistor to provide a logic-compatible pulse.

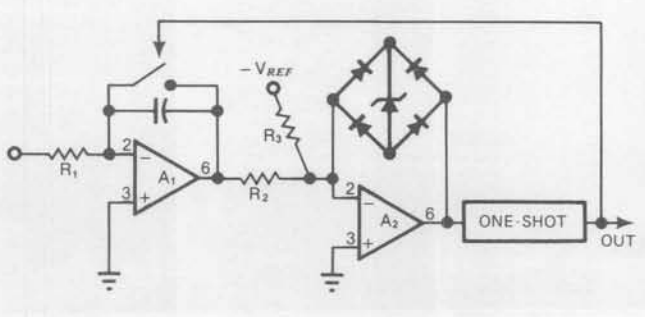


Fig 1—Simple voltage-to-frequency converter *demonstrates the basic single-slope conversion technique.*

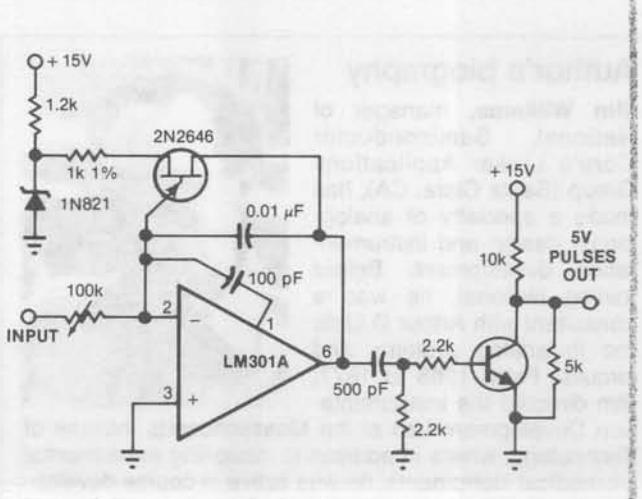


Fig 2—Single-slope conversion *can suffer from nonlinearity arising from the capacitor's reset time.*

Nonlinearity errors can be overcome, but at the cost of circuit simplicity

Nonlinearity comes from several sources

A 100 pF feed-forward capacitor between the inverting input (pin 2) and the balance/compensation input (pin 1) increases the slew rate of the 301A; however, capacitor reset requires 900 nsec. At 1 kHz, this figure represents about 0.1% dead time and produces a nonlinearity error. At 10 kHz FS, the nonlinearity arising from this effect would reach 10 Hz.

There are some other architectural weaknesses in this particular circuit, including the gain error that arises from any change in the integrating capacitor's value. Drifts in the UJT can also introduce errors. You can overcome any and all of these problems by trading off circuit simplicity.

Another way to do it

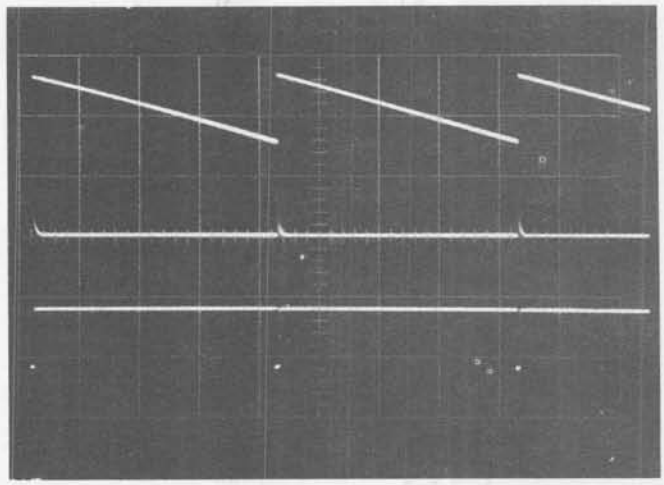
Charge dispensing, the method used in most industrial V/F converters, was first applied by R A Pease. **Fig 3** gives an example.

The output state of the amplifier switches C_1 between a reference voltage provided by the diode bridge and its inverting input. R_1 limits the current through the zener to its specified zero-TC value. Output pulse width is unimportant so long as it permits complete discharge and charge of the capacitor. The network formed by R_2 and C_2 reinforces the direction of the output's movement. Any negative-going output is followed by a positive edge after a time governed by the R_2C_2 time constant.

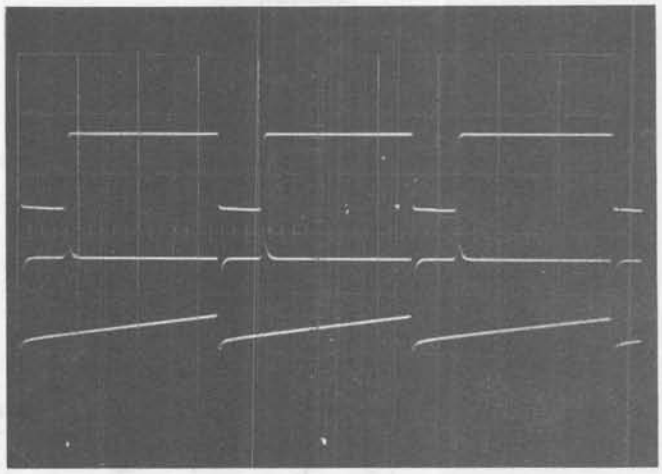
The actual integration capacitor in the circuit, C_3, never charges beyond 10 to 15 mV because it is constantly being reset by charge dispensed from switching C_1. Whenever the amplifier's output goes negative, C_1 dumps a quantity of charge into C_3, forcing it to a lower potential. A negative-going output causes the transfer of a short pulse through C_3 to the noninverting input. When this negative pulse decays out and the noninverting input is at a higher potential than the inverting input, C_1 can receive a charge and the cycle repeats. The diodes in C_1's path compensate for the diodes in the bridge.

Preventing lock-up

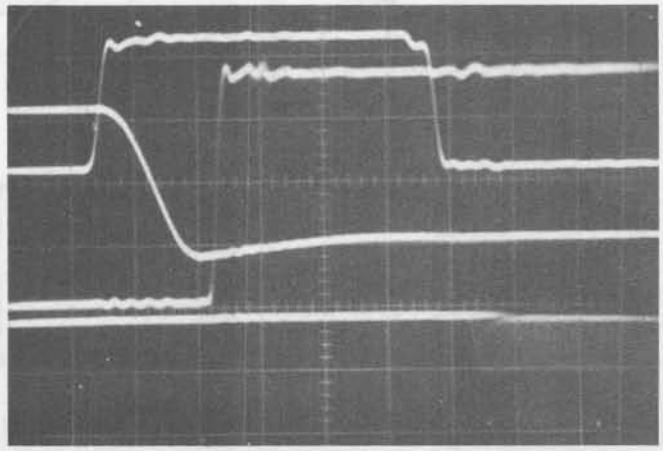
The circuit must deal with several lock-up conditions; any condition that allows C_3 to charge beyond 10 to 20 mV causes the amplifier to go to the negative rail and stay there. The 2N2907A transistor prevents such an occurrence by pulling the inverting input toward −15V. The RC network in the base circuit (33k and 10 μF) then determines at what point the transistor will come ON. When the circuit is running normally, the transistor is biased OFF and effectively remains out of the circuit. The 50k potentiometer trims



The V/F converter scheme *illustrated in* ***Fig 2*** *produces these waveforms. The top trace is the integrator's output, the middle one the diffentiated output and the bottom one the output pulse.*



Improved linearity *results with the use of charge-dispensing techniques. The top trace shows the amplifier output for* ***Fig 3,*** *while the middle and bottom traces represent the noninverting and inverting inputs, respectively.*



Blazing speed *is the strong point of the ultra-high-speed A/D converter shown in* ***Fig 4.*** *Horizontal scale here equals 30 nsec/div. The top trace shows the ramp resetting, the second trace is the convert command, the third is the comparator output and the bottom is data out.*

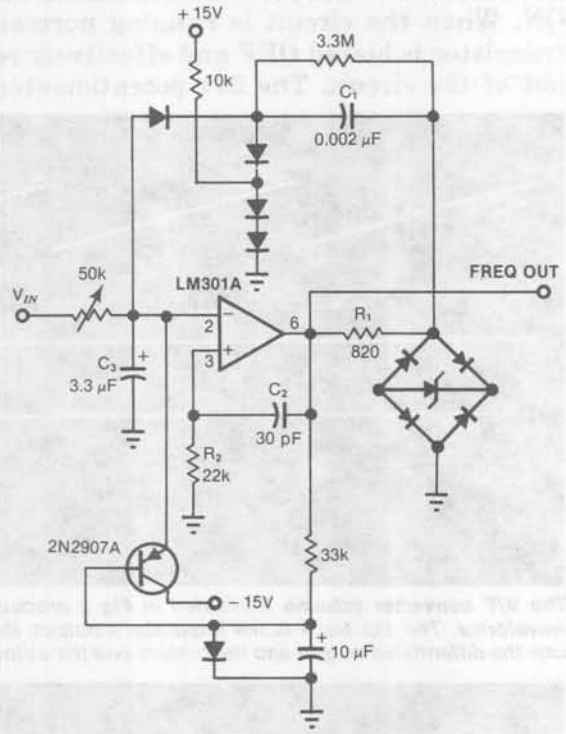


Fig 3—Charge-dispensing techniques *provide better linearity but require slightly more complex circuitry.*

the full-scale output, while the amplifier's offset limits zero frequency. This offset can be trimmed at the amplifier trim terminals or by summing a current of the appropriate polarity to the inverting input.

With proper selection of C_1, this circuit can deliver 0 to 10 kHz output with 0.01% linearity for a 0 to 10V input. Slight nonlinearity does still exist and manifests itself as a bow in the response over the total dynamic range. Normally this factor would limit linearity to about 0.05%, but the 3.3M resistor across the 0.002 μF capacitor corrects for the effect by altering the capacitor's charge characteristic. The slew rate and bandwidth limitations in the amplifier, and the difficulty of resetting the integrator, are the stumbling blocks for high-speed operation with single-slope converters. The solution is achievable, however, and in an economical (about $20 worth of parts) fashion.

Picking the players for performance

A low cost, high speed, single-slope 10-bit A/D converter appears in Fig 4. The discrete-component current source is the secret here. A 1N827 temperature-compensated zener diode, dual transistor and two film resistors constitute the reference-current source. One-half of the transistor provides temperature compensation

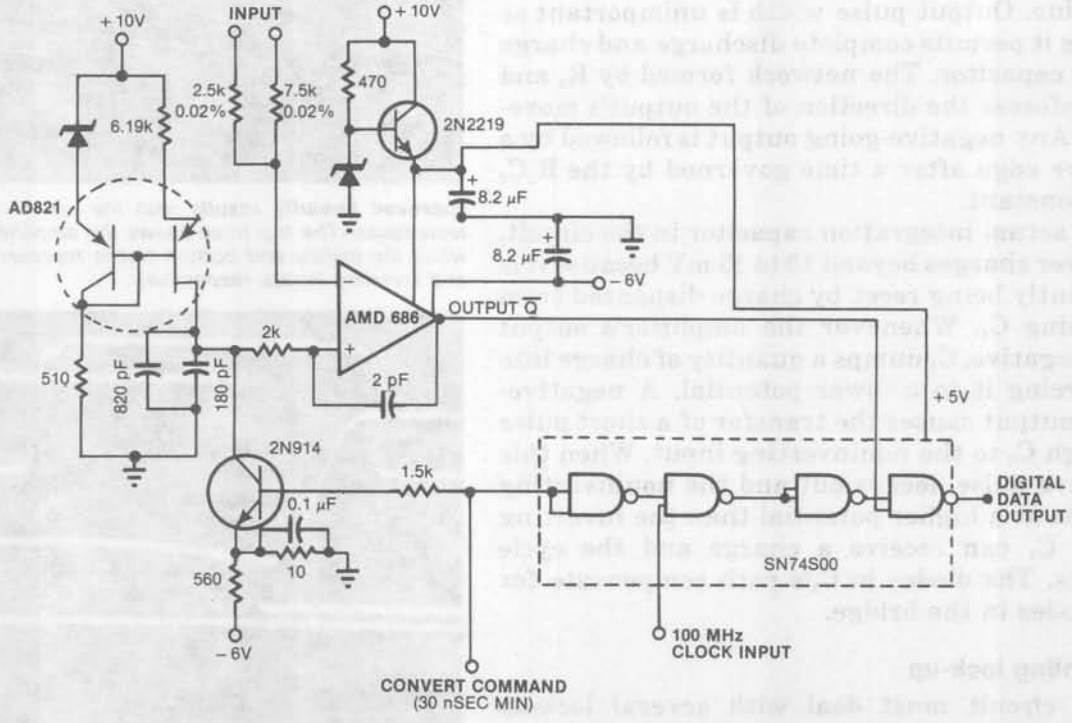


Fig 4—A discrete-component current source *allows high-speed operation with full 10-bit accuracy.*

Slew-rate and bandwidth limitations are the bars to high-speed operation

for the current-pump half, and the 510Ω film resistor ensures that the zener receives its zero-TC current—7.5 mA. The 6.19k resistor determines the magnitude of the current delivered by the current pump. Although the transistor halves run at different current densities (7.5 and 1 mA), the circuit achieves adequate temperature compensation.

The 1000 pF capacitor comprises polystyrene and silver-mica units in a ratio that cancels the temperature drifts of the individual units. In addition, the dielectrics selected have excellent aging characteristics and very low soakage (dielectric absorption). This parallel-capacitor approach has been used successfully by manufacturers, and the resulting temperature and time drifts are well documented. At least one manufacturer provides a dual-electric capacitor.

The current source provides a ground-referenced output that allows easy reset of the capacitor. Operational-amplifier-based current sources do not allow the fast integration (10-μsec) and reset (30-nsec) times without extravagant compensation techniques. Finally, note that the current source runs at all times—even when the capacitor is being reset to zero, thus eliminating errors caused by switching the current on and off.

Each time a pulse is applied to the convert-command input, the 2N914 resets the 1000 pF capacitor to 0V. This resetting action takes 30 nsec—the minimum acceptable convert-command pulse width. On the falling edge of the convert-command pulse, the capacitor begins to charge linearly; in precisely 10 μsec, it charges to 2.5V. Normally, the 2N914 would not be able to reset the capacitor to 0V because of its V_{CE} saturation voltage, but returning the 2N914 emitter to −0.1V compensates for this effect. The 560Ω resistor is selected from standard 1/4W values to give the right voltage at the 2N914's emitter to enable a reset within 1 mV (much less than 1 LSB) of ground.

The 10-μsec ramp is applied to the AMD 686 "+" input and compared with the unknown at its "−" input. For a 0 to 2.5V range, the input is applied to the 2.5k resistor. For a 0 to 10V input range, the 2.5k resistor is grounded and the input applied to the 7.5k resistor. Under both conditions, source impedance is the same. The 2.0k resistor at the "+" input provides balanced source impedance, and the 2N2219 emitter follower drops the +10V supply to +5V to run the comparator. The 686 outputs a pulse whose width is directly dependent on the value of the input; this pulse width is then used to gate a 100 MHz clock. The 74S00 gate achieves this function and also gates out the portion of the 686 output caused by the convert-command pulse. Thus, the 100 MHz clock-pulse bursts that appear at the output are proportional to the input. For a 0 to 10V input, 1024 pulses appear at full scale, 512 at 5V, etc. **EDN**

References

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Author's biography

Jim Williams is a consultant at Arthur D Little Inc, Cambridge, MA. Previously he was a senior engineer at MIT's Dept of Nutrition and Food Science, where he designed experimental biomedical instrumentation. Jim enjoys a variety of outside activities, including sculpture, travel, art, skiing, tennis, and collecting antique scientific instruments.