RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Slow "starting" ADCs (or the beneficial effects of in diagnosing converter problems)

Q. To save power, my ADC is powered up only to make a measurement. The system is very accurate in continuous operation, but completely unpredictable when power is strobed.

A. As a by product of the securityobsessed Soviet system. Russians can be very reluctant to provide all the details of an applications problem. Alexei, whom I met at a seminar in Novosibirsk in Siberia, was no exception. He complained that his ADC (analog-to-digital converter) was badly out of specification and sometimes did not work at all.



by the system. Such problems rarely occur in converters with "sleep" circuitry where the supply is still present but the device is switched to a low consumption standby mode for power saving. Logic is not the only possible cause of

start-up errors in converters. Thermal stabilization, capacitance charging, and slow starting of regenerative current mirrors can all degrade reference accuracy for many milliseconds after power-up.

Alexei programmed some dummy conversions and I boarded the Trans-Siberian Express for Vladivostok leaving a working system, and a happy, if over fed, engineer behind me

Furthermore, not only the data output is affected. The EOC (end of conversion) or "busy" output may also be confused—if this output is used to initiate the next conversion, the system may not self-start on power-up. If such latch-up always occurs, the problem will be recognized during system design, but if it only occurs occasionally (as with the original ADC84 in the 1970s) the problem can be

but was reluctant to provide details of his sys-

tem. So I provided some vodka, caviar and bli-

nis, and we toasted Mother Russia, Catherine

analog engineers everywhere. He loosened up

the Great, the Trans-Siberian Express, and

and revealed that he was only powering his

and then shutting it down again.

ADC for just long enough to do a conversion

Microprocessors reset with each start, but

few ADCs do, so after power-up their logic is

randomized. The first conversion (or in some

pipelined converters the one when the initial

data exits the pipeline) resets the logic, but

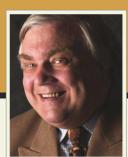
the first results may be totally wrong.

overlooked—with dire results.

Data converters should perform one or more "dummy" conversions after power-up before the conversion results are actually used. During these "dummy" conversions the output data, and anomalous behavior of EOC or other logic outputs, should be ignored

To learn more about behavioral problems in ADCs & how to avoid them Go to:

http://rbi.ims.ca/4394-504



Contributing Writer James Bryant has been a European **Applications Manager** with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

SPONSORED BY

