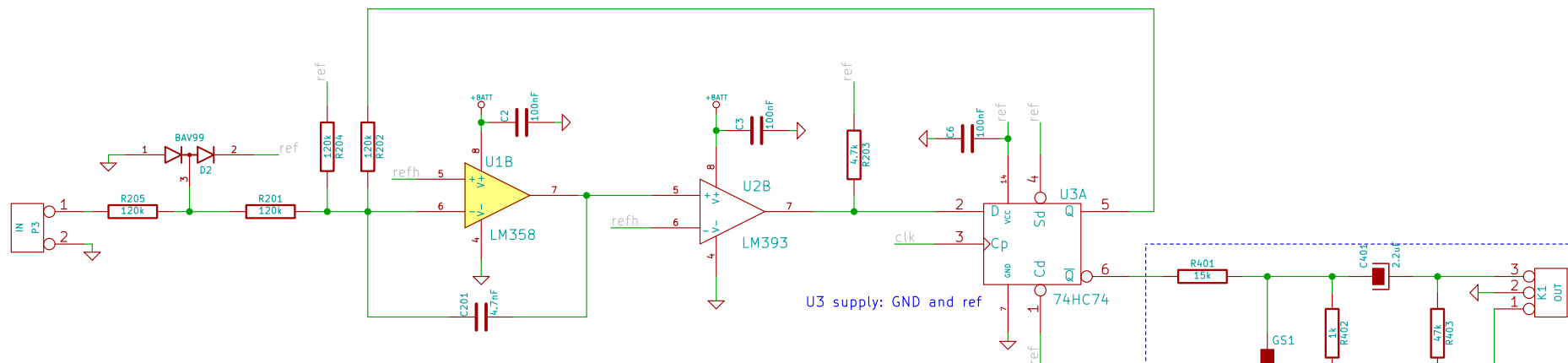
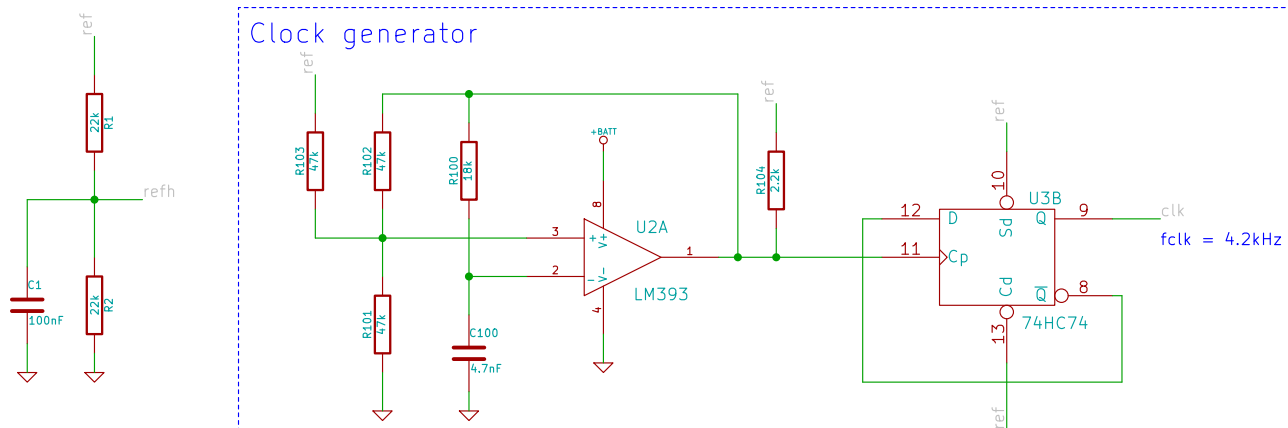


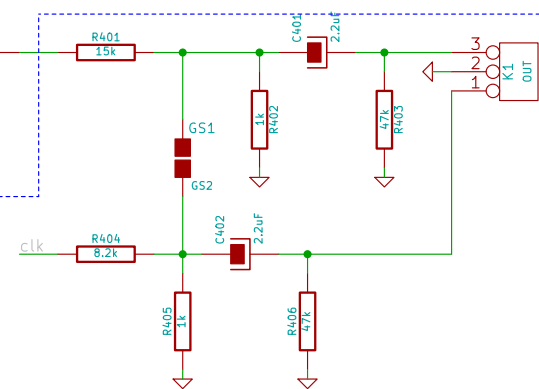
Delta sigma circuit



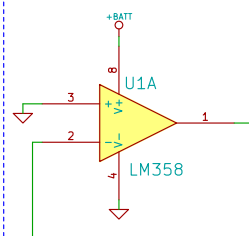
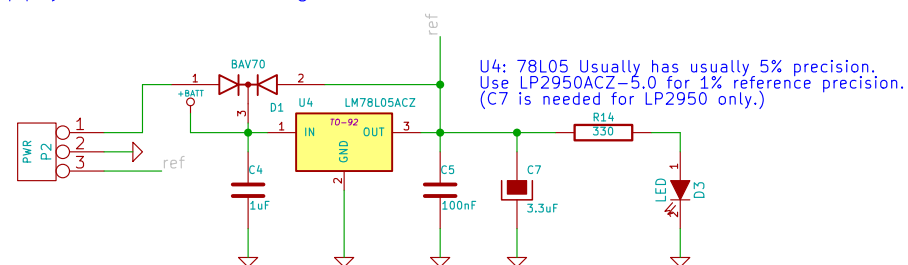
Clock generator



Output signal level matching



Supply and reference generation



ref 5V
refh ... half reference voltage (2.5V)

Close GS1 to mix clock and data onto a single channel.
This is needed for the SocDVM software.

Adjust R205 and R201 for desired input voltage range:
 $|V_{in_max}| = 2V \cdot (R201 + R205) / R202$

U3 *must* be a HC type!

File: sdadc2.sch

Sheet: /

Title:

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Date: 27 sep 2013

Rev:

KiCad E.D.A.

Id: 1/1