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High-Voltage Signal Conditioning for Low-Voltage ADCs

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ABSTRACT

Analog designers are frequently required to develop circuits that convert high-voltage signals to levels acceptable for low-voltage data converters. This paper describes several solutions for this common task using modern amplifiers and typical power supplies. Five examples of conditioning ±10V bipolar signals for low-voltage, single-rail analog-to-digital converters (ADCs) are presented: a modular approach, a single-supply/single-part approach, and an instrumentation amplifier approach. Both single-ended, differential input versions are discussed.

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Introduction

Analog front-end designers are often confronted with the challenge of coupling high-voltage bipolar signals to ADCs that operate on low-voltage single supplies. Traditional single-part, high-voltage converters are becoming obsolete, although many applications continue to use high-voltage bipolar analog signals. Modern data converters are designed on small geometry processes because of advanced digital capabilities, higher yields, and overall lower costs. Op amps, on the other hand, are designed on large geometry processes to withstand higher internal voltages and allow precise control of internal elements. Modern op amps offer several outstanding features, such as rail-to-rail I/O, a wide input common-mode voltage range, linear transfer functions, low power consumption and low-voltage operation. By using discrete op amps and data converters, designers can optimize circuit performance by using the proper part and avoiding expensive, compromised, single-part solutions.

1 Circuit 1: The Modular Approach

The circuit shown in Figure 1 is a classic modular approach to circuit design. The first stage is attenuation. The second stage is level-shifting. This style is convenient because designers can compartmentalize adjustments. Input range can be adjusted by changing R1. Level-shift can be changed by adjusting REF1V50. These parameters are independent and can be tuned with minimal interactions. Furthermore, designers may want to include anti-alias filtering or other analog functions. These blocks can be neatly inserted at node N_2.

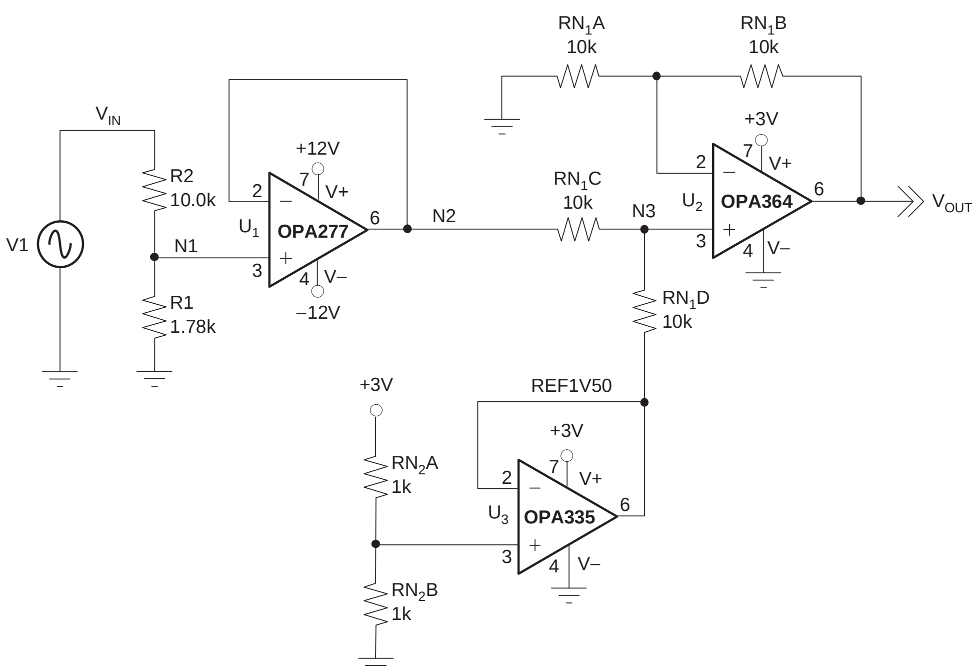

Figure 1. Circuit 1: Modular Design

On the front-end voltage divider, the equation for R1 is:

$$\frac{R1}{R2} = \frac{V_{OUT}}{(V_{IN} - V_{OUT})} \tag{1}$$

In Circuit 1, the following values are used:

$V_{OUT} = 3V$

$V_{IN} = 20(\pm10)V \quad = V_1$

$R1 = 1.76k$ (1.78k is closest standard value)

$R2 = 10k$

REF1V50 = midpoint of ADC full-scale input range.

These component values can be altered to account for different input ranges or input impedance requirements. In this example, the value of R2 is held constant to simplify calculations and reduce trimming to one element.

The first stage op amp is an OPA277. The OPA277 was chosen for its low V_{IO}, low drift, and bipolar swing. This stage needs to have bipolar swing about ground because the input signal is bipolar. The OPA277 is also a great candidate for active-filter stages. TI’s free FilterPro design tool (available for download at www.ti.com) can be used to design and model active filters. FilterPro presumes that the amplifiers under consideration are operating in a bipolar mode, making node N1 the appropriate place for filters. Another option for the first stage is the OPA725, which is suitable for bipolar stages with ±5V rails.

The second stage op amp is the OPA364. This outstanding, low-voltage op amp offers many assets which are ideal at this stage: it is low-voltage and low-power, in addition to having a large input common-mode voltage range. It also has zero crossover distortion for linear, monotonic, large-signal output.

Resistor networks are used to bias the OPA364 and the reference because they are matched. This ratiometric design takes advantage of this property. Gain errors from mismatched components cannot be distinguished from genuine signals. For example, the gain error from discrete 1% components is equivalent to −40dB of erroneous signal. This is inadequate for 12-bit, or higher, conversions, where the minimum detectable signal is below −70dB. Resistor networks with ratio 0.01% tolerances (−80dB) are readily available. High-quality metal foil networks with 0.005% tolerances (−106dB) may be necessary for extreme cases.

The DC sweep plot of Circuit 1 is shown in Figure 2. Node N3 shows the input common-mode voltage swing of the second stage.

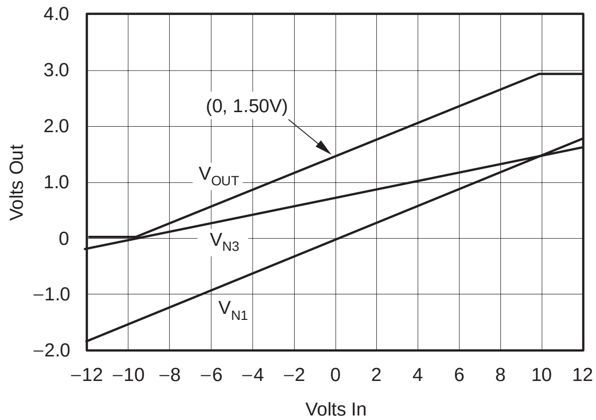

Figure 2. DC Sweep of Circuit 1

Designers may want to consider the INA132 or the INA152 for the second stage. These amps are considerably slower than the OPA364, but they come with precision-matched internal resistors to reduce gain errors. In general, DC precision is desirable for open-loop applications such as temperature sensors or calibrated transducers, where absolute accuracy, offset and drift are critical. This precision makes the INA132 a good choice for absolute measurements. In closed-loop applications such as servos loops or PID controllers, high-speed and monotonicity are desirable. In closed-loop systems, DC offsets and gain errors will be canceled by feedback and calibration. This makes the OPA364, or the OPA301, good choices for servos and feedback signals.

2 Circuit 2: Single-Supply/Single-Part Approach

Figure 3 shows a circuit that is attractive to designers who are limited to a single low-voltage supply. The proper selection of biasing components enables both the attenuation and level-shifting functions to be accomplished in one stage.

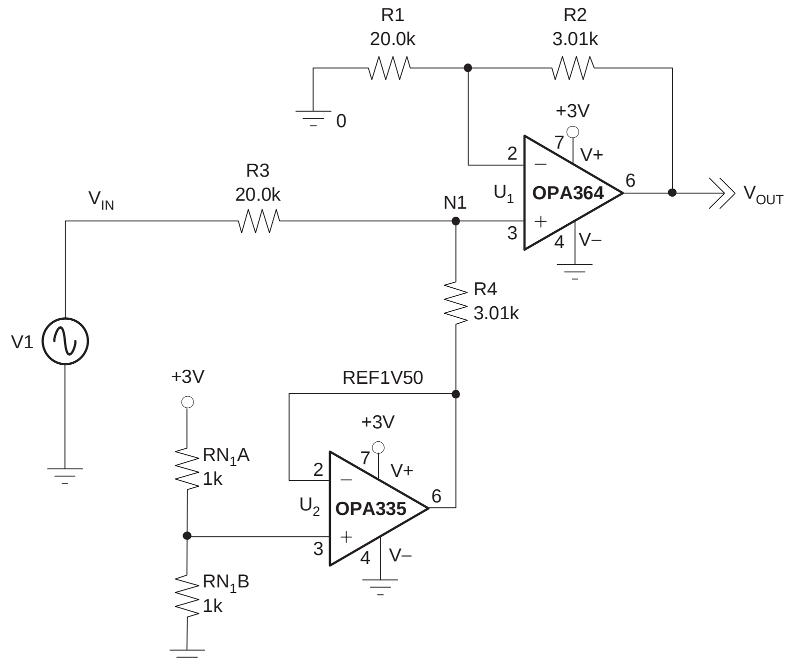

Figure 3. Circuit 2: Single-Supply/Single-Part

The following series of formulas defines the relationship of the bias components:

$$R1 = R3$$

$$R2 = R4$$

$$\frac{R1}{R2} = \frac{V_{IN}}{V_{OUT}}$$

Circuit 2 uses the following values:

$$V_{OUT} = 3$$

$$V_{IN} = 20(\pm 10) \quad = V_1$$

$$R1 = R3 = 20.0k\ 1\%$$

$$R2 = R4 = 3.01k\ 1\%$$

REF1V50= midpoint of ADC full-scale input range

This architecture is much more compact than the modular solution of Circuit 1; however, it does rely on tight component tolerances, and does not offer either simple adjustment or filter insertion options. The DC sweep plot of Circuit 2 is shown in Figure 4. Note the large common-mode voltage swing at node N1 and the rail-to-rail output range. These two requirements make the OPA364 the best choice. Also, note the output clamping action of the OPA364, which ensures that the ADC output is not overdriven. This design can be used with input voltages far outside the power-supply rails, though designers need to pay attention to the power dissipated in R1 and the input common-mode voltage limitations of the op amp.

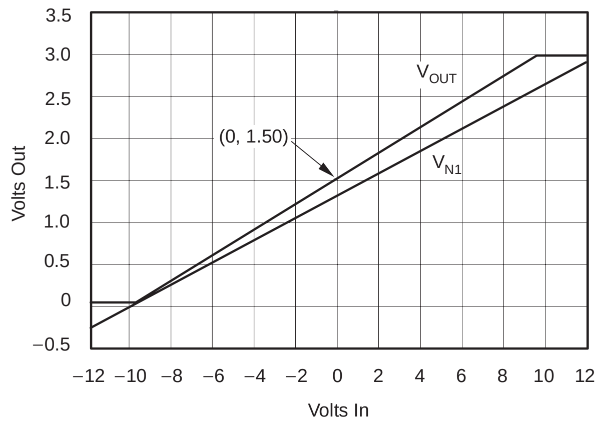

Figure 4. DC Sweep of Circuit 2

3 Circuit 3: Instrumentation Amp Approach

Figure 5 shows a circuit designed with the INA137. This part has built-in biasing components that can be configured for attenuation. Additionally, it has a pin for injecting REF1V50 for the level-shift function. The INA137 is a complete solution in one part, and offers additional features such as high common-mode rejection and easy adaptation to differential inputs. Components R1 and R2 are used to scale the input range. By itself, the INA137 can be configured for an attenuation of one-half. In this case, we need a slightly different ratio for our ±10V input range; thus, the additional components R1 and R2 are included.

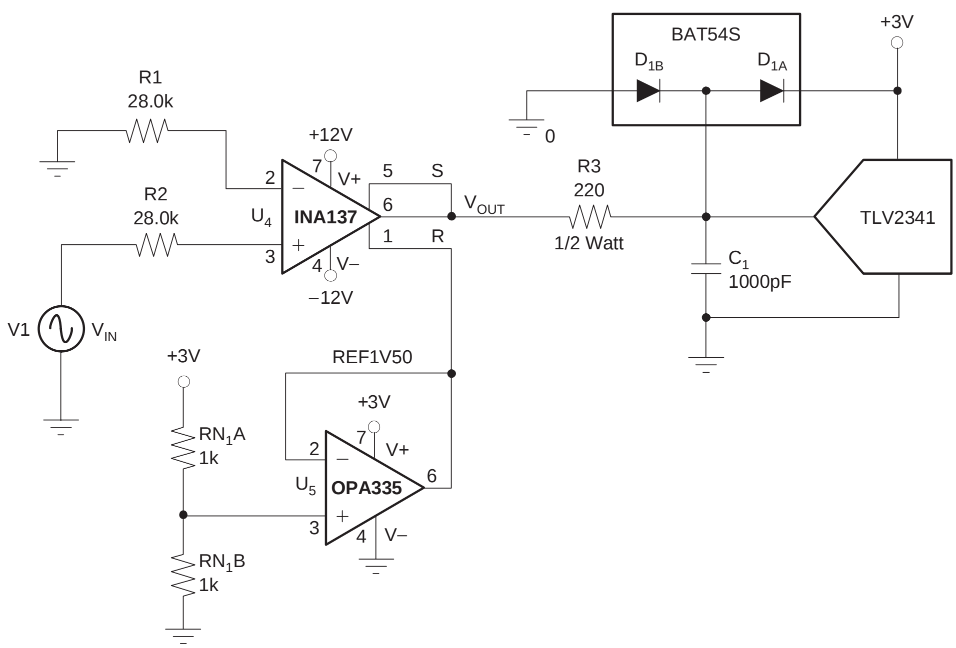

Figure 5. Circuit 3: INA137

The following equation relates the bias components:

$$R1 = R2 = \frac{(6k \cdot V_{IN} - 12k \cdot V_{OUT})}{V_{OUT}}$$

Circuit 3 uses the following values:

$V_{OUT} = 3V$

$V_{IN} = 20(\pm10)V = V_1$

$R1 = R2 = 28.0k$

The greatest advantage of an instrumentation amp design is excellent common-mode rejection. This circuit would also benefit from the use of resistor networks for R1 and R2 because of the close matching. If R1 and R2 are tightly matched, the circuit is balanced and maintains a high CMRR. Figure 6 shows the DC sweep of Circuit 3.

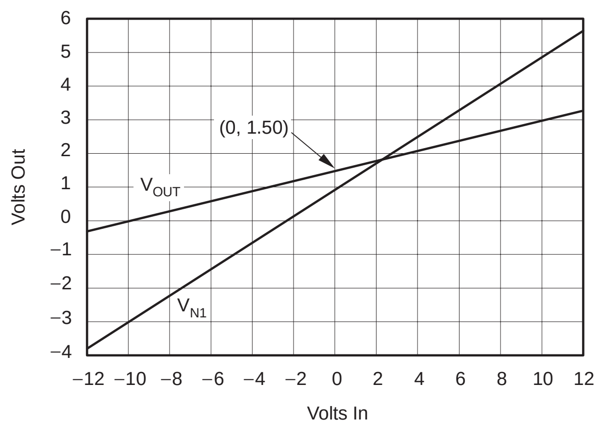

Figure 6. DC Sweep of Circuit 3

Circuit 3 shows the INA137 connected to a TLV2341 (see Figure 5). In this application, the INA137 can potentially swing outside the rails of the TLV2341. This excess swing could happen if there is an imbalance between R1 and R2 or a cabling error. To prevent overstress on the TLV2341 input, a dual clamping diode D_1 was added. Furthermore, a current-limiting resistor R3 was added to prevent the INA137 from exceeding the maximum drive current in this failure mode.

The designer must now carefully balance the relationship between the current limiting resistor R3, C_1 and the input capacitance of the converter. Too much resistance will dampen the transient response of the converter; however, too little resistance will overdrive the INA137. The values shown are reasonable starting points. Also, notice how these complications are avoided by using the low-voltage second stage that is presented in the first example (see Figure 1).

4 Circuit 4: Differential Input with INA137

Some systems have differential inputs. This is a popular technique to reduce common-mode noise. Audio engineers have used low-level, balanced, differential signals in harsh on-stage environments for decades. The INA137 is designed for these applications. Figure 7 shows Circuit 3 adapted for differential input.

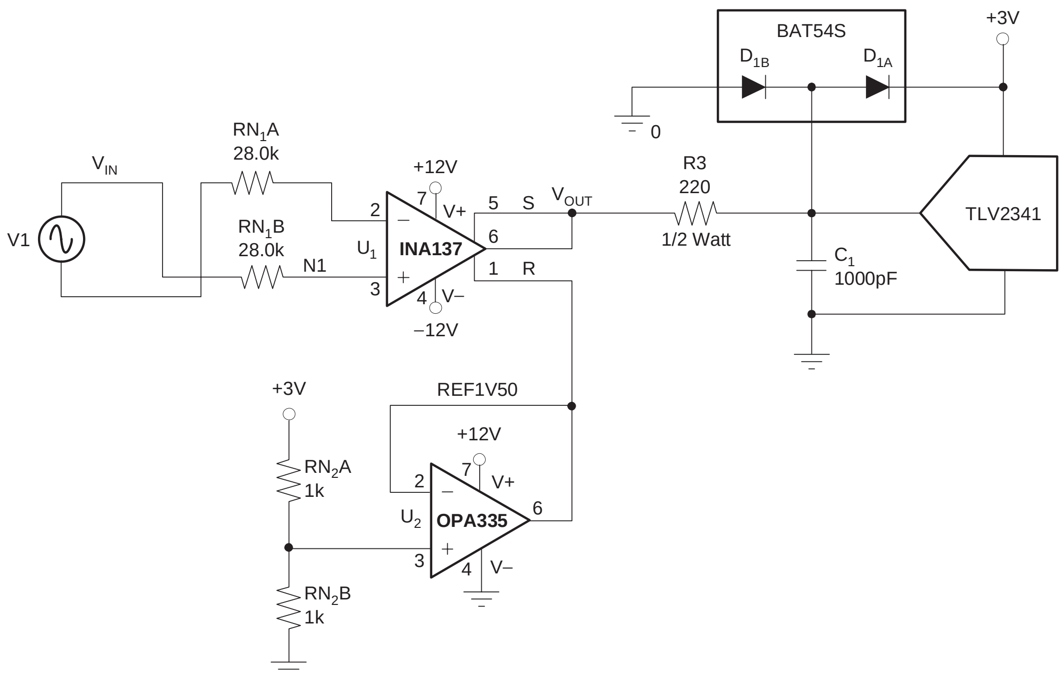

Figure 7. Circuit 4 (Circuit 3 with Differential Input)

Changing Circuit 3 from single-ended to differential is straightforward. Note the polarity reversal of the inputs, however. Figure 8 shows the DC sweep of Circuit 4.

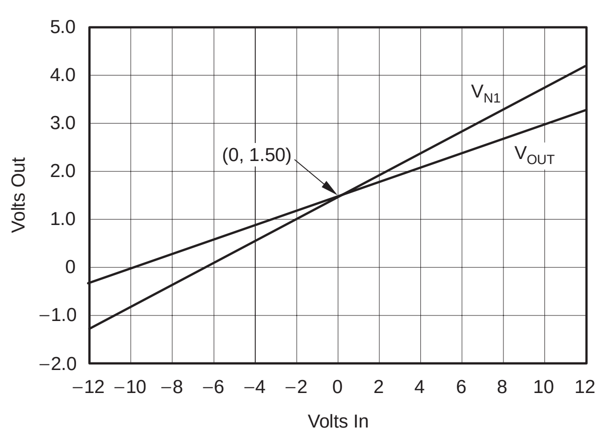

Figure 8. DC Sweep of Circuit 4

5 Circuit 5: Differential Input Modular

Circuit 1 can also be adapted for differential input. The changes require more effort, though; additionally, the attenuation stages are inverting, and the overall circuit looks more like a classic differential audio input. Note the use of matched components in this circuit. Figure 10 shows the DC sweep of Circuit 5.

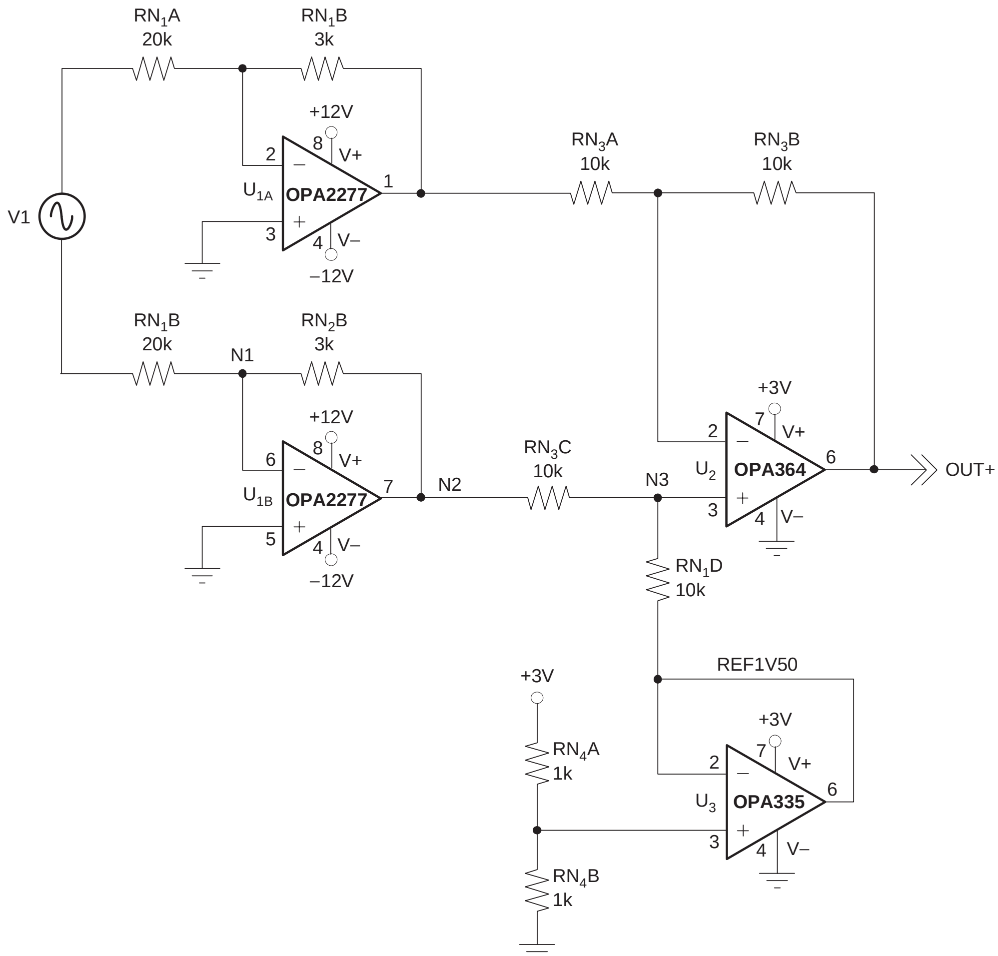

Figure 9. Circuit 5 (Circuit 1 with Differential Input)

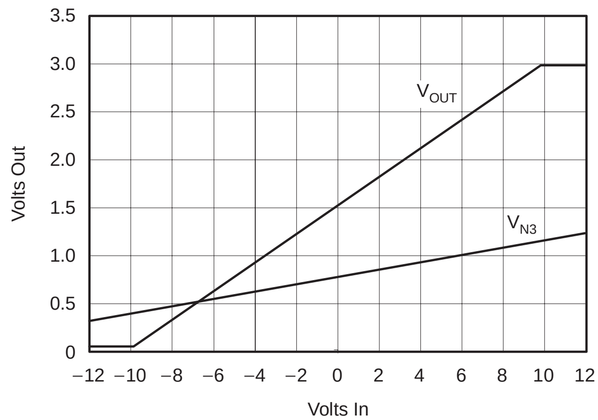

Figure 10. DC Sweep of Circuit 5

6 Voltage References and Ranges

The references shown in these examples are simple. They are for ratiometric applications where the ADC range is the rail. The references shown are $V_{CC}/2$, or at the mid-scale of the ADC range. This proportion is required for these circuits. 3.3V or 5V can be used in any of these designs; the references would be 1.65V or 2.5V, respectively. These designs will work with absolute references as well, as long as the V_{REF} is one-half of the ADC full-scale range.

The other requirement is a good buffer driving the reference signal. These designs put a wide range of loads on the reference, and a buffer is essential. For in-depth information on buffering references for precision and high-resolution designs, please see Application Note SBVA002, *Voltage Reference Filters.*

References

Bishop, J., B. Trump, and R.M. Stitt. MFB Low-Pass Filter Design Program. Application note. (SBFA001)

Stitt, R.M. Voltage Reference Filters. Application note. (SBVA002)

FilterPro™ MFB and Sallen-Key Design Program. Executable program. (SLVC003.zip)

To obtain a copy of the referenced documents, visit the Texas Instruments web site at www.ti.com.

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