Continuous-time Sigma-Delta AD conversion for wireless communication

K. Philips, P. A. C. M. Nuijten, A.H.M. van Roermund*
Philips Research, The Netherlands
* Eindhoven University of Technology, The Netherlands

Abstract

In a quest for flexibility, receivers for wireless communications are being digitized. Analog filters and variable gain amplifiers (VGA) are exchanged for digital processing at the expense of a very challenging ADC. Wireless interconnectivity in particular, seems a first candidate for a full-digital baseband implementation. Compared to mobile communication, sensitivity and interferer levels are moderate. Two converter solutions for a full-digital Bluetooth receiver are presented here. The first –rather conventional- ADC achieves high resolution and low power consumption by careful design. The second solution merges analog filtering and VGA into the ADC. This results in a further power reduction because the converter performance is better tailored to the input signal.

1. Bluetooth receiver

A conventional –highly analog- Bluetooth receiver is depicted in Figure 1. The baseband part consists of a cascade of filter and gain sections. The latter limit the signal to a pre-defined level. The bits are recovered by further analog demodulation (for example using a zero-crossing detector [1] or a frequency discriminator [2]) and by consecutive quantization.

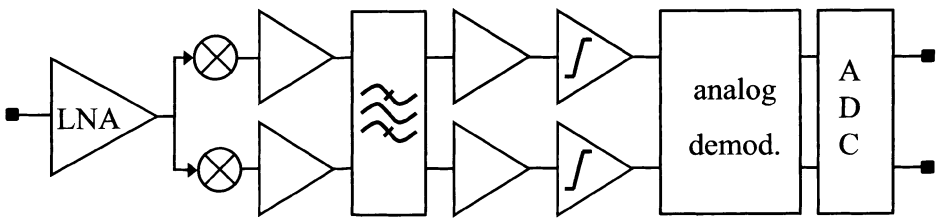


Figure 1 Conventional, dominantly analog Bluetooth receiver

J. H. Huijsing et al. (eds.), Analog Circuit Design, 273-292.

Figure 2 presents an alternative concept based on sigma-delta A/D conversion. The sigma-delta loop resembles the baseband of Figure 1 in the sense that the loop filter takes the place of the cascade of filter and gain sections. The quantizer is sampled at a much higher rate mf_s (m indicates the over-sample factor, f_s is the Nyquist sample frequency equaling 2MHz for this low-IF Bluetooth receiver). In addition, overall feedback from the output of the quantizer to the first analog stage at baseband is applied. The feedback results in relaxed dynamic range (DR) requirements on the second, third and higher sections of the loop filter of the sigma-delta ADC because their noise and distortion is counteracted by the loop operation. Notice, this is similar to the conventional baseband: there the DR requirements on the consecutive sections decrease because of preceding filtering and (variable) gain.

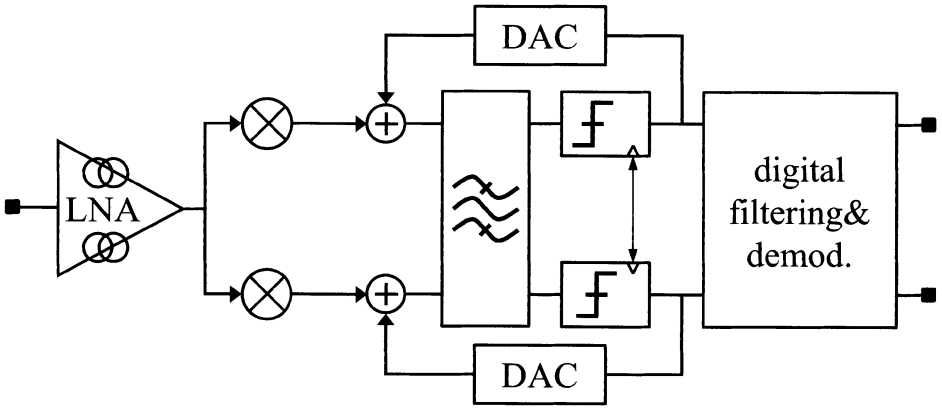


Figure 2 Highly digitised Bluetooth receiver with sigma-delta ADC

Other requirements on the analog sub-blocks are more relaxed for the sigma-delta solution than they are for the conventional solution. For example, gain accuracy, accuracy of time-constants, offset, etc. are very critical in the conventional baseband. Likely, multiple calibration loops need to be implemented. On the contrary, the gain accuracy of the loop filter is not important for a single-bit sigma-delta ADC and only a moderate accuracy is required for the loop filter time-constants. Furthermore, offset in the sigma-delta ADC is primarily due to the input stage and the amplification of the offset to the output is less than in the conventional baseband.

The above gives an intuitive reasoning why a high performance sigma-delta ADC in combination with digital demodulation can be a low power alternative for a conventional analog baseband in combination with analog demodulation.

2. High performance ΣΔ ADC with complex loop filter

A single-bit, continuous-time sigma-delta ADC is presented here (Figure 3, [3]). At a sample rate of 64MHz it needs a fifth-order complex loop filter to meet the required DR. The loop filter realizes high gain within the conversion bandwidth from 0 to 1MHz resulting in aggressive shaping of the quantization noise. The magnitude of the complex transfer function is depicted in Figure 4. Four filter notches are distributed evenly over the conversion bandwidth. One notch is put at the edge of the image band (i.e. at –1MHz). It –moderately- attenuates the noise in the image band such that a certain ''leakage'' due to finite matching between the I- and the Q-path is acceptable [4].

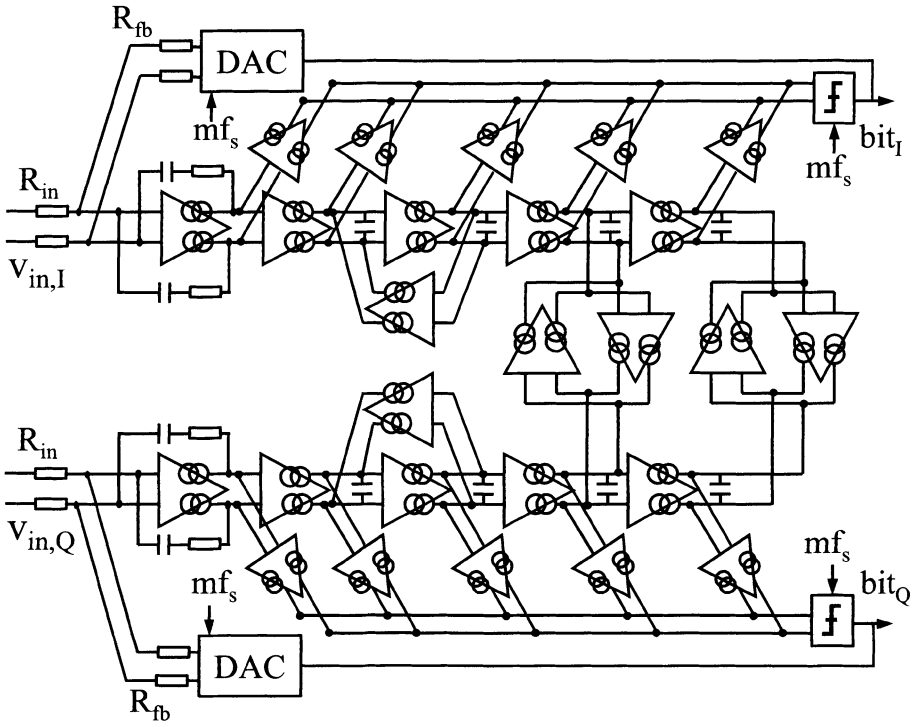


Figure 3 Block diagram of complex sigma-delta ADC

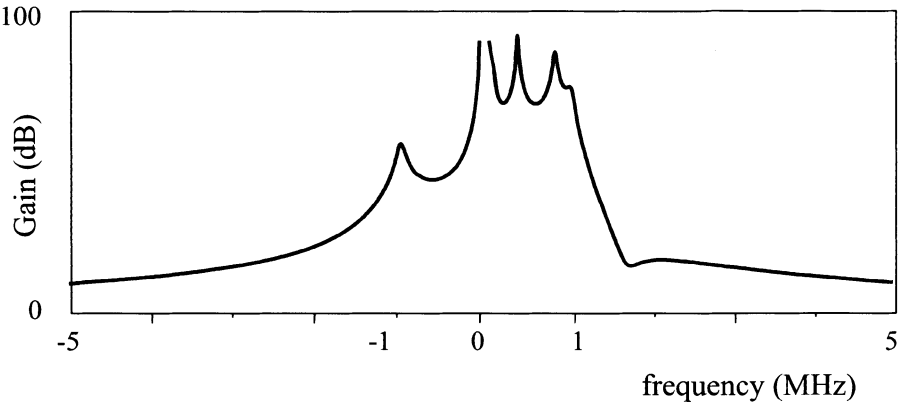


Figure 4 Transfer of complex loopfilter

2.1. Implementation

The loop filter consists of g_mC sections, except for the first stage [5]. The first stage is an operational transconductance amplifier (OTA) in a negative feedback configuration. It is of utmost importance to the performance of the sigma-delta ADC. This is motivated next.

First of all, the input transconductance g_m contributes importantly to the overall noise and therefore must be large. Also for linearity reasons a large g_m is favourable. Based on [6] the third-order inter-modulation product can be calculated as a function of the input signal v_{IN}, the g_m and v_{GT} of the input transistor and the resistors R_{in} and R_{fb} (see Figure 3):

$$IM_3 = \frac{3}{16}\left(\frac{\hat{v}_{IN}}{v_{GT}}\right)^2 \frac{1}{g_m^3 R_{in}^3}\left(1+\frac{R_{in}}{R_{fb}}\right) \qquad (1)$$

For a fixed bias current IM_3 improves quadratically with v_{GT} while it is cubic in g_m. Hence, the input transistor should be biased near weak-inversion to achieve lowest distortion. In that case, the linear input range, i.e. v_{GT}, decreases but g_m grows. A larger g_m results in a smaller error signal at the virtual ground input. Both effects are counteracting but the latter is dominant because of the cubic relation. Hence, $g_m/I = 10$ is chosen (with the bias current $I=500\mu A$)[1].

[1] When biasing the input transistors in weak-inversion v_{GS} should be replaced by nkT/q in the formulas.

Beyond the unity gain bandwidth f_{ug} of the sigma-delta loop:

$$IM_3 = \frac{3}{16}\left(\frac{\hat{v}_{IN}}{v_{GT}}\right)^2 \quad (2)$$

Hence, v_{GT} should not be too small either to prevent inter-modulation of interferers at high frequencies causing spurious components within the conversion bandwidth.

Furthermore, the input stage must provide a virtual ground summing node for the input current and the feedback current. The virtual ground node must be guaranteed over a wide bandwidth. In this particular receiver, the ADC is not preceded by any channel filter. Therefore, the bandwidth of the overall input signal, including interferers, can be large. It may extend over the entire Bluetooth operation band of ~80MHz. (For clarity, the conversion bandwidth of the ADC only corresponds to a single 1MHz wanted channel.) Also, the feedback signal contains a lot of energy at high frequencies. The bandwidth of the input stage must be large compared to that of the input signal and that of the feedback signal. This favors the use of single stage solutions such as a telescopic or a folded cascode topology.

A folded cascode stage can accommodate a large output swing for the integration while a telescopic cascode only takes a minimum number of current branches. Because the first stage dominates in the overall current consumption (due to the high g_m) the latter argument prevails. This choice is a key reason for the power efficiency of the presented ADC.

Table 1 gives a further comparison of some candidate topologies for the first stage. The telescopic cascode features a large bandwidth and a minimum bias current for a target g_m. In addition, it has a minimum number of noise sources. The telescopic cascode is likely to be somewhat less linear because of a tighter output range. The dominant non-linearity, i.e. the input transconductance, is the same as in the other topologies though.

Table 1 Circuit topologies for the input stage

	2-stage	Folded cascode	Telescopic cascode
BW	-	+	+
I_{bias} (for fixed g_m)	-	--	+
Noise	-	--	+
Distortion	+	+	-

Figure 5.a shows the schematic of the first integrator in the loop filter. All sources are cascoded to improve the output impedance and to decrease the influence of its non-linearity. The n-MOS current source is degenerated with transistors in the triode region providing the output common mode control. The control relies on matching with a replica bias circuit. The input common mode is set by the DAC output. Noticeably, a differential output swing of $0.5V_{pp}$ is allowed even though a lot of devices are stacked in the circuit.

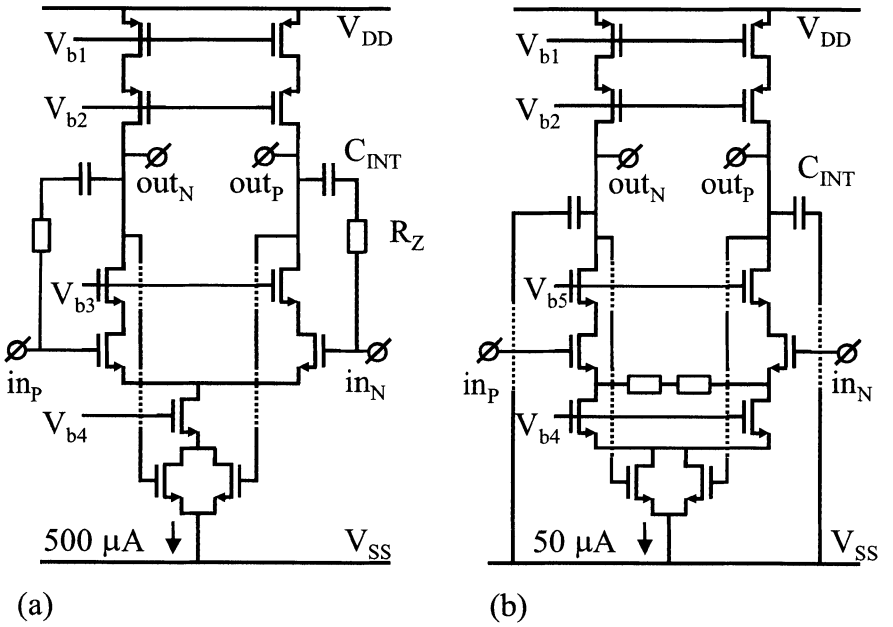


Figure 5 Implementation of the first (a) and the following integrators (b)

Basically, the second and higher sections of the loop filter consist of down-scaled copies of the first stage (Figure 5.b). Because their noise and distortion is suppressed by the preceding gain in the loop they can be biased at a 10 times lower current. Contrary to the first stage the input of these OTAs is not a virtual ground node. Instead, there can be a large signal swing on the input node since it is connected to the output of the previous integrator. The transconductances are degenerated to increase their linear input range. As a consequence, all time-constants of the loop filter are set by RC-products and therefore match well.

The feed-forward coefficients are based on degenerated differential pairs. These feed their output current directly into a current-mode latch that also serves as a summing node [7].

The single-bit output code is fed back to the input by a resistive DAC: the resistor R_{fb} is connected to a positive or a negative reference voltage depending on the output code. A return-to-zero scheme is applied to reduce inter-symbol-interference.

2.2. Measurement results

Figure 6 shows the measured SNR as a function of the signal level. The latter is normalized to the full-scale of the digital output code: at a 70% modulation depth of the digital output (i.e. –3dB digital full-scale) a peak-SNR of 75.5dB is achieved.

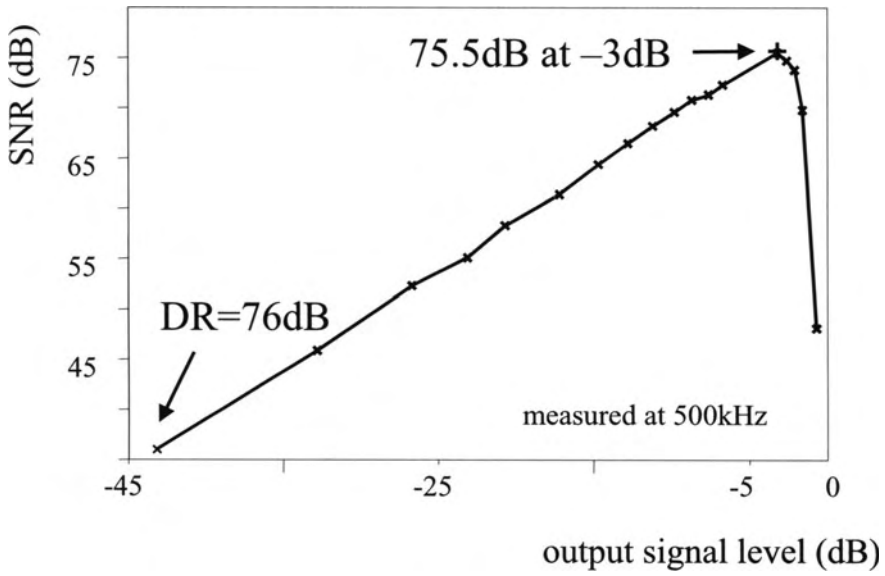


Figure 6 SNR as a function of the output level

Figure 7 shows the output spectrum of a two-tone test: two input signals are applied at –9dB, their IM_3 products are smaller by 82dB.

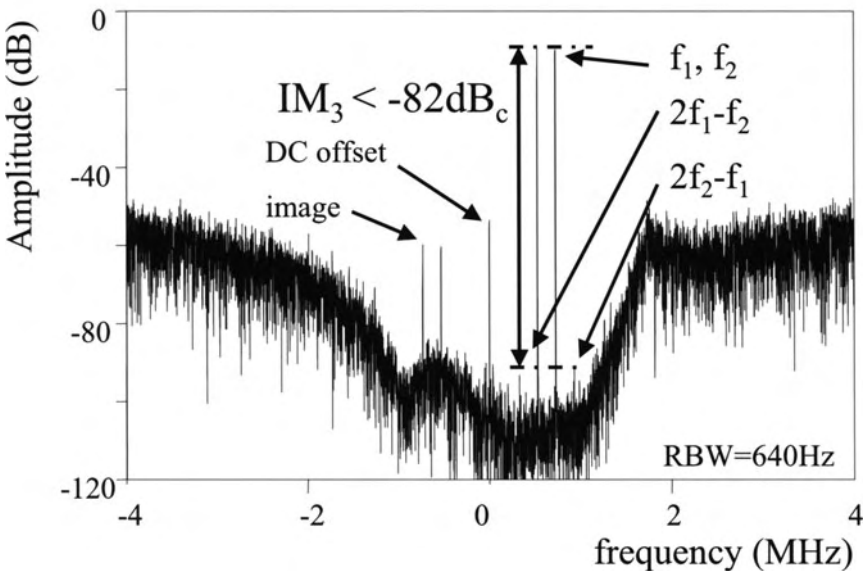


Figure 7 Output spectrum for IM_3 test

Finally, Table 2 lists some conventional ADC performance metrics.

Table 2 Performance metrics

input signal	0-1 MHz, 0.35 V_{rms}(per channel)
sample frequency	64 MHz
dynamic range	76 dB
SINAD	75.5 dB
IM_3	<-82 dB_c
aliasing spurious	<-75 dB
power consumption	4.4 mW @1.8V
die area	0.22 mm^2

Since the ADC is used without preceding filter also the performance with respect to interferers must be evaluated. As the interferer channels grow they cause over-load of the DAC and the quantization noise rises. The allowed interferer level is frequency dependent because the signal transfer function (STF) from the input to the output of the ADC is so. Moreover, due to the complex loop filter the STF –and therefore the allowed interferer level- is asymmetrical around DC. This is illustrated with the measurement results in Figure 8.

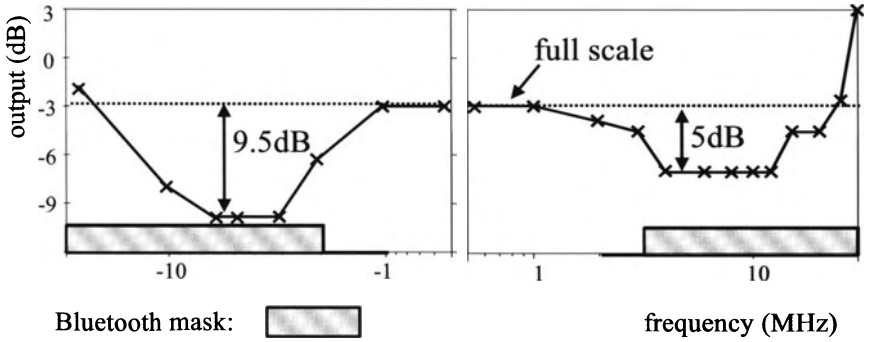


Figure 8 Allowed input level over frequency such that the DR in [0; 1MHz] does not decrease

Furthermore, Figure 9 shows the results of an interferer test: an input signal near the clock frequency is applied. It is attenuated in the continuous-time loop filter before being sampled in the quantizer. The remaining aliasing is counteracted by the loop operation such that it appears at –75dB. (The input level of the interferer corresponds to the level specified by the Bluetooth standard.)

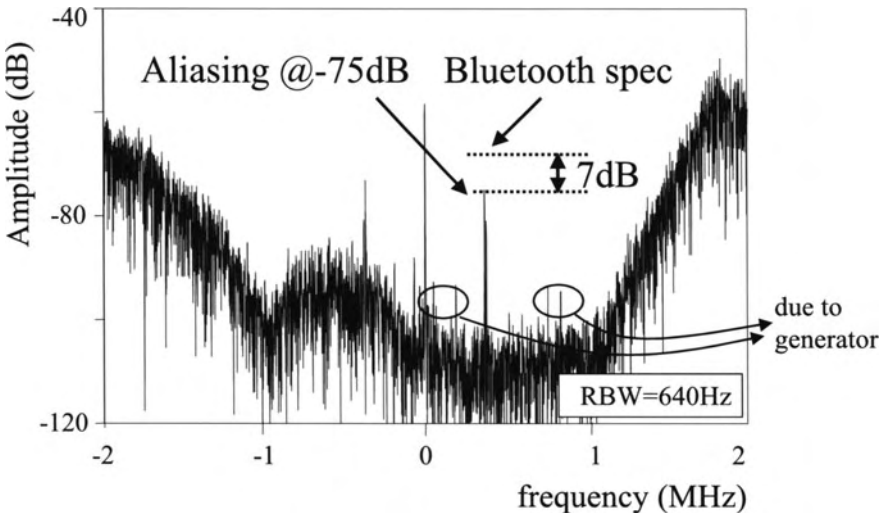


Figure 9 Anti-aliasing test with an input signal at –7dB (complying to a Bluetooth test) and 370kHz offset from the clock frequency

2.3. Evaluation of performance/power

The above ADC achieves a high DR and excellent linearity while consuming only 4.4mW. This is state-of the-art when comparing to [8] (achieving the same DR at a five times higher power consumption) or [9] (achieving 12dB less DR at only twice less current).

Still, it does not necessarily provide the most low-power baseband architecture for the receiver. This is intuitively understood from the example of the input spectra of Figure 10. Suppose the wanted signal is small but a large interferer is present (Figure 10.a). The full-scale input level of the ADC must be designed to accommodate the large interferer while the noise must remain low compared to the wanted signal. Alternatively, suppose the wanted signal is strong (Figure 10.b). It is converted with a SINAD of 75.5dB while only some 18dB is required for demodulation. In both examples, part of the DR is ''wasted" for the interferers.

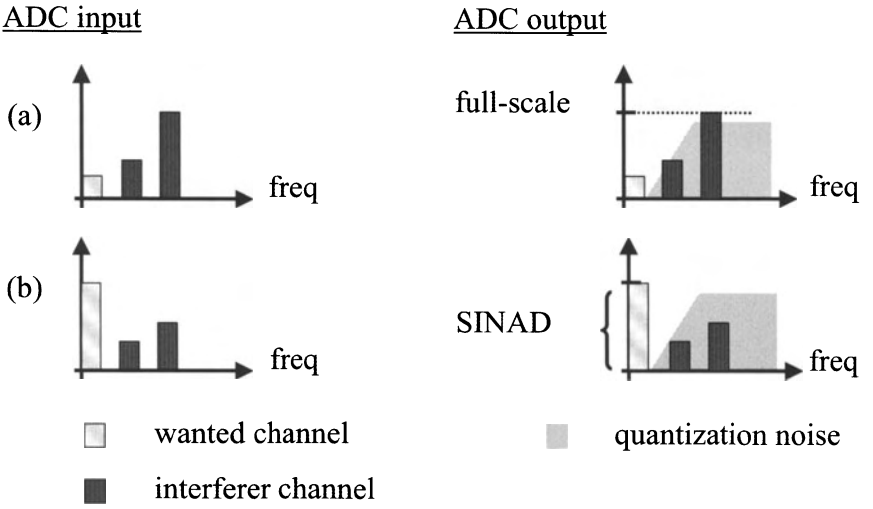


Figure 10 Example input spectra and corresponding output

The ADC that is presented next merges some explicit analog filtering and variable gain control into the sigma-delta loop. By consequence, the input range is better tailored to the expected spectrum of the input signal including interferers. This results in lower overall power consumption.

3. Filtering sigma-delta ADC

A low-pass filter $H_{LPF}(s)$ and a compensating high-pass filter $H_{HPF}(s)$ are added to a conventional sigma-delta ADC as depicted in Figure 11, [10]. The sum of these filters equals 1 over the entire frequency range such that the stability and the noise shaping of the loop remain unaltered from that of the conventional ADC. The STF of the new topology is different though:

$$STF_{filterADC}(s) = STF_{conv.ADC}(s) \cdot H_{LPF}(s) \qquad (3)$$

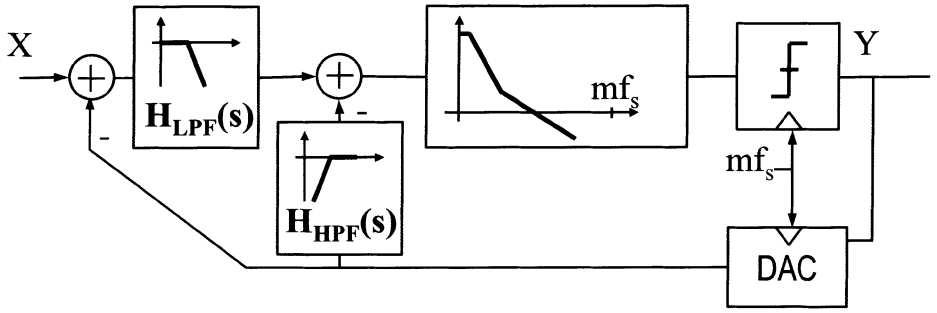


Figure 11 Concept of the sigma-delta ADC with explicit filtering

The STF features explicit low-pass filtering. The –3dB-frequency of $H_{LPF}(s)$ is chosen such that interferers are attenuated towards the output[2]. This is shown in Figure 12 for a filtering ADC based on a conventional design with a fourth order loop filter, to which a first-order low-pass filter and the compensating high-pass filter are added. As a consequence, interferers can be applied at a higher level than in the conventional ADC without over-loading the DAC. The maximum allowed input level –without increasing the noise in the wanted channel- equals the full-scale level for the wanted channel divided by the STF of the filtering ADC. Hence, it is inversely proportional to the curve of Figure 12. This will be illustrated with measurements later on. Notice, a fourth-order, real loop filter is used instead of the fifth-order complex filter for the previous ADC. Again, this is commented further on.

[2] Only for nearby frequencies the attenuation is limited. This is due to the overshoot in the STF of the conventional ADC that is taken as a starting point. In case a less aggressive loop filter were chosen the overshoot would be less.

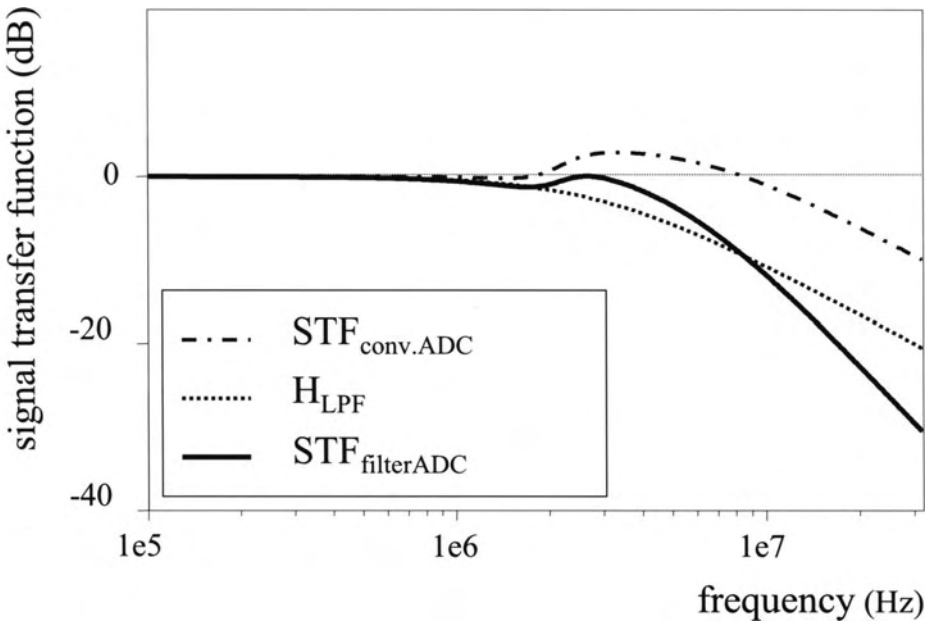
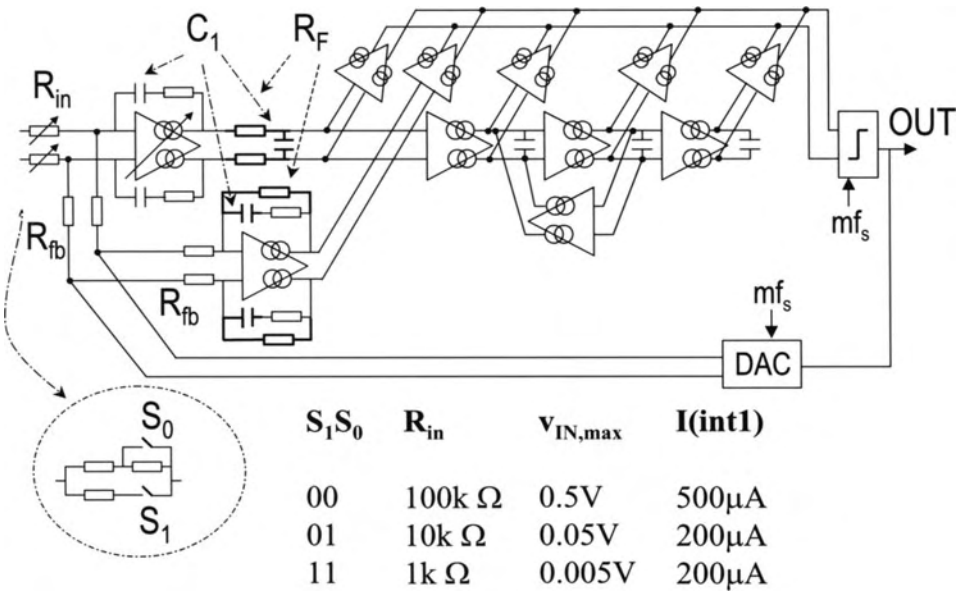


Figure 12 Signal transfer function of the filtering ADC, of the conventional ADC and of the first-order low-pass filter

3.1. Implementation

The implementation of the loop filter is similar to that of the previous ADC. In fact, the same building blocks are re-used and are scaled were appropriate.

A simple first-order low-pass filter with a –3dB-frequency of 3MHz and the compensating high-pass filter are added. A passive implementation of $H_{LPF}(s)$ becomes possible when shifted behind the first integrator stage (Figure 13). The first integrator stage must then be duplicated in the compensating path. There, the series configuration of $H_{HPF}(s)$ and the integrator results in a low-pass filter allowing an easy implementation.



S_1S_0	R_{in}	$v_{IN,max}$	I(int1)
00	100k Ω	0.5V	500μA
01	10k Ω	0.05V	200μA
11	1k Ω	0.005V	200μA

Figure 13 Block diagram of filtering sigma-delta ADC

The added filters hardly increase the overall power consumption of the ADC. The noise and distortion of the passive filter is suppressed by the preceding gain of the first integrator[3]. The same is true for the OTA in the feedback path. Hence, this active stage can be biased at only 50μA. Only the first integrator remains critical for the same reasons as discussed for the complex ADC in the previous section.

The filtering STF of this ADC is optimally exploited in combination with variable gain control of the input signal. The input resistance is switched between 1kΩ, 10kΩ and 100kΩ depending on the amplitude of the input signal. As such, the input range for wanted signals is scaled from 5mV to 50mV and to 500mV. The interferer signal can be larger by at least 20dB per decade of frequency offset from the –3dB-frequency of $H_{LPF}(s)$. The characteristic of the allowed input level over frequency (i.e. the inverse of the curve in Figure 12) must be tailored such that it optimally accommodates the entire input spectrum. This is achieved by the choice of $H_{LPF}(s)$ and –to a lesser extent- by the design of the STF of the conventional ADC.

[3] Notice, this would not have been the case if the passive filter were preceding the ADC. Then, it would contribute in the overall noise.

The bias current of the first stage is adapted dynamically to the input range in order to scale this dominant noise source. The bias current equals 500μA for the smallest input range and 200μA otherwise. The lower limit on the bias current is set by a bandwidth limitation. The dynamic biasing lowers the average power consumption.

Notice, a fourth-order, real loop filter is used instead of a fifth-order complex filter in the previous section. Because of the integration of the filter and VGA a reduced output SINAD is allowed while the input-referred DR remains large. Hence, the noise shaping can be relaxed. (Potentially, also the sample rate can be reduced. In this design, it remains 64MHz though.) By consequence, the decimation filter becomes simpler as well. Moreover, the accuracy of the DAC references can be relaxed because the clock jitter and the noise on voltage or current references is related to the output SINAD instead of the much larger DR of the input signal. This results in a major power reduction in all these circuits.

As a summary, the integration of a filter in the sigma-delta loop in combination with variable gain control of the input signal and adaptive biasing results in a lower average power consumption of this ADC compared to the ADC of the previous section. Its peak consumption has hardly increased. In addition, the power consumption in the decimation filter and all DAC references decreases.

3.2. Measurements results

The filtering behavior of the ADC is demonstrated in the three-tone test of Figure 14: a small wanted signal of 5mV at f_1=700kHz is applied as well as interferers of 30mV and 120mV at f_2=4.8MHz and f_3=10MHz respectively. The input resistance is switched to 1kΩ such that the wanted signal appears at –3dB of the digital full-scale output. The interferers though, are attenuated to –9dB and –10dB respectively. Within the conversion bandwidth of the ADC the noise increases by only 1dB due to spurious components from the generator. The inter-modulation tone at f_3-2f_2 is at –58dB.

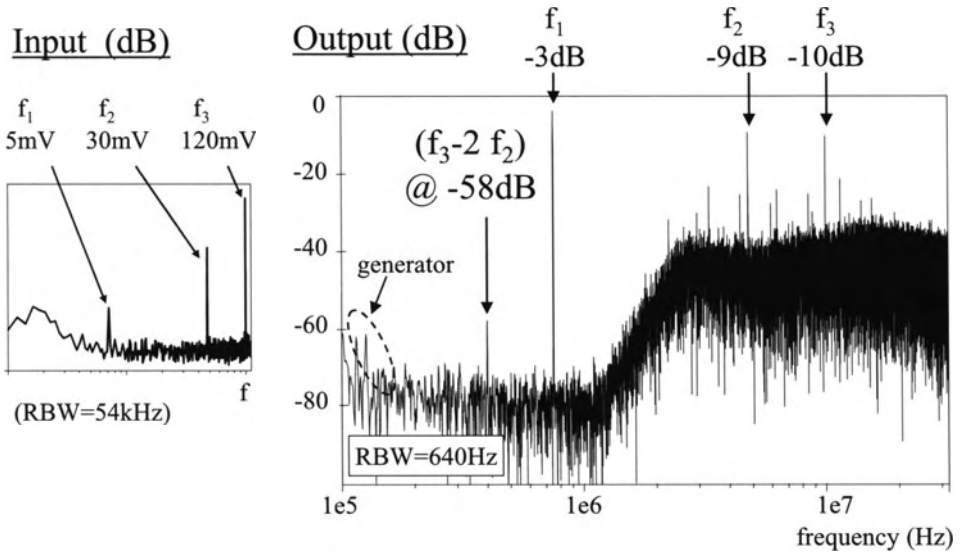


Figure 14 Three-tone measurement proving filtering transfer and linearity (f_1=700kHz, f_2=48MHz and f_3=10MHz)

Figure 15 plots the measured allowed input level over frequency such that noise and spurious do not increase within the conversion bandwidth. The measurements are shown for R_{in}=1kΩ: especially in the case of a small wanted signal the interferers are likely to be larger. The allowed interferer level is compared to that for a conventional (i.e. without $H_{LPF}(s)$ and $H_{HPF}(s)$), fourth-order sigma-delta ADC in order to demonstrate the improvement. For the other settings, i.e. R_{in}=10kΩ and R_{in}=100kΩ, the allowed level of nearby interferers

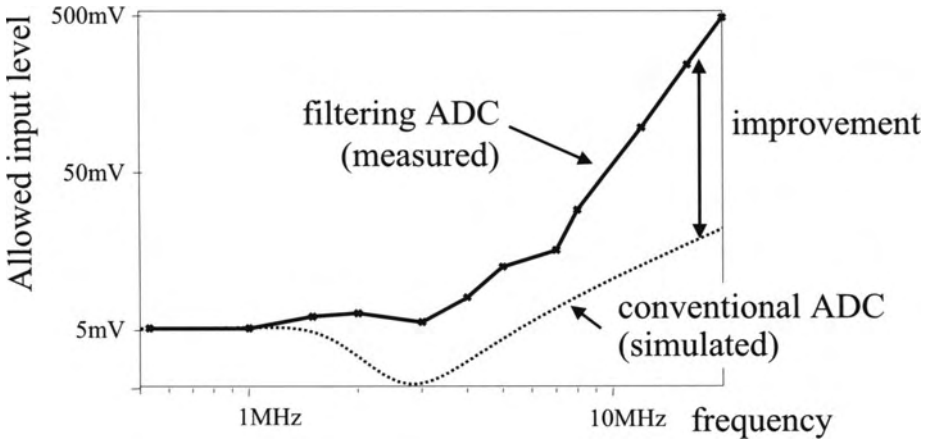


Figure 15 Allowed input level over frequency such that DR in the wanted channel is not jeopardized (for gain setting R_{in}=1kΩ)

follows the same curve; only, the absolute value is larger by a factor 10 and 100 respectively. Reliability issues proper to the technology limit the allowed level of far-off interferers.

Figure 16 shows the measured signal-to-noise (SNR) and the signal-to-noise-and-distortion (SINAD) as a function of the input level for the three modes. An overall, input-referred dynamic range of 89dB is achieved. The SNR and SINAD at the output are moderate because of the integrated filtering and variable gain control. Hence, this filtering ADC constitutes a true equivalent of the conventional cascade of analog filter, VGA and ADC in the sense that it reduces the signal dynamic range from input to output. The moderate SINAD at the output of the ADC results in a low-power ADC (see Table 3), a high tolerance of noise and jitter on the DAC references and relaxed attenuation demands on the decimation filter. This will be demonstrated in the next paragraph.

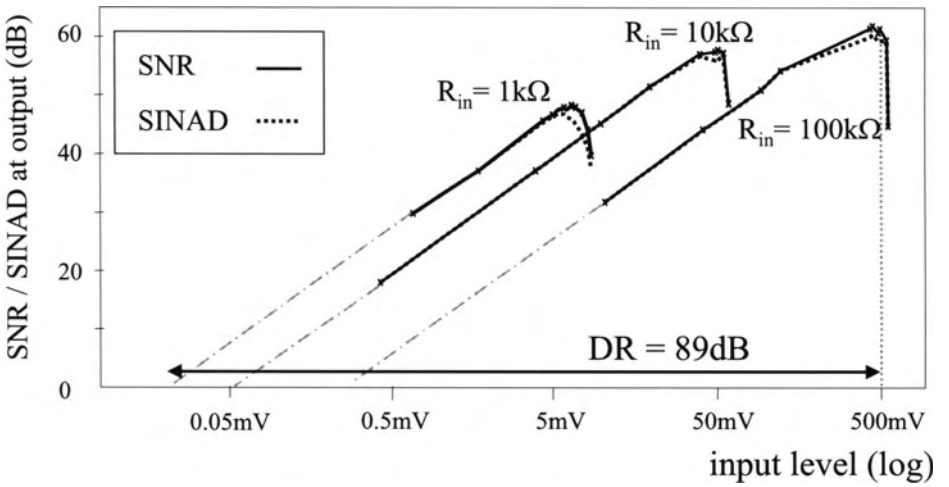


Figure 16 Measured SNR (SINAD) as a function of the signal level

Notice that the peak-SNR and the DR differ per gain setting (see Table 3). This is due to the fact that the relative contribution of thermal noise –compared to quantization noise- is different for the various gain settings. For Rin=100kΩ quantization noise is dominant. For Rin=1kΩ the input signal is 100 times smaller while the bias current of the first stage is only 2.5 times larger. As a consequence, the thermal noise power associated with this stage is significantly larger than the quantization noise. As a second order effect, also the influence of the other stages of the loop filter becomes more important: as Rin is smaller their input-referred contribution scales as well. The quantization noise though,

remains the same for all gain settings because the loop parameters (i.e. the time-constants) are unaltered.

4. Evaluation of performance/power

Table 3 summarizes the measured performance of the ADC for the three gain settings. These numbers only relate to the performance with respect to the wanted channel. In addition to that, the performance in the presence of interferers has been evaluated: the filtering STF provides immunity to interferers above the full-scale level for wanted signals as characterized in Figure 8. The combination with passive, programmable gain enables an input referred, overall DR of 89dB for the wanted signal while only consuming 2mW (or less depending on the gain setting). As discussed, the DR for interferers is even larger.

Table 3 Performance of the filtering ADC for the three gain settings

R_{in}	$V_{IN,max}$	DR	SINAD	P (@1.8V)
100 kΩ	500 mV	65 dB	59 dB	1.5 mW
10 kΩ	50 mV	59 dB	57 dB	1.5 mW
1 kΩ	5 mV	49 dB	46 dB	2 mW

5. Comparison of the ADCs in terms of performance/power

The presented ADCs target the same application. Moreover, they largely consist of the same circuits and are implemented in the same 0.18μm CMOS technology. Hence, a comparison of the performance/power between both is straightforward. It is listed in Table 4. Since quadrature conversion is targeted the numbers in the right-hand column of Table 4 refer to the power, area and performance of two filtering ADCs together. At a comparable area and power consumption the solution with the filtering ADCs achieves a 16dB higher DR (input-referred) and a better tolerance to noise on the DAC references.

The SINAD provided at the output of the filtering ADC is much smaller because of the integrated filtering and VGA. It is still by far sufficient though for the demodulation of a Bluetooth signal. This moderate SINAD is intentional and results in a major power saving in the ADC and on a system level. First of all, the requirements on the consecutive decimation filter can be relaxed: only a moderate attenuation of quantization noise and interferers is needed. This translates in a lower power and area for this block. More important even, noise and jitter on the references (i.e. voltage/current/charge and time) for the feed back DAC become less critical since the DAC only needs a moderate accuracy. The last row of Table 4 indicates a major improvement with respect to noise and

jitter. Especially for the clock generation this again results in significant power saving.

Table 4 Comparison of conventional complex ADC and filtering ADC with merged VGA

	Complex ADC	2 filtering ADCs
P	4.4 mW	< 4.1 mW
die area	0.22 mm^2	0.28 mm^2
DR	76 dB	92 dB
SINAD	75.5dB	> 46 dB
allowed noise and jitter on DAC references	< 0.02 %	< 0.4 %

6. Conclusions

Two ADCs have been presented. The first one combines a high SINAD with low power consumption. These features result from the aggressive loop filter and the low power circuit design. The latter is achieved by biasing the critical transconductors near weak-inversion and by using a minimum number of current branches.

In the second ADC some VGA and filtering of interferers are merged into the sigma-delta loop. This architectural innovation yields 16dB more DR and an overall power saving. The power saving results from a lower average power consumption in the ADC and from relaxed requirements on peripheral circuits. The technique is particularly interesting in wireless applications: these typically require a large input-referred DR while only a small SINAD is needed for demodulation.

Although the first ADC already achieves an excellent power/performance ratio the comparison proves that by tailoring the ADC to the specific needs of the application a further, major improvement is possible. While circuit level optimization improves the power/performance ratio of ADCs in an evolutionary way architectural innovation may yield a leap step.

7. Acknowledgements

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