Advanced Digital Post-Processing Techniques Enhance Performance in Time-Interleaved ADC Systems

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INTRODUCTION

Time interleaving of multiple analog-to-digital converters by multiplexing the outputs of (for example) a pair of converters at a doubled sampling rate is by now a mature concept—first introduced by Black and Hodges in 1980.[1, 2] While designing a 7-bit, 4-MHz A/D converter (ADC), they determined that a time-interleaved solution would require less die area than a comparable 2^n flash converter design. This new concept proved of great value in their design, but saving space was not its only benefit. Time interleaving of ADCs offers a conceptually simple method for multiplying the sample rate of existing high-performing ADCs, such as the 14-bit, 105-MSPS AD6645 and the 12-bit, 210-MSPS AD9430. In many different applications, this concept has been leveraged to benefit systems that require very high sample rate analog-to-digital conversion.

While the speed and resolution of standard ADC products have advanced well beyond 4 MHz and 7 bits, time-interleaved ADC systems (for good reasons) have not advanced far beyond 8-bit resolution. Nevertheless, at 8-bit performance levels, this concept has been widely adopted in the test and measurement industry, particularly for wideband digital oscilloscopes. That it continues to make an impact in this market is evidenced by the 20-GSPS, 8-bit ADC that was recently developed by Agilent Labs[3] and adopted by the Agilent Technologies Infiniium™ oscilloscope family.[4] Indeed, time-interleaved ADC systems thrive at the 8-bit level, but they continue to fall short in applications that require the combination of high resolution, wide bandwidth, and solid dynamic range.

The primary limiting factor in time-interleaved ADC systems at 12- and 14-bit levels is the requirement that the channels be matched. An 8-bit system that provides a dynamic range of 50 dB can tolerate a gain mismatch of 0.25% and a clock-skew error of 5 ps. This level of accuracy can be achieved by traditional methods, such as matching physical channel layouts, using common ADC reference voltages, prescreening devices, and active analog trimming, but at higher resolutions the requirements are much tighter. Until now devices employing more innovative matching techniques have not been commercially available.

This article will outline in detail the matching requirements for 12- and 14-bit time-interleaved ADC systems, discuss the idea of advanced digital post-processing techniques as an enabling technology, and introduce a device employing the most promising solution to date, *Advanced Filter Bank* (AFB™), from V Corp Technologies, Inc.[5, 6]

Time Interleaving Process Overview

Time interleaving of ADC systems employs the concept of running m ADCs at a sample rate that is $1/m$ of the overall system sample rate. Each channel is clocked at a phase that enables the system as a whole to sample at equally spaced increments of time, creating the seamless image of a single A/D converter sampling at full speed. Figure 1 illustrates the block- and timing diagrams of a typical four-channel, time-interleaved ADC system. Each of the four ADC channels runs at one-fourth the system's sample rate, spaced at 90° intervals. The final output data stream is created by interleaving all of the individual channel data outputs in the proper sequence (e.g., 1, 2, 3, 4, 1, 2, etc.). In a two-converter example, both ADC channels are clocked at one-half of the overall system's sample rate, and they are 180° out of phase with one another.

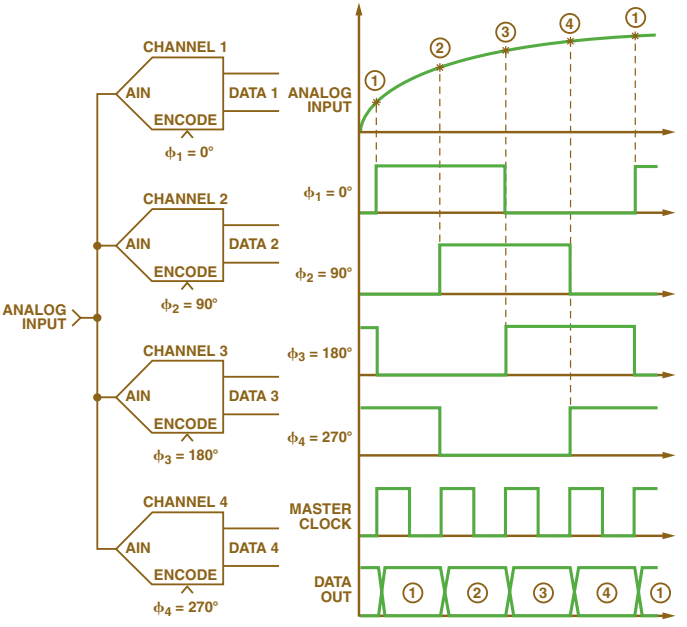

Figure 1. Four-channel time-interleaved ADC system.

For simplicity, this article focuses primarily on two-converter systems, but four-converter systems are discussed when required to articulate key performance differences. Most of the block diagrams, mathematical relationships, and solutions will highlight the two-channel configuration.

Design Challenge of Time Interleaving

As mentioned, channel-to-channel matching has a direct impact on the dynamic range performance of a time-interleaved ADC system. Mismatches between the ADC channels result in dynamic range degradation that—in an FFT plot—show up as spurious frequency components called *image spurs* and *offset spurs*. The image spur(s) associated with time-interleaved ADC systems are a direct result of gain- and phase mismatches between the ADC channels. The gain- and phase errors produce error functions that are orthogonal to one another. Both contribute to the *image-spur* energy at the same frequency location(s). The *offset spur* is generated by offset differences between the ADC channels. Unlike the image spur(s), the offset spurs are not dependent on the input signal. For a given offset mismatch, the offset spur(s) will always be at the same level. Extensive studies of the behavior of these spurs have resulted in several mathematical methods for characterizing the relationship between channel matching errors and dynamic range performance.[7, 8]

While these methods are thorough and very useful, the "error voltage" approach used here provides a simple method for understanding the relationship without requiring a deep study of complex mathematical derivations. This approach is based on the same philosophy used in Analog Devices Application Note AN-501[9] to establish the relationship between aperture jitter and signal-to-noise (SNR) degradation in ADCs. The *error voltage* is defined as the *difference between the "expected" sample voltage and the "actual" sample voltage*. These differences are a result of a large subset of errors that fall into three basic categories: *gain* (Figure 2), *phase* (Figure 3), and *offset* (Figure 4) mismatches.

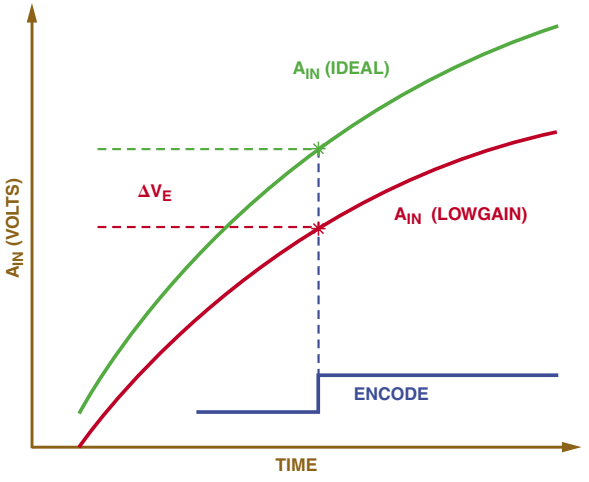

Figure 2. Voltage error due to gain mismatch.

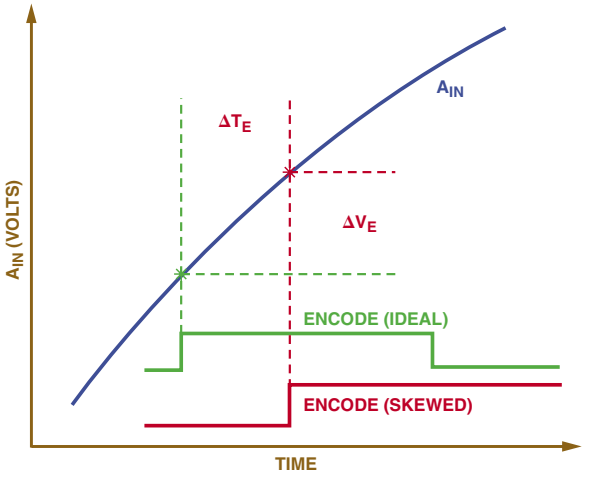

Figure 3. Voltage error due to encode/clock skew.

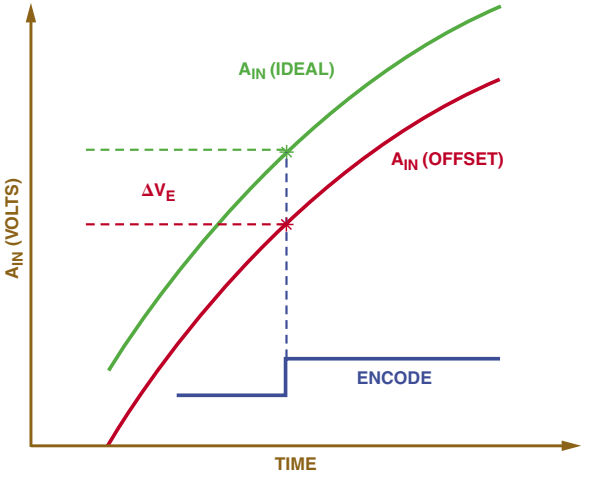

Figure 4. Voltage error due to offset mismatch.

In a two-converter interleaved system, the error voltages generated by *gain* and *phase* mismatches result in an *image* spur that is located at Nyquist minus the analog input frequency. The *offset* mismatch generates an error voltage that results in an *offset spur* that is located at Nyquist. Since the offset spur is located at the edge of the Nyquist band, designers of two-channel systems can typically plan their system frequency around it, and focus their efforts on gain- and phase matching. Figure 5 displays a typical FFT plot for a two-channel system.

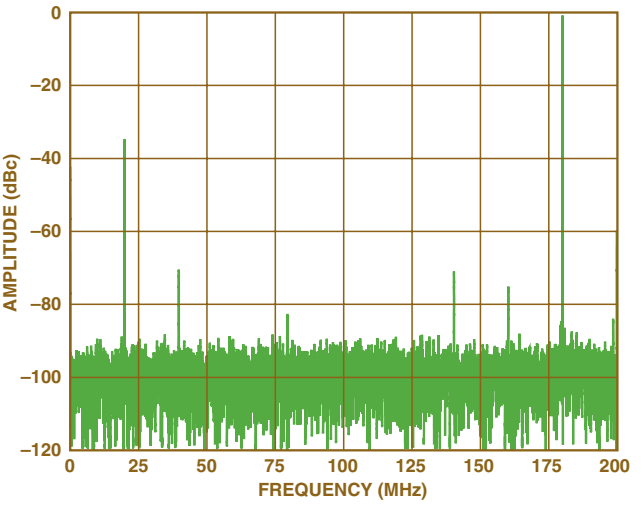

Figure 5. Typical two-converter interleaved FFT plot.

In a four-converter interleaving system, there are three image spurs and two offset spurs. The *image spurs*, generated by gain and phase mismatches between the ADC channels, are located at (1) Nyquist minus the analog input frequency and (2) one-half Nyquist plus or minus the analog input frequency. The *offset spurs* are located at Nyquist and at one-half of Nyquist (middle of the band). Figure 6 displays a typical FFT plot of a four-converter system, illustrating the locations of these five spurs.

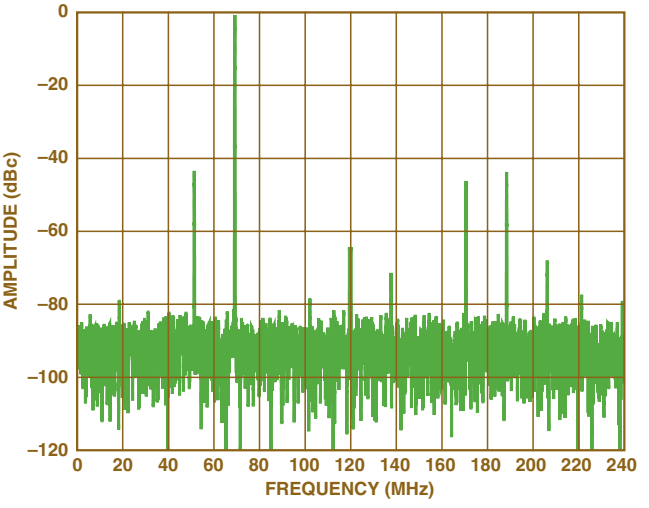

Figure 6. Typical four-converter interleaved FFT plot.

Once the error voltages from each of the three mismatch groups are known, the following equations can be used to calculate the image and offset spurs (IS_{gain}, IS_{phase}, IS_{total}, OS_{offset}) in a single-tone, two-converter system:

$$IS_{gain(dB)} = 20 \times \log(IS_{gain}) = 20 \times \log\left(\frac{G_e}{2}\right)$$
$$where\ G_e = gain\ error\ ratio = \left|1 - \frac{V_{FSA}}{V_{FSB}}\right| \quad (1)$$

$$IS_{phase(dB)} = 20 \times \log(IS_{phase}) = 20 \times \log\left(\frac{\theta_{ep}}{2}\right)$$
$$where\ \theta_{ep} = \omega_a \times \Delta t_e (radians) \quad (2)$$
$$\omega_a = analog\ input\ frequency$$
$$\Delta t_e = clock\ skew\ error$$

$$IS_{total\,(dB)} = 20 \times \log \sqrt{\left(IS_{gain}\right)^2 + \left(IS_{phase}\right)^2} \quad (3)$$

$$OS_{offset\,(dB)} = 20 \times \log\left(\frac{Offset}{2 \times Total\,Codes}\right) \quad (4)$$

$$where\,Offset = channel - to - channel\,offset\,(codes)$$

As noted earlier, the gain- and phase errors generate error functions that are orthogonal[7], requiring a "root-sum-square" combination of their individual contributions to the image spur. Using these equations, an error budget can be developed to determine what level of matching will be required to maintain a given dynamic range requirement. For example, a 12-bit dynamic range requirement of 74 dBc at an input frequency of 180 MHz would require gain matching better than 0.02% and aperture delay matching better than 300 fs! If the gain can be perfectly matched, the aperture delay matching can be "relaxed" to approximately 350 fs. Figure 7 displays an example of a detailed "error budget curve" for this 12-bit, 180-MHz example.

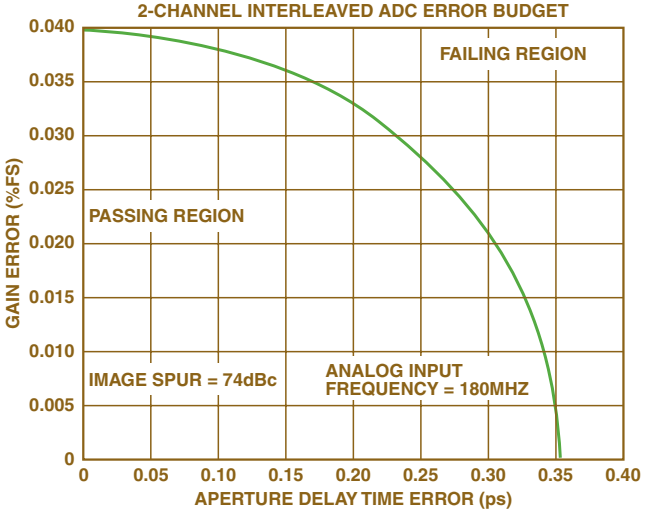

Figure 7. Error budget: 12-bit, 2-channel, 180-MHz input.

Table I provides the matching requirements for several different cases to illustrate the extreme precision required to make a classical time-interleaved A/D conversion system work at 12- and 14-bit resolutions over wide bandwidths.

Table I. Time-interleaved ADC matching requirements.

Performance Requirement at 180 MHz	SFDR (dBc)	Gain Matching (%)	Aperture Matching (fs)
12 Bits	74	0.04	0
12 Bits	74	0	350
12 Bits	74	0.02	300
14 Bits	86	0.01	0
14 Bits	86	0	88
14 Bits	86	0.005	77

Traditional Approach to Wide-Bandwidth Time-Interleaved ADC Systems

A traditional, 2-channel time-interleaving ADC system employs the basic configuration displayed in Figure 8. The first level of matching in traditional time-interleaving ADC systems is achieved through reducing the physical and electrical differences between the channels. For example, gain matching is typically controlled by the use of common reference voltages and carefully matched physical layouts. Phase matching is achieved by manually tuning the electrical length of the clock (or analog input) paths and/or through special trimming techniques that control an electrical characteristic of the clock distribution circuit (rise/fall times, bias levels, trigger level, etc.). The offset matching depends on the offset performance of the individual ADCs.

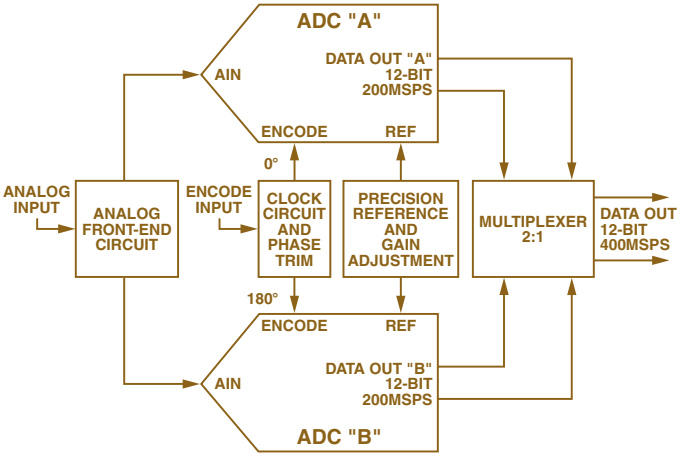

Figure 8. Functional diagram of a traditional time-interleaved ADC.

Many of these matching approaches are based on careful analog design and trim techniques. While there has been an abundance of excellent ideas to address these tough matching requirements, many of them require additional circuits that add error sources of their own—defeating the original purpose of achieving precise gain and phase matching. An example of such an idea would be setting the rise and fall times of the two different clock signals. Any circuit that could provide this level of control would be subjected to increased influence of power-supply voltage—and temperature—on each channel's phase behavior.

Advanced Digital Post Processing

The development of new digital signal processing techniques, along with the advances in inexpensive, high-speed, configurable digital hardware platforms (DSPs, FPGAs, CPLDs, ASICs, etc.), has opened the way for breakthroughs in time-interleaving ADC performance. Digital *post-processing* approaches have several advantages over classical analog matching techniques. They are flexible in their implementation and can be designed for precision well beyond the ADC resolutions of interest. A conceptual view of how digital signal processing techniques can impact time-interleaved system architectures can be found in Figure 9. This concept employs a set of digital calibration transfer functions that process each ADC's output data, creating a new set of "calibrated outputs." These digital calibration transfer functions can be implemented using a variety of digital filter configurations (FIR, IIR, etc.). They can be as simple as trimming the gain of one channel or as complicated as trimming the gain, phase, and offset of each channel over wide bandwidths and temperature ranges.

Wide bandwidth and temperature matching presents the greatest opportunity—and challenge—for using digital post-processing techniques to improve the performance of time-interleaving ADC systems. The mathematical derivations required for designing the digital calibration transfer functions for multiple ADC channels over wide bandwidths and temperature ranges are extremely complex and not readily available. However, a great deal of academic work has been invested in this area, creating a number of interesting solutions. One of these solutions, known as *Advanced Filter Bank* (AFB), stands out in its ability to provide a platform for a significant breakthrough.

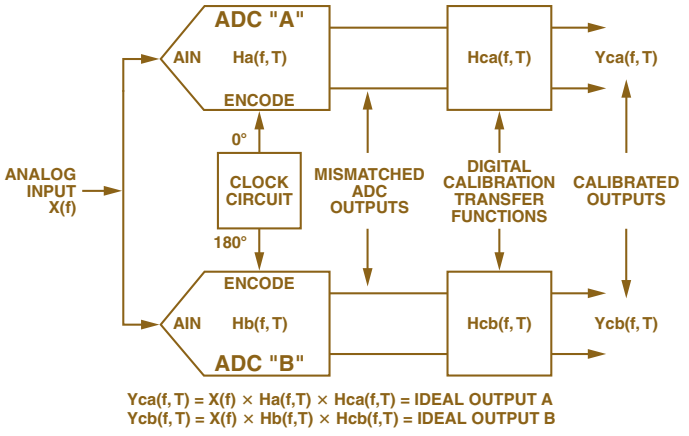

Figure 9. Example of digital post-processing architecture.

Advanced Filter Bank (AFB)

AFB is one of the first commercially available digital post-processing technologies to make a significant impact on the performance of time-interleaving ADC systems. By providing precise channel-to-channel gain, phase, and offset matching over wide bandwidths and temperature ranges, AFB is well-positioned to solidly establish time-interleaving ADC systems in the area of high-speed, 12-/14-bit applications. Besides its matching functions, AFB also provides phase linearization and gain-flatness compensation for ADC systems. Figure 10 displays a basic block diagram representation of a system employing AFB.

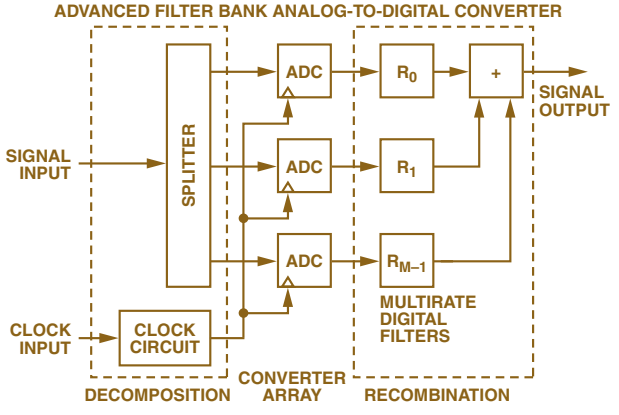

Figure 10. AFB basic block diagram.

By using a unique multirate FIR filter structure, AFB can be easily implemented into a convenient digital hardware platform, such as an FPGA or CPLD. The FIR coefficients are calculated using a patented method that involves starting with the equations seen in Figure 9, and then applying a variety of advanced mathematical techniques to solve for the digital calibration transfer function.

AFB enables time-interleaving ADC systems to use up to 90% of their Nyquist band, and can be configured to operate in any Nyquist zone of the converter (e.g., first, second, third, etc.) The appropriate Nyquist zone can be selected using a set of logic inputs, which control the required FIR coefficients.

AFB Design Example

The AD12400 is the first member of a new family of Analog Devices products that leverage time interleaving and AFB. Its performance will be used to illustrate what can be achieved when state-of-the-art ADC design is combined with advanced digital post-processing technologies. Figure 11 illustrates the AD12400's block diagram and its key circuit functions. The AD12400 employs a unique analog front-end circuit with 400-MHz input bandwidth, two 12-bit, 200-MSPS ADC channels, and an AFB implementation using an advanced *field-programmable gate array* (FPGA). It was designed using many of the classical matching techniques discussed above, together with a very low jitter clock distribution circuit. These key components are combined to develop a 12-bit, 400-MSPS ADC module that performs very well over 90% of the Nyquist band and over an 85°C temperature range. It has an analog input bandwidth of 400 MHz.

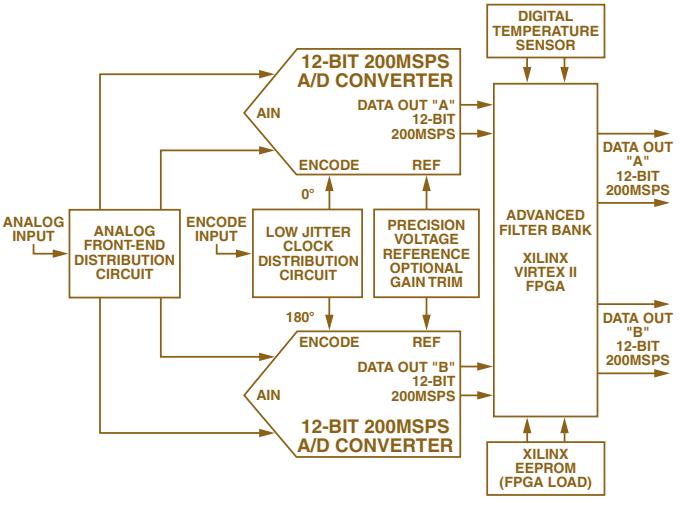

Figure 11. AD12400 block diagram.

The ADCs' transfer functions are obtained using wide-bandwidth, wide-temperature range measurements during the manufacturing process. This characterization routine feeds the ADCs' measured transfer functions directly into the AFB coefficient calculation process. Once the ADCs have been characterized, and the required FIR coefficients have been calculated, the FPGA is programmed and the product is ready for action. Wide bandwidth matching is achieved using AFB's special FIR structure and coefficient calculation process. Wide temperature performance is achieved by selecting one of the multiple FIR coefficient sets, using an on-board digital temperature sensor.

The true impact of this technology can be seen in Figures 12 and 13. Figure 12 displays the *image-spur* performance across the first Nyquist zone of this system. The first curve in Figure 12 represents the performance of a 2-channel time-interleaved system that has been carefully designed to provide optimal matching in the layout. The behavior of the image spur in this curve makes it obvious that this system was manually trimmed at an analog input frequency of 128 MHz. A similar observation of Figure 13 suggests a manual trim temperature of 40°C.

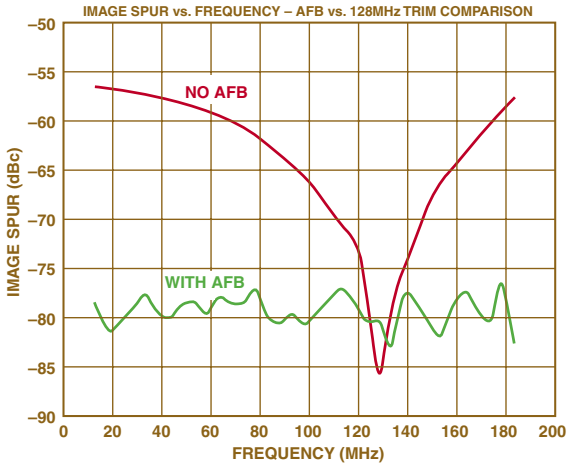

Figure 12. Performance of a manually trimmed system "before and after" AFB compensation over the frequency range.

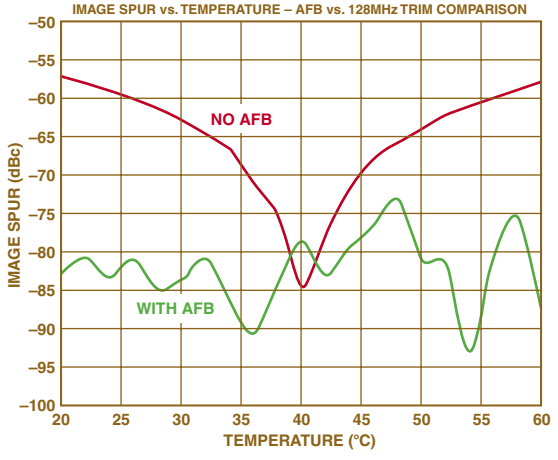

Figure 13. Performance of a manually trimmed system "before and after" AFB compensation over the temperature range.

Despite a careful PCB layout, tightly matched front-end circuit, tightly matched clock-distribution circuit, and common reference voltages used in the AD12400 ADC, the dynamic range degrades rapidly as the frequency and/or temperature deviates from the manual trim conditions. This rapid rate of degradation can be anticipated in any two-converter time-interleaved ADC system by analyzing some of the sensitive factors affecting this circuit. For example, the gain-temperature coefficient of a typical high-performance, 12-bit ADC is 0.02%/°C. In this case, a 10°C change in temperature would cause a 0.2% change in gain, resulting in an image spur of 60 dBc (see Equation 1). Considering just this single ADC temperature characteristic, the predicted image spur is 3 dB worse than the 30°C performance displayed in Figure 13.

By contrast, the dynamic range performance shown in these figures remains solid when the AFB compensation is enabled. In fact, the dynamic range performance surpasses the 12-bit level across a bandwidth of nearly 190 MHz and a temperature range of 40°C. Another significant advantage of this approach is that the temperature range can actually be expanded from the 20°C to 60°C range shown to 0°C to 85°C by using additional FIR coefficient sets—as embodied in the AD12400.

CONCLUSION

Time interleaving is growing into a significant trend in performance enhancement for high-speed ADC systems. Advanced digital post-processing methods, such as AFB, provide a convenient solution to the tough channel-matching requirements at resolution levels that were not previously achievable for time-interleaved systems. When combined with the best ADC architectures available, advanced DSP technologies, such as AFB, are ready to take high-speed ADC systems to the next level of performance and facilitate greatly improved products and systems in demanding markets such as medical imaging, precise medicine dispensers (fluid flow measurement), synthetic aperture radar, digital beam-forming communication systems, and advanced test/measurement systems. This technology will result in many breakthroughs that will include 14-bit/400-MSPS and 12-bit/800-MSPS ADC systems in the near future.

ACKNOWLEDGEMENT

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