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Using Self-Calibration to Improve Performance of Ultra High-Speed Data Converters

Application Note AN-1727

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The ADC08xxxx family of Giga Sample Per Second (GSPS) A/D Converters (ADCs), incorporates sophisticated self-calibration circuitry. This application note gives the system designer a comprehensive description of how to use this feature. The device datasheets contain specific details about the self calibration features.

The Self-Calibration Scheme

Since calibration is essential to performance, the device performs self-calibration upon each power-up. In addition, the device allows the user to manually command the device to perform self-calibration as required. Typically this would be done when the system temperature has changed beyond a threshold that system design has established. Since ultimately it is the device's own temperature that affects its performance, an on-chip diode can be connected to an external temperature sensor for device temperature monitoring. National recommends the LM95221 temp sensor for this purpose.

The calibration procedure takes roughly 1–2 msec to complete, depending upon the CLK frequency and the specific device (refer to the device datasheet). In addition, at power-up only, the device inserts a much longer delay before starting the self-calibration process. This delay can be relatively short (tens of milliseconds) or relatively long (few seconds) and is user-selectable. The purpose of this delay is to allow the power-supply and other variables to stabilize. Also, when the device is configured in extended control mode the longer delay is not available (i.e. configured through the serial interface).

The CalRun pin always indicates whether the device is in self calibration mode or operating normally.

Performing Self-Calibration

Self-calibration is part and parcel of the "normal" operation of the device. As such, the device's operating conditions should be as stable and as close to "normal" system conditions as possible during calibration. The power supply, temperature and all inputs must be within the operating conditions stated in the datasheet and stable. Then, for greater calibration accuracy, the operating conditions should be as close to their operational state as possible.

In order to allow the conditions to stabilize, a certain amount of time delay would be necessary. The system engineer must decide what this time delay is for their system — which may vary from about 1–2 seconds to 10s of seconds. If longer delay is required then the CAL input pin can be used to further delay the start of the calibration cycle. The user does this by holding the CAL pin high during power up and keeping it high for as long a delay as desired. The device will wait until the CAL pin is cycled low and then high again before initiating the power-up calibration cycle.

The CAL input "low-then-high cycle" timing requirements can be found in the AC Electrical Characteristics table in the datasheet. Other than inhibiting the calibration from occurring, this scheme does not interfere with the rest of the device's behavior. Although delayed in this manner with the CAL input, this should still be considered the power-up calibration that must occur before proper performance can be expected.

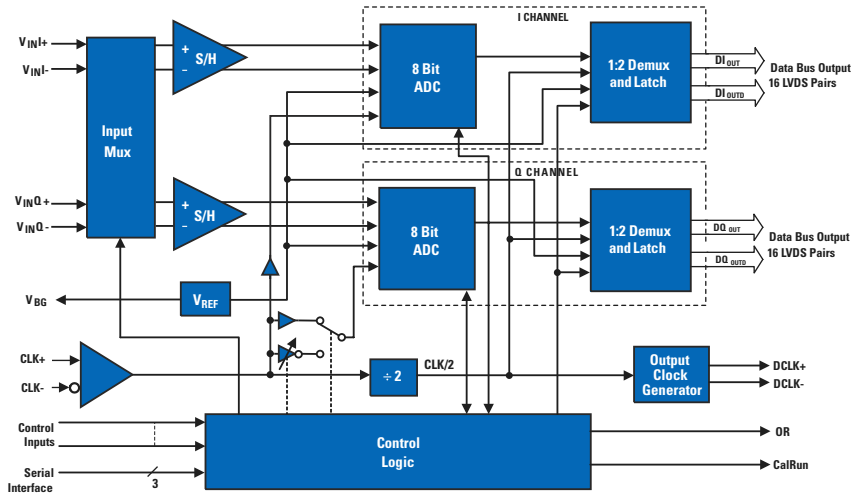

Figure 1. Block Diagram of ADC08D1500

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To obtain accurate calibration, it is important for key variables to stabilize. In addition to environmental conditions (supply and temperature), the device's other operational conditions have to be stable as well.

- The clock input must be stable (this includes not performing DCLK_RST);
- The analog input is within the specified range, but the frequency is not important — including DC;
- The control/configuration settings must not be disturbed during calibration;
- The device must be in normal mode (not DES mode) for the ADC08D500/1000/1500, but not for the ADC08D1020/1520 or ADC083000/B3000;
- The control registers must not be accessed, though the SCLK may be active;
- The device should not be in power-down mode when starting calibration, nor enter power-down while calibration is underway

Device Behavior During Self-Calibration

In addition to the interruption to the signal processing path, the device has other effects during the calibration cycle:

1. The digital outputs are disabled.
2. The DCLK output is also disabled on certain devices of this family.

The DCLK output of the device is generally intended for data capture purposes only. The fact that it is interrupted means that the ASIC/FPGA device should not rely on it as a clock signal for its logic beyond the capturing logic. However, for those applications where it is essential to use the DCLK signal as a general purpose clock, the newer devices of this family give the user the control to keep the DCLK running during calibration. The cost of this is that the analog input termination resistor (Rterm) is not calibrated if the DCLK is kept active — causing the Rterm value to be slightly less accurate. Thus, this option should be used only for subsequent on-command calibration cycles.

On the devices, the Resistor Trim Disable (RTD) bit in the Extended Configuration Register controls whether the DCLK is allowed to stop ion Register controls whether the DCLK is allowed to stop during calibration or not. The default state of this bit (at power-up) is DCLK will be stopped and Rterm will be trimmed during calibration. At the time of power-up calibration, the user must leave this bit in its default state and expect the DCLK to stop during calibration. The user may clear this bit in order to keep the DCLK running during on-command calibration cycles.

Performance Effects

Guaranteed performance in the datasheet is based on the device being correctly calibrated. As with any electronic circuitry, the device exhibits some amount of performance degradation as environmental conditions change after calibration. The system parameter that usually affects performance is temperature. On-command self-calibration should be performed when temperature change exceeds a threshold. This threshold should be determined during the design process. The following observations, from limited data, may be useful to the user.

1. The ENOB performance of the device has been seen to degrade by 0.35 bits over a temperature range of 55°C (from +45°C to +100°C die temperature).

2. Gain error of 2% across an 80°C temperature range (from +20°C to +105°C die temperature) has been observed.

3. If the DCLK is enabled to run during calibration and the Rterm is not calibrated after the required power-up calibration, the Rterm value due to temperature effects alone is expected to vary by 1% from 0°C to +120°C die temperature.

A reasonable temperature variance threshold to trigger a self-calibration cycle could be in the 20 to 30°C maximum range.

Conclusion

The user is provided a great deal of flexibility to allow these devices to provide reliable performance over a wide range of temperature. By maintaining the device's temperature feedback, the sampling can be adjusted in subtle ways to allow these ADCs much better accuracy. Design solutions strive for better performance and self-calibration enables a better thermal performance. ■

For Additional Design Information

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