BY BONNIE BAKER

When undersampling, clock jitter *does* matter

In undersampling applications, such as wideband receivers, cellular base stations, and communications receivers, the undersampled signal has a relatively low-frequency bandwidth—with the help of the Nyquist Theorem and slower clocks to the converter. However, the carrier frequency for this signal frequency is high enough so that timing inconsistencies, such as clock jitter (or phase noise) and ADC aperture jitter, can increase noise as the signal goes through the ADC. Large amounts of jitter make the ADC block unusable for this type of system.

The noise sources in this type of application include the quantization noise of the converter (or the ac differential-nonlinearity error), the internal converter thermal noise, and the system jitter. The ADC quantization noise and thermal noise have a direct effect on the converter's SNR (signal-to-noise ratio), which is under your control only as you select the converter. The contributors to the system jitter are the aperture jitter of the sample-and-hold switch at the input of the ADC and the sampling-clock jitter. Aperture jitter is the sample-to-sample-variation timing of the ADC's input switch. The product data sheet indicates the aperture-jitter specification of your undersampling ADC. Clock jitter is an artifact of clock variation from cycle to cycle. You combine these two uncorrelated jitter-noise sources using the root-sum-square formula, or $t_{JITTER}=\sqrt{(t_{JCLOCK}^2+t_{JADC}^2)}$ in rms picoseconds, where t_{JITTER} is the total jitter of the system, t_{JCLOCK} is the jitter from the external ADC clock, and t_{JADC} is the jitter of the ADC-input-sampling switch. You cannot change your application circuit to improve the ADC's aperture jitter. However, several techniques can improve the clock jitter.

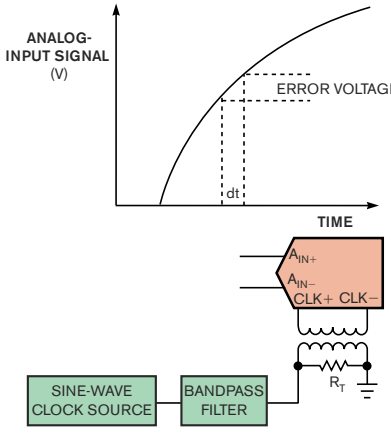

Figure 1 A variation of phase or jitter in the converter's clock input causes a deviation in the sampling time of the ADC-analog-input signal. This deviation produces degradation in conversion accuracy, which you quantify with the converter's SNR performance.

In this application, the external clock controls the sampling frequency or speed of successive conversions. Assuming the analog-input signal is void of phase shifts, clock jitter causes sampling-time uncertainty (**Figure 1**). This uncertainty affects the SNR of the conversion. The theoretical impact on SNR, due to jitter from the clock as well as from the ADC-sampling mechanism, is $SNR\ (dBc)=-20\log_{10}(2\pi f_{IN}t_{JITTER})$, where f_{IN} is the analog-input frequency.

Undersampling systems requires a clock with low jitter or phase noise to drive the ADC. These clocks can be digital or sinusoidal. Digital clocks have a fast slewing transition, which facilitates the reduction of clock jitter. However, the fast edges of digital clocks create wideband noise due to the complexity of the square wave's frequency content, producing wideband noise that aliases back into the signal bandwidth. Sinusoidal clock signals may be alternatives to the digital-clock option, depending on your application layout and implementation. However, they usually have higher rms near-band jitter. (Most ADC vendors provide clock recommendations for their converters.)

Using differential versus single-ended inputs is another clock alternative with most undersampling ADCs. Single-ended clocks must have a clock slope of approximately 1V/nsec or better. Single-ended inputs are not appropriate connections for sine-wave clocks. In addition, you need limits to the voltage swing of the single-ended clock. Otherwise, the clock signal bumps into supply rails, turning on internal protection devices. Differential-clock signals double the voltage range of the clock. The converter also does some common-mode rejection of noise signals.

So, when planning your clock strategy for your undersampling ADC, you should take into account your clock phase noise or jitter. The clock source you choose need not be expensive—only low noise. EDN

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