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Using Clock Conditioners to Clean Recovered Clocks

Application Note AN-1734

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Introduction

In wired communications, there is a need to recover a clock from the data. Having the clock encoded in the data eliminates the need for a wire to transmit the clock, and also helps with skew issues. This application note investigates the impact of cleaning the clock at every stage, as well as at the end.

Serializer-Deserializer (SerDes) parts such as the SCAN25100 can take a set of parallel data and convert it into a series set of data that can be sent on a single wire. Another SerDes part at the receiving end can be used to generate the parallel data from the received series data. This is a very effective technique for sending data over long distances, but the recovered clock will have added phase noise (jitter) relative to the original clock used to generate this serial data.

When data is transmitted over long cables, the signal will become weaker and the Signal-to-Noise Ratio (SNR) will be less. If the length of cable is too long, it will not be possible to recover the clock. For this reason, a SerDes part can be used as a repeater, where it receives the serial data, recovers the clock, and then re-clocks the data using the recovered clock or a jitter-cleaned clock. In this way, data can be transmitted over much longer distances.

Clock conditioners, such as the LMK03000C, can be used to take this dirty (higher phase noise/jitter) clock and generate a clean clock (lower phase noise/jitter) that is the exact same frequency.

Jitter Calculation

Phase noise is more descriptive than jitter. Jitter can be calculated from phase noise, but not the other way around. Given a phase noise profile, carrier frequency, and lower and upper limits for integration, the jitter can be calculated as follows:

$$Jitter = \frac{\sqrt{\int_{LowerLimit}^{UpperLimit} 10^{PhaseNoise(Offset)/10} \cdot dOffset}}{2 \cdot \pi \cdot Frequency}$$

From this formula it is apparent that minimizing jitter is a matter of minimizing the area under the phase noise curve.

Choosing the Optimal Loop Bandwidth

The loop filter can be implemented with one external resistor and two external capacitors. These components can be chosen to adjust the loop bandwidth of the system. At frequencies below the loop bandwidth, noise from the 30.72 MHz recovered clock pass through, but the Voltage-Controlled Oscillator (VCO) noise is attenuated. At frequencies above the loop bandwidth, the noise of the 30.72 MHz recovered clock is attenuated, but the VCO noise passes through. Therefore, the optimal design choice for the loop bandwidth depends on the noise of the VCO and recovered clock.

In this case, the VCO used was the internal VCO of the LMK03001C clock conditioner. The recovered clock was from the SCAN25100, and is shown for one hop, two hops, or three hops in *Figure 1*. Normally, one finds the frequency at which the free-running VCO noise is equal to the other in-band noise sources and adds 25% to this in order to find the optimal jitter. However, in the case of dealing with recovered clocks, it makes sense to round this down a little bit, since the phase noise may vary with the number of hops and data.

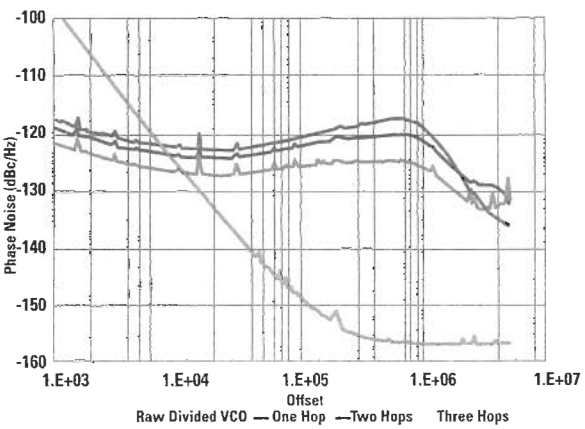

Figure 1. Determining which Loop Bandwidth to Use

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Implementation

In order to show all these techniques, three hops with the SCAN25100 were used and the final stage was cleaned with the LMK03001C clock conditioner. From *Figure 1*, we see that the optimal loop bandwidth for three hops is about 7.2 kHz. However, the choice of three hops is arbitrary, and perhaps more hops could be used.

For this reason, a narrower loop bandwidth of 4 kHz was used to be sure that this solution would be robust if more hops were used.

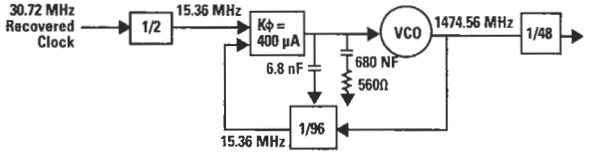

Figure 2. LMK03001C Setup for Cleaning a 30.72 MHz Recovered Clock

Note that in *Figure 3*, the recovered clock has lower jitter. If one uses an integration limit of 100 Hz to 5 MHz, then the recovered clock has a jitter of 5.3 ps and the cleaned recovered clock has a jitter of 1.4 ps.

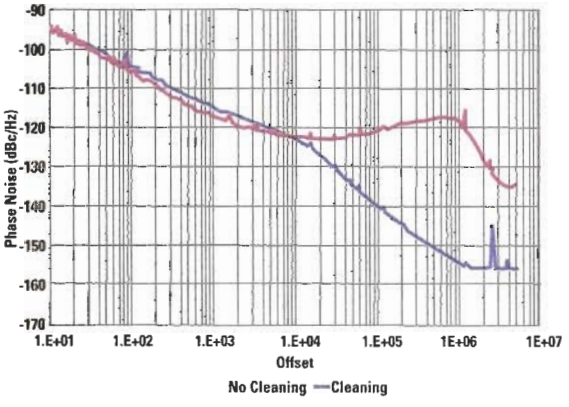

Figure 3. LMK03001C Setup for Cleaning a 30.72 MHz Recovered Clock

Note that in the range of 100 Hz to about 8 kHz, the clock conditioner actually adds a little phase noise. This is because the VCO noise is contributing here. If this is a major concern, the loop bandwidth should be increased. This design was done with a wider loop bandwidth as well and the jitter was reduced to around 900 fs.

Conclusion

The SCAN25100 and LMK03001C families are an excellent choice for sending and recovering data. In a multi-hop architecture, the SCAN25100 has a built-in reference clock that makes it such that there is no reference clock necessary for any of the SCAN25100 parts, except for the first in the series that is used to serialize the data.

The LMK03001C is an ideal choice for cleaning this clock, since it has excellent phase noise performance at higher offset frequencies. The noise of the reference clock of the SCAN25100 deteriorates primarily at higher phase noise offset frequencies when increasing the number of hops. So filtering at every hop, as opposed to just the last hop, only gives a marginal benefit to jitter cleaning, since this noise will all be filtered at the last hop. However, there could be reason to clean the clock at every hop if there was a need to use this recovered clock at every hop, instead of just at the very end.

The LMK02000 clock conditioner allows the user to supply a VCXO in order to obtain improved phase noise performance close to the carrier, if that is required for system reasons other than data clocking. ■

For a more detailed version of this article, including information on recovered clocks, visit:

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