Two-phase clock features nonoverlapping outputs

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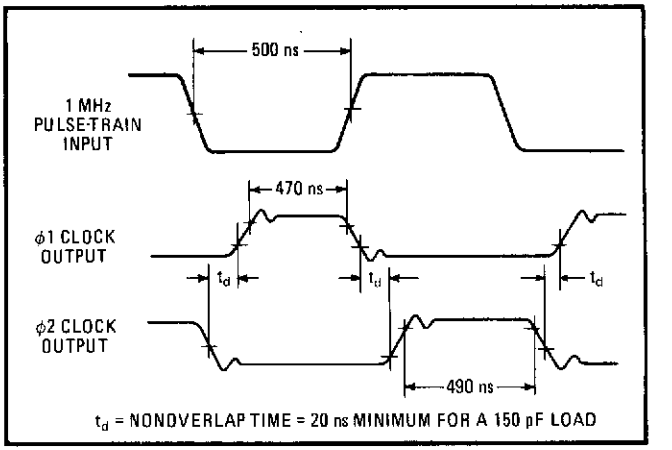
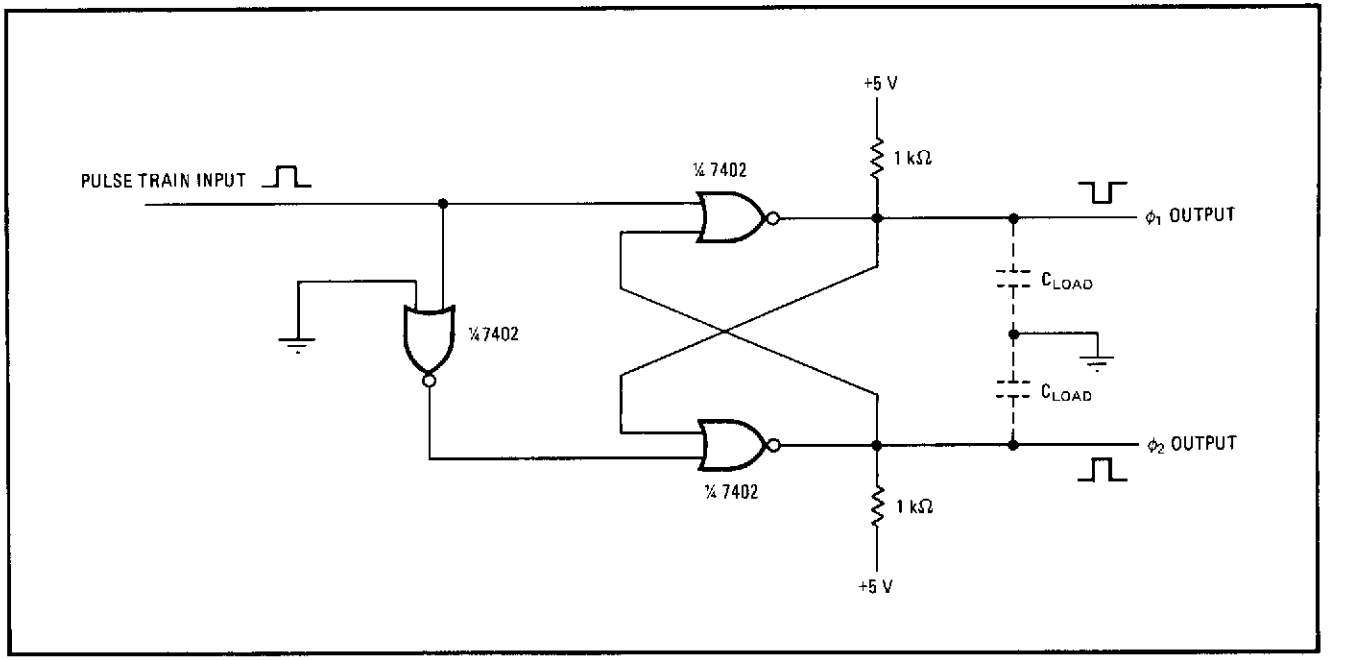
A reliable, two-phase clock signal with nonoverlapping outputs—the kind that is an absolute must for the Motorola 6800 and other microprocessing units—can easily be derived from a pulse train input. This design avoids overlap by exploiting the propagation delays inherent in transistor-transistor logic, and it uses only one integrated circuit.

As shown in the schematic of Fig. 1, a pair of two-input NOR gates in the 7402 chip are wired as an R-S flip-flop to provide the split-phase outputs. The propagation delay of the gates depends on their capacitive loading; it is typically 10 nanoseconds with a 15-picofarad load, increasing to 20 ns with a 150-pF load. As specified in the Motorola 6800 applications manual, the clock inputs of the central processing unit are capacitive, with maximum values of 160 pF but typically 110 pF.

With a 1-megahertz, 50%-duty-cycle input pulse train, this circuit produces a ϕ_1 output 470 ns in duration, a ϕ_2 output 490 ns in duration, and 20 ns of nonoverlap, as shown in Fig. 2. The duration of the nonoverlap is independent of the input duty cycle. □



2. No overlap. With a 1-MHz, 50%-duty-cycle input signal, the ϕ_1 and ϕ_2 outputs have durations of 470 ns and 490 ns, respectively. The nonoverlap, which is dependent upon the propagation delay of the gates, is a function of load capacitance and varies from about 10 ns with a 15-pF load to 20 ns with a 150-pF load.



1. Phase splitter. Simple circuit derives two out-of-phase signals from oscillator input, with outputs suitable for clocking 6800 and other microprocessors that have strict timing requirements. Nonoverlapping of outputs is constant, regardless of input duty cycle.