

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Watch for Those Multiple Clocking Edges!

Q. How can I improve system performance when using multiple clocks?

A. A common problem that arises when using multiple clocks generated from the same source is noise—usually a spur popping out of the noise floor—because the single clock source is multiplied or divided into several versions of the same clock. Skewing the adjacent edges of each clock allows you to reduce the noise spur, or get rid of it completely, depending on the system's timing margin. This phenomenon indicates a time-variant system, in which corruption on the clock signal is related to the location of the interference in the time domain. The location of the interference is fixed, so the degree of clock corruption is proportional to the magnitude of the interference, just like in a linear system.

As an example, let's take two outputs of the AD9516 clock generator. One output, at 100 MHz, is connected to an ADC; the other, at 25 MHz ($1/4 \times f_{\text{SAMPLE}}$), clocks an FPGA. Rising and falling edges occur on both output clocks at nearly the same time. The result is a coupling effect, because two fast moving, high-bandwidth edges occur every 10 ns instead of one as desired. During this transition period, the noise—intrinsic or extrinsic—must be low, as jitter or noise can only corrupt the ADC's timing when present during the transition region of the clock. Making the edge faster (and hence the threshold region smaller) by increasing the slew rate will inevitably reduce the amount of time



that noise can be present during the threshold period, effectively reducing the amount of rms (root-mean-square) jitter introduced to the system. During the steady-state period of the clock—the high and low levels—the clock noise is irrelevant. Therefore, simply delaying either the 25 MHz or 100 MHz clock will spread them apart in time, moving the location of the interference. In other words, arrange for the transition edges of one clock to happen during the steady-state period of the other clock.

In essence, what is happening here is crosstalk-induced jitter (noise) from one trace to an adjacent trace. If one trace carries a signal, and a nearby parallel trace carries a varying current, a voltage will be induced in the signal trace; if it is a clock signal, the time at which the clock edge occurs will be modulated. This causes problems if these edges are taking place at nearly the same time.

**To Learn More About
Clock Distribution**

<http://dn.hotims.com/27753-101>



Contributing Writer
Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

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