Multiphase clock produces nonoverlapping pulses

by Glen Coers
Texas Instruments, Components Group, Dallas, Texas

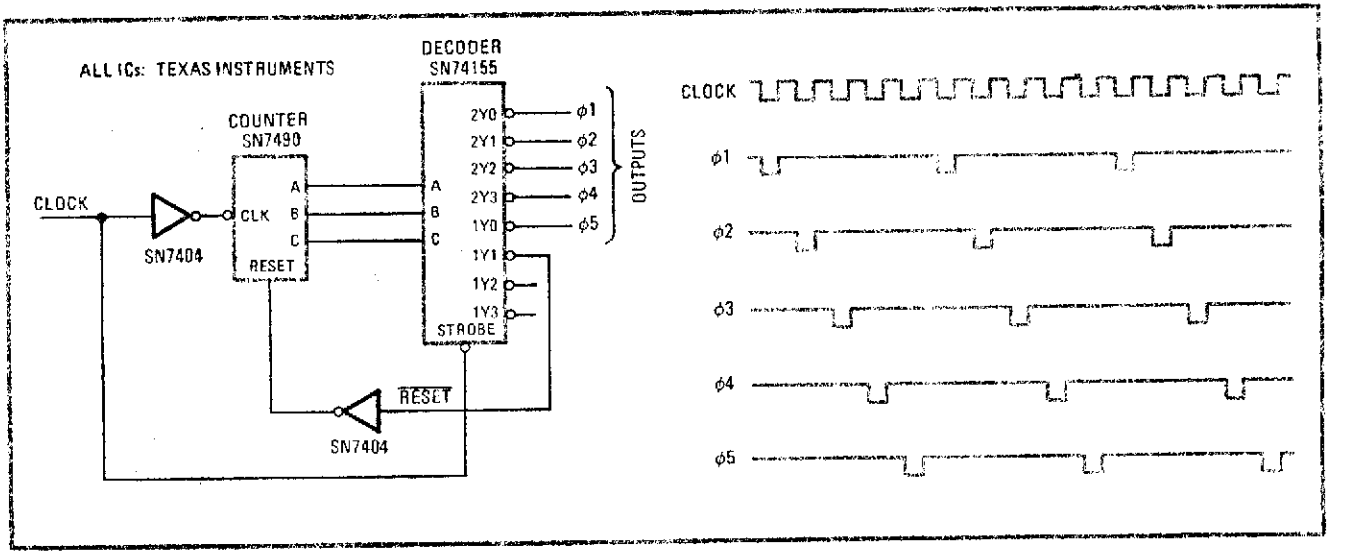
A multiphase clock pulse generator can be put together from a few IC packages by taking advantage of the versatility of an MSI TTL decoder/demultiplexer. The clock generator can be programed to produce from two to seven differently phased clock-pulse trains, and none of the pulse edges will overlap. Furthermore, the time between the pulses of the various clock phases is the same as the width of a single pulse. This means that each individual clock phase is well-defined, and there is no pulse-edge ambiguity, as with other clock-generating techniques.

An MSI decade counter is used with the MSI decoder/demultiplexer, which is connected as a three-line-to-eight-line decoder. Only three of the outputs of the decade counter are needed.

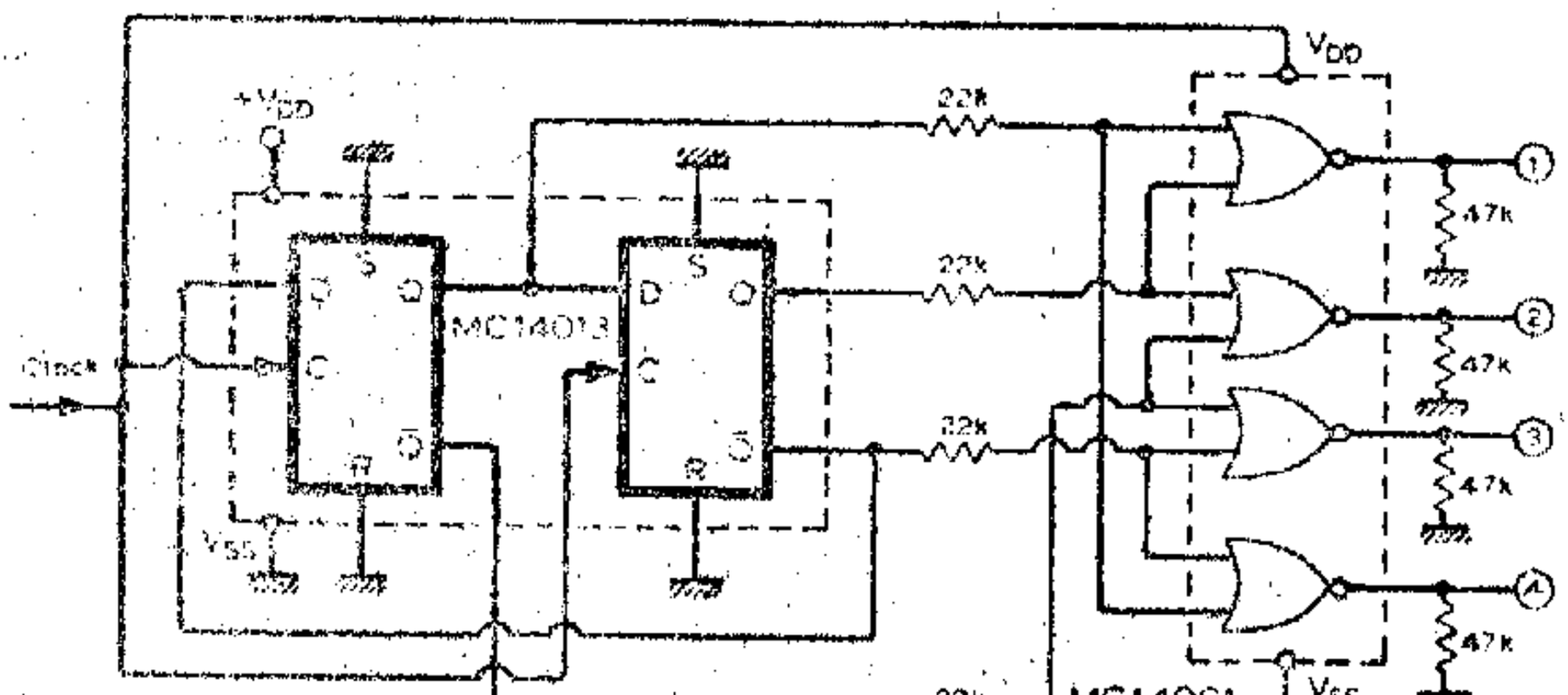
The number of clock phases is determined by the decoder output that is selected to reset the counter to zero. The counter's reset line is simply connected to the decoder's output line that is next in the sequence. As shown in the figure, a five-phase clock is produced by wiring the counter-reset line to the sixth decoder's output line.

The inverter at the input of the counter assures that the decoder is disabled when the count is changing and enabled after the data has stabilized. This eliminates the transients that can appear on the decoder's output lines when the counter is changing states. □

Programable clock. Two MSI devices—a decade counter and a three-line-to-eight-line decoder—can be wired as a simple multiphase clock generator. The circuit can produce from two to seven clock phases without any overlapping pulse edges. The number of clock phases is determined by connecting the counter's reset line to the decoder output line that is next in sequence. A five-phase clock is shown here.



MULTIPHASE CLOCK GENERATOR



Whenever sequential logic operations are to be performed, a multiphase clock generator is often required. The circuit shown, which uses only two CMOS ICs, was designed by Michel Burri of Motorola's Geneva applications laboratories. It will produce a pulse on each of the four output lines in turn. These pulses do not overlap one another.

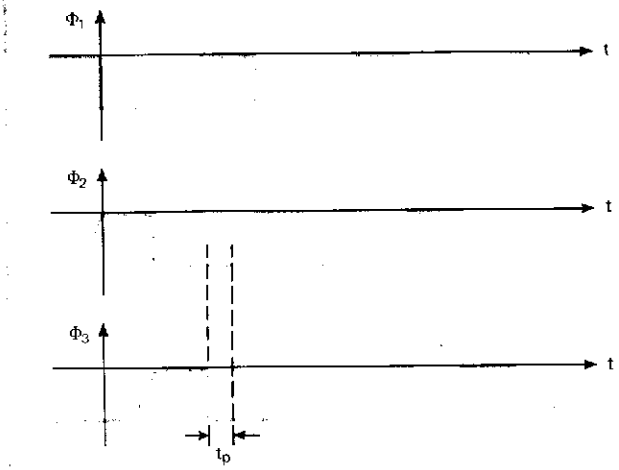
Operation of the circuit is self-evident from an examination of the schematic; however, it interesting to note that the po supply of the MC14001 is deri from the clock input. The maxim operating speed of this circuit is ab 1 MHz.

Generating overlapped clock phases for CCD array

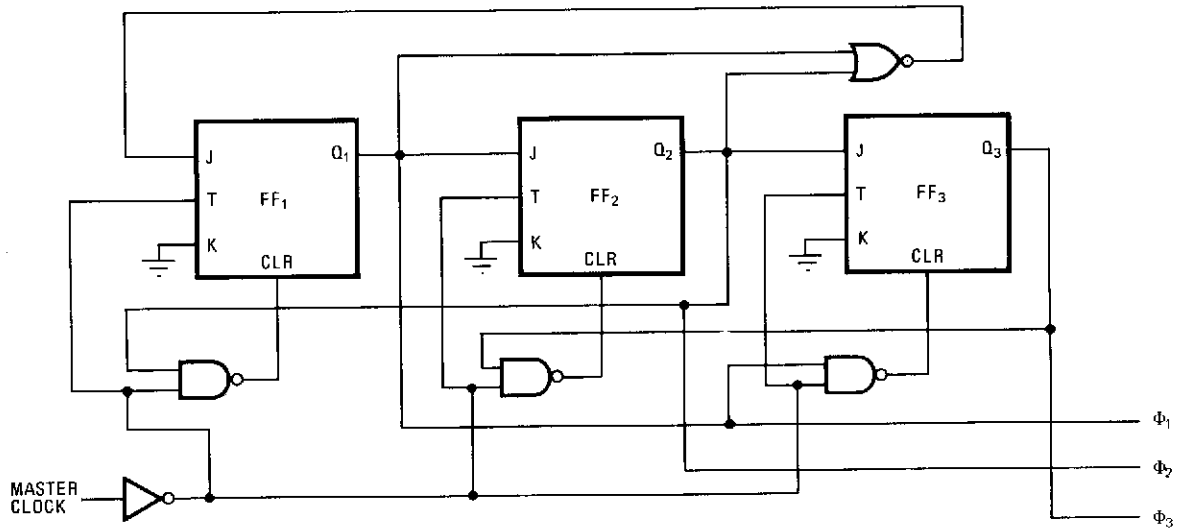
by Hans-Jörg Pfleiderer and K. Knauer,
Siemens AG, Munich, Germany

Arrays of three-phase charge-coupled devices require overlapped clock pulses (Fig. 1) for satisfactory operation. To generate these overlapped pulses, Fairchild Semiconductor, which produces the arrays commercially, suggests a rather complicated logic circuit in a report that it circulates.

But a less complicated circuit (Fig. 2) can also generate the train of overlapped pulses, as shown in the timing chart (Fig. 3). When the master clock pulse goes high, J-K flip-flop FF_1 turns on only if the outputs Q_1 and Q_2 are both low. With FF_1 on, Q_1 rises, opening the gate so that the rise of the next master clock pulse turns on FF_2, without affecting FF_1. However, with Q_2 up,



1. Overlap. Arrays of three-phase charge-coupled devices require overlapping pulse trains for proper operation. The logic to produce these trains does not have to be complicated—it need not involve more than three flip-flops and a few gates.

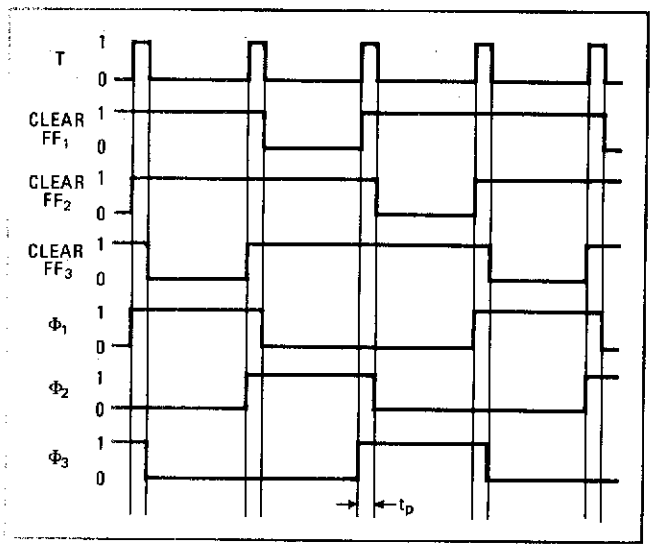


2. Pulse-train generator. When the master clock's pulse rises, one flip-flop turns on, gated by the state of the flip-flop before it. When the pulse falls, the preceding flip-flop turns off, this time gated by the state of the following flip-flop.

the fall of the master clock's pulse clears FF_1 via the CLR input of FF_1.

This approach—setting the output of each flip-flop high with the J input, provided the preceding flip-flop is already on, and setting it low with the clear input when the following flip-flop is on—is used for each of the three flip-flops. The width of the overlap is approximately equal to the width of the master clock's pulse, and the frequency of each waveform is one third that of the master clock's pulse. The circuit is self-correcting and also self-starting.

The same idea can also be used in driving the phase voltages for a two-phase CCD. □



3. Pulse timing. As the three flip-flops turn on and off (second, third, and fourth traces from top), their outputs overlap by the width of the clock pulse, minus circuit delays. The frequency of each waveform is one third that of the master clock's pulse.

Decoders drive flip-flops for clean multiphase clock

by Craig Bolon
Massachusetts Institute of Technology, Cambridge, Mass.

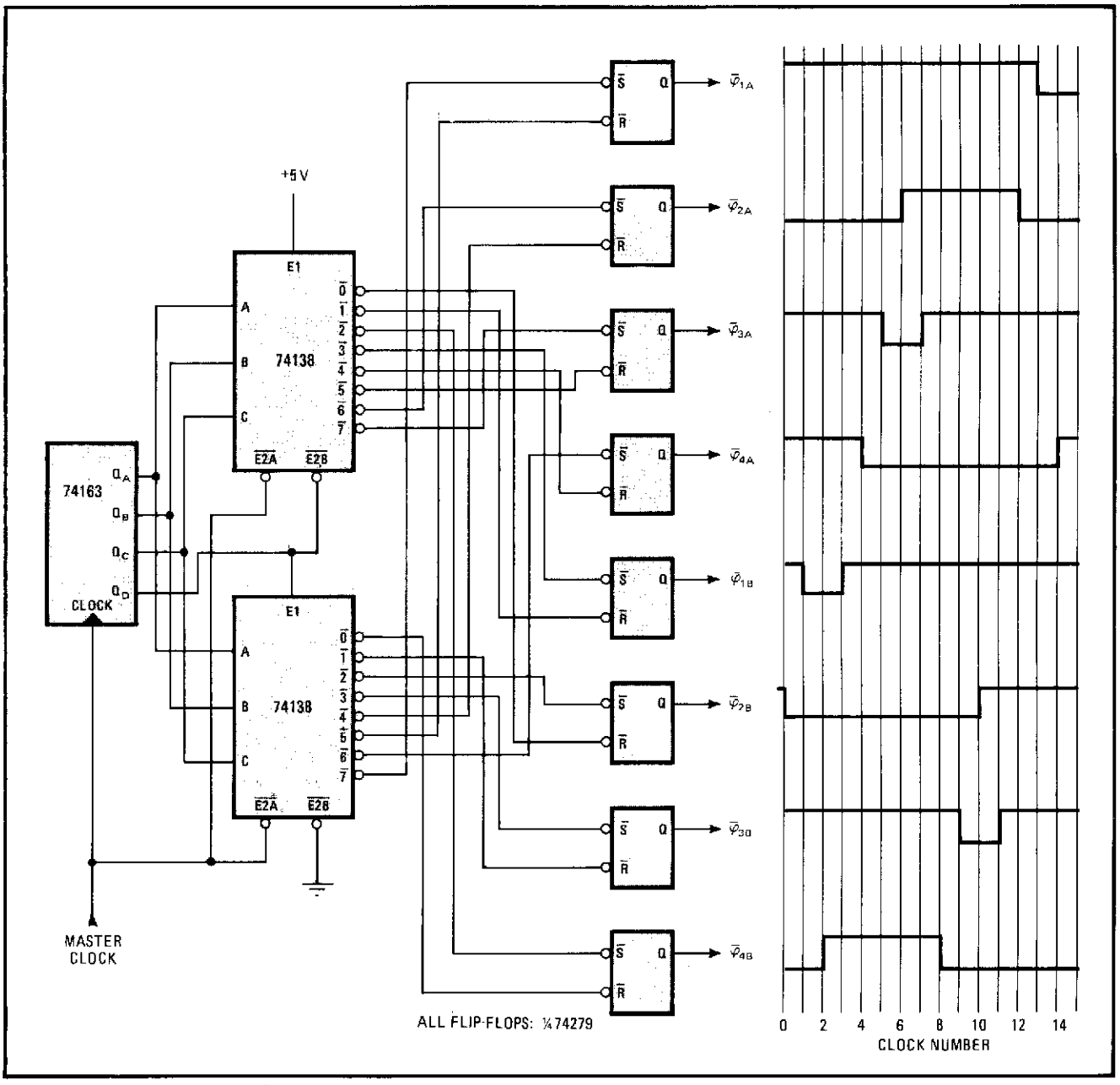
A multiphase clock suitable for driving circuits with strict timing requirements, such as charge-coupled-device memories, can be built with a counter, decoder, and set/reset flip-flops. This clock can generate any number of outputs at any duty cycle, yet never suffers from the drift and "glitches" encountered in most multiphase designs. Although each signal is phase-locked to a master clock, its timing and duty cycle can be set independently of the others, permitting great flexibility.

The figure shows a typical application—an eight-phase clock designed for driving parallel banks of Intel 2416 CCD memories. A master clock drives the 74163 synchronous 4-bit binary counter. The binary output is then presented to the combinational logic of two 74138 1-of-8 decoders.

The decoders count one pulse on the rising edge of each clock. The first decoder counts eight pulses (0–7) before its outputs are held high by the Q_D output of the binary counter. The second decoder is then enabled and counts an additional eight pulses, after which the 16-count sequence is repeated.

Each decoder output controls an R/S flip-flop by setting or resetting it at the desired moment. Thus, the master clock assures synchronous operation, and the strictly sequential nature of the decoder output keeps it glitch-free for all time.

The clock waveforms are shown to the right of the circuit. Phase 2A of the clock, for example, is generated by setting a flip-flop on count 6 of the 16-count cycle ($\overline{6}$ of the first decoder) and resetting it on count 12 of the cycle ($\overline{4}$ of the second decoder). The number of phases can easily be increased by expanding the binary counter and adding decoders and flip-flops. □



Multiphase clock and waveforms. Master clock can be stopped or started at any point in cycle without affecting the phase relationship at all. Skew in output waveforms can be limited to propagation delay of one gate, provided that edge-triggered flip-flops are used.

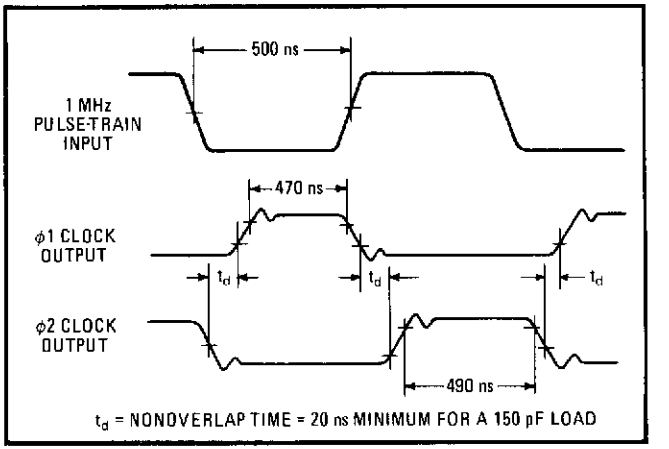
Two-phase clock features nonoverlapping outputs

by Neil Heckt
The Boeing Co., Seattle, Wash.

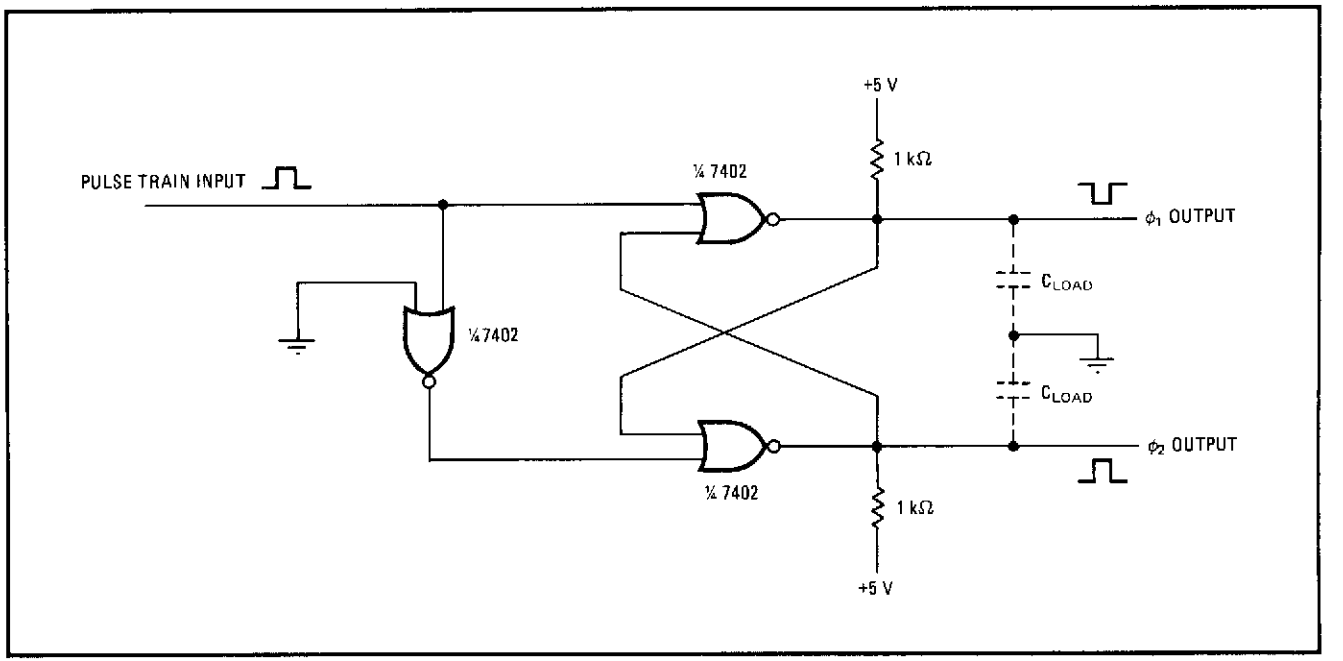
A reliable, two-phase clock signal with nonoverlapping outputs—the kind that is an absolute must for the Motorola 6800 and other microprocessing units—can easily be derived from a pulse train input. This design avoids overlap by exploiting the propagation delays inherent in transistor-transistor logic, and it uses only one integrated circuit.

As shown in the schematic of Fig. 1, a pair of two-input NOR gates in the 7402 chip are wired as an R-S flip-flop to provide the split-phase outputs. The propagation delay of the gates depends on their capacitive loading; it is typically 10 nanoseconds with a 15-picofarad load, increasing to 20 ns with a 150-pF load. As specified in the Motorola 6800 applications manual, the clock inputs of the central processing unit are capacitive, with maximum values of 160 pF but typically 110 pF.

With a 1-megahertz, 50%-duty-cycle input pulse train, this circuit produces a ϕ_1 output 470 ns in duration, a ϕ_2 output 490 ns in duration, and 20 ns of nonoverlap, as shown in Fig. 2. The duration of the nonoverlap is independent of the input duty cycle. □



2. No overlap. With a 1-MHz, 50%-duty-cycle input signal, the ϕ_1 and ϕ_2 outputs have durations of 470 ns and 490 ns, respectively. The nonoverlap, which is dependent upon the propagation delay of the gates, is a function of load capacitance and varies from about 10 ns with a 15-pF load to 20 ns with a 150-pF load.



1. Phase splitter. Simple circuit derives two out-of-phase signals from oscillator input, with outputs suitable for clocking 6800 and other microprocessors that have strict timing requirements. Nonoverlapping of outputs is constant, regardless of input duty cycle.