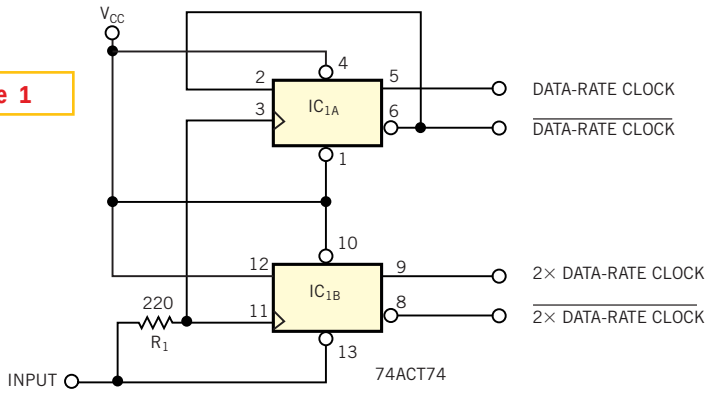
74ACT74 makes low-skew clock divider

Tom Napier, Consultant, North Wales, PA

Serial-data systems often generate an internal clock at twice the data rate for mid-bit sampling or for generating bi-phase codes. External equipment and some internal processes require a clock that runs at the data rate. Simply dividing the twice-rate clock with a flip-flop generates a data-rate clock that is skewed by one logic delay with respect to the input. This delay can be a significant fraction of the bit period. You can use specialized PLL-based low-skew divider chips to deal with this problem, but these chips have a limited frequency range and are not designed to follow rapid changes in the data rate.

Figure 1



The 74ACT74 dual flip-flop generates two clock rates with negligible skew.

The circuit in **Figure 1** uses a dual flip-flop, the 74ACT74, to generate both clock rates as well as both clock polarities with negligible skew. One half of the chip, IC_{1A}, acts as a normal divide-by-two circuit. The other half, IC_{1B}, tracks the input clock because the input's leading edge triggers IC_{1B} high and the input's trailing edge resets IC_{1B}. The divider transitions are synchronous within a few hundred picoseconds with the positive transitions of the twice-rate clock that the chip's other half generates. This circuit works with inputs from a few hertz to more than 100 MHz.

Without R_1, the input removes the reset from the twice-rate flip-flop at the same moment as the input clocks this flip-flop on. Theoretically, this setup is allowable because the 74ACT74's reset-recovery time is specified as 0 nsec. In practice, a resistor in the 100 to 500V region, in conjunction with the chip's input capacitance, delays the clock inputs slightly and adds a useful safety margin. (DI #2282)

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