C-MOS decade divider clocks bucket-brigade delay line

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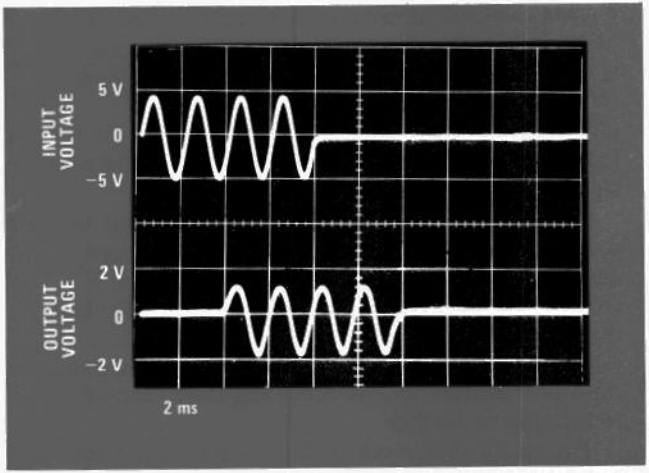
The bucket-brigade analog shift register is a charge-transfer device that can delay an input signal by a fixed or variable time. A TCA350 MOS bucket-brigade shift register, which has 185 stages, delays the signal by a time $t = 185/2f_c$, where f_c is the clock frequency. The clock frequency must be considerably higher than the signal frequency f_s for sampling and filtering reasons (f_c must be filtered from f_s at the output), so the maximum signal delay is about $10/f_s$. A TCA350 was used to delay 1-kilohertz tone bursts, as illustrated in Fig. 1, for measurements of distortion and insertion loss.

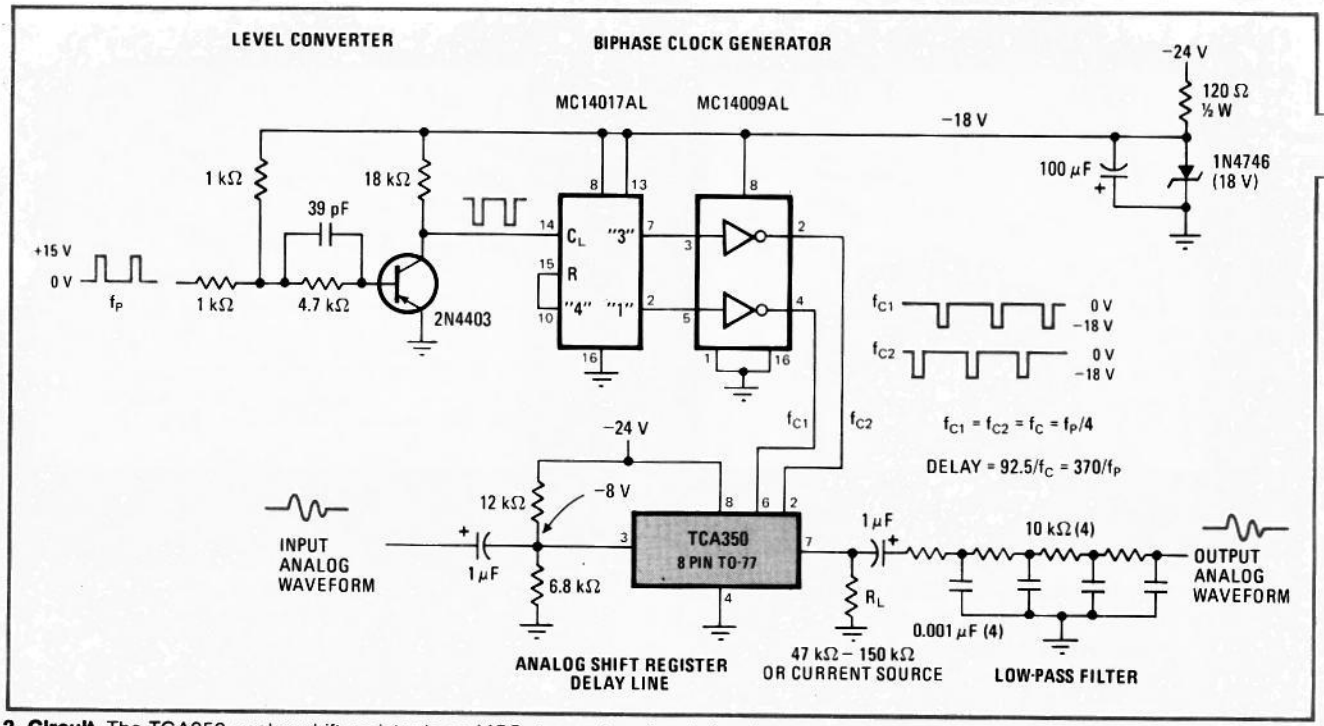
The TCA350 requires two clock-pulse trains of -18 volts; both are at frequency f_c, but they are separated in phase by 180°. [The function of the biphase clock in the charge transfer process is described in *Electronics*, June 21, 1971, p. 58.] A drain supply of -24 V and an input bias voltage of -8 V are also required. Figure 2 shows the circuit for the shift-register delay line, complete with clock generator and output filter.

In this circuit, an externally generated train of positive pulses at frequency f_p is applied to the 2N4403 transistor switch/level-converter, which produces negative pulses suitable for driving the biphase clock generator. The generator, a divide-by-four circuit that uses an MC14017AL C-MOS divider, is biased at -18 V and therefore can drive the TCA350 directly. It generates two non-overlapping pulses at $f_c = f_p/4$, separated by 180°. An MC14009AL C-MOS hex buffer inverts the clock pulses.

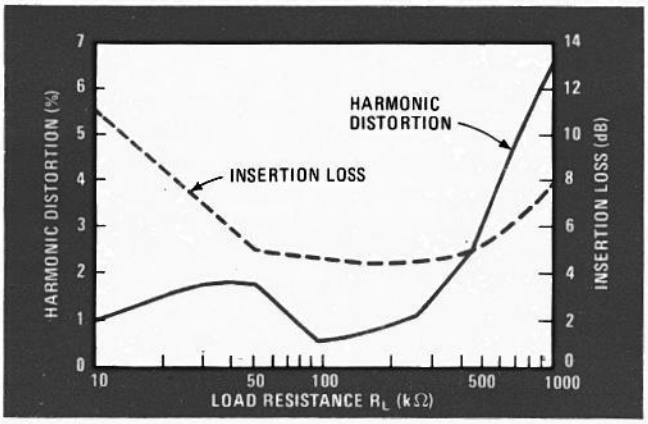
The output from the delay line consists of the delayed input signal superimposed on a clock-generated waveform. The output wave that is generated by the clocking pulses has an rms value of 3 V, and its frequency spectrum is integral multiples of f_c. A filter is needed to re-



1. Delay. Dual-trace scope photo shows 2-millisecond delay of 1-kHz tone burst in bucket-brigade delay line. Output has been filtered to remove clock-frequency components. Delay is inversely proportional to clock frequency; here $f_c = 46.25$ kHz.



2. Circuit. The TCA350 analog shift register is an MOS charge-transfer device that requires two clock inputs. Clocks of required amplitude and phase relationship are generated by C-MOS divider plus inverters from a conventional input pulse train. Low-pass filter removes clock frequencies from output waveform. Note dc bias at input of delay line. Cascaded shift registers can delay signals for tens of milliseconds.



3. Load carefully. Harmonic distortion and insertion loss in circuit depend upon value of load resistor R_L, as shown. Data assumes that f_s = 1 kHz, f_c = 46.25 kHz, and input signal = 0.77 V rms.

ject the clock frequency and its multiples; the more rejection the filter provides at f_c, the better the wideband signal-to-noise ratio is.

Of course, if f_c is so high that the following system cannot detect it, the filter requirements are not as stringent. For the four-section RC filter shown in Fig. 2, the clock-frequency energy is down about 50 decibels from the maximum allowable output signal within the low-pass filter passband. If a more elaborate filter such as a multipole active filter is used, the clock energy may be reduced even further.

The cutoff sharpness of the low-pass filter determines the maximum amount of delay realizable because a sharp cutoff allows a lower f_c. With the four-section RC filter shown, the maximum delay before signal degradation is about 2 milliseconds. The minimum delay is about 180 μs. The longest practical delay is about 18 ms. With such a long delay, however, the signal is less than 500 hertz. Since the delay changes with clock frequency, the worst-case f_c must be determined when calculating the s/n ratio of the delay line.

The usable dynamic range of the shift register also depends upon the filter response and acceptable s/n ratio. The dynamic range of the shift register is greater than 70 dB when a sharp-cutoff filter is used to remove the clock frequency. The analog shift register tracked within 1 dB as the input signal level changed from 3 V to less than 300 μV. The tracking error was measured in a filter bandwidth of 200 Hz, centered at 2 kilohertz. For input voltages above 3 V rms, the harmonic distortion exceeds 4%. For input amplitude levels of less than 0.5 V rms, the distortion is less than 0.5%. At higher input levels, clipping of signal peaks causes a distortion that is a nonlinear function of the input level.

The output stage of the TCA350 is a source follower that must be terminated in either a load resistor R_L or a constant-current load of about 0.5 milliampere. The relationship between harmonic distortion and load resistance is shown in Fig. 3; note that there is an optimum value for R_L. The distortion curve reflects a 0.2% distortion in the input signal plus the nonlinearity of the bucket brigade. If a current source is used in place of the load resistor, the current should be adjusted for minimum distortion.

Figure 3 also indicates that the attenuation of the input signal varies between 4 and 11 dB as the size of the load resistor is changed. □

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