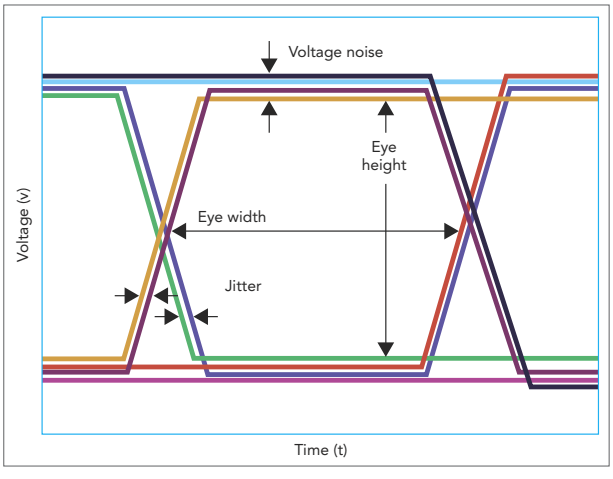
THE DATA DETECTIVE

Digital Signals Arrive on Time

Clock signals comprise rising edges (logic-low to logic-high transitions), and falling edges (logic-high to logic-low transitions). A clock signal can exist as square waves with a regular period and duty cycle or as a continuous series of periodic pulses. The latter type of signal can trigger a latch to accept data, interrupt a microcontroller, and so on. Regular clock waveforms govern the timing of microprocessor-based controllers, communication systems, memory chips, and other devices that perform operations at regular intervals. Depending on the clocked device, either a rising or a falling clock-signal edge causes an action. A device such as a double data-rate (DDR) memory uses both clock edges to trigger actions.

Clock signals do not cause instantaneous actions, though. A memory device, for example, requires the presence of unchanging data during a fixed amount of time, called the set-up time (t_{su}), prior to the arrival of a clock signal. The data must then remain stable for a specified hold time (t_H) after the clock-edge transition. These times, specified in chip manufacturers' data sheets, ensure designers know the timing requirements for the data and clock signals input to a device. A hand-drawn timing diagram may show the theoretical action of clocked circuits, but the design of complex circuits requires simulations that account for timing values such as t_{su} and t_H.



In this eye diagram, the overlaid samples of all 3-bit states show how jitter and voltage noise appear on a clock signal. Many communication signals must conform to standard templates that define minimum eye values (colored lines exaggerated for emphasis).

Unfortunately, clock signals come with imperfections such as jitter and drift. Drift occurs when the period of two clocks differs slightly over time. These slight timing differences can accumulate and affect a system adversely. For example, assume researchers have two data-acquisition devices that each supply a 100-MHz clock. Even if the two devices are synchronized to start together perfectly, over time one device may begin to run slightly faster than the other due to circuit imperfections or due to an external factor such as temperature. That difference badly skews the data the researchers expect will align perfectly in time. Timing techniques can reduce or eliminate drift.

Jitter represents a slight deviation in the timing of a signal's edges during a clock cycle, and it can arise from signal cross-talk, switching transients, and the effect of other signals. Engineers generally measure jitter as a time difference between the clock signal of interest and a reference clock signal at their zero-crossing points. Jitter measurements range from a visual estimate on an oscilloscope to quantitative measurements that extract statistical data from many signal samples.

The sequential acquisition of a clock signal over three periods produces a diagram that reveals both jitter and voltage noise. Because the signal may produce any of eight binary patterns during an acquisition, a measuring instrument overlays millions of signal samples to create an "eye" diagram (see figure). The overlay diagram lets engineers determine a signal's maximum jitter and voltage noise. As these errors increase, the eye width and height decrease. The better the quality of a digital signal, the more open the eye. Said differently, engineers strive to maximize eye width and height.

When an eye diagram comprises millions of samples, the eye width indicates the time the data lines remain stable. Thus, engineers can determine how much set-up and hold time a clock signal provides.

A Case of the Jitters?

The microcontroller board Jane designed seems to suffer from intermittent problems. The microcontroller's specifications list tight timing requirements, so the cause of intermittent behavior may rest with Jane's new clock circuit.

Can you help Jane analyze her clock signal to identify possible problems?

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