

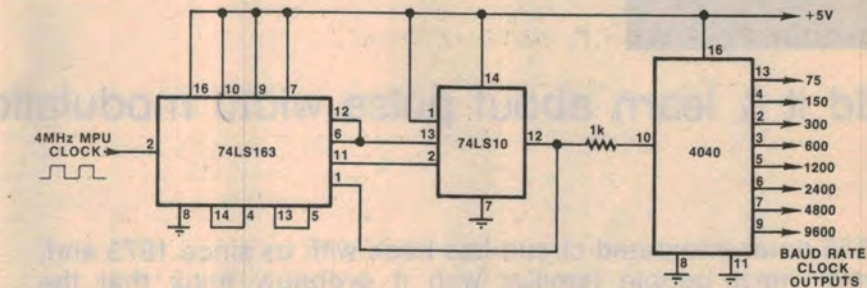
CIRCUIT & DESIGN IDEAS

Direct derivation of baud rate clock signals from a 4MHz clock signal

The specific ICs designed to provide these signals are generally rather expensive and tend to use a separate non-standard quartz crystal. This generally results in a system costing of the order of \$30 merely to generate those I/O clock signals.

After some thought and the use of a calculator, it became clear that another far less expensive method of obtaining these important signals was possible. The result is a circuit which produces 16x baud rate clock signals only +0.16% above the nominal values and which is in a constant timing and phase relationship with the MPU clock signals.

In operation, the 74LS163 (any 4 bit resettable counter may be used) is driven by the 4MHz clock signal, derived in the author's system from a 6875 clock generator. The 74LS10 is used to decode a count of 13 (decimal), hence



we have a modulo 13 counter. The resulting signal has a repetition rate equivalent to 307.692kHz, as against the nominal 307.2kHz.

This is further divided by the 4040 12-stage binary counter to give appropriate output frequencies for 9600 baud, 4800 baud, 2400 baud, 1200 baud, 600 baud, 300 baud, 150 baud and 75 baud. Since the author's system does not include a TTY it was thought an un-

necessary refinement to generate a 110 signal.

The outputs of the 4040 may be buffered as required to suit the system in use. I hope that this information may be of use to other interested readers.

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