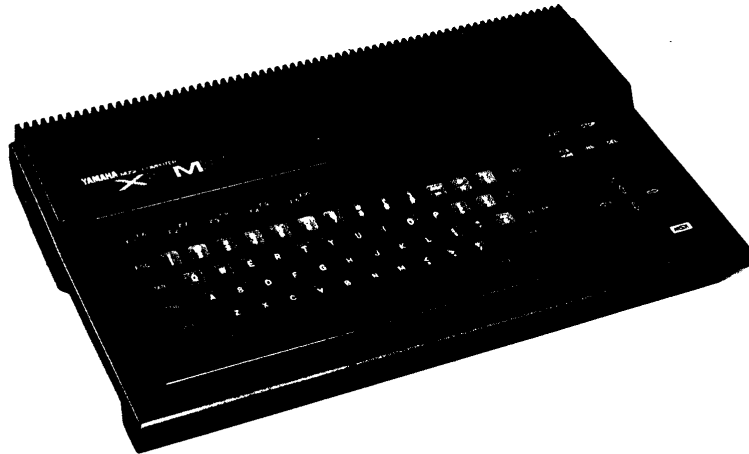


MUSIC COMPUTER CX-5M II

SERVICE MANUAL



MSX

CX-5M IIC
CX-5M IIE
CX-5M IIF
CX-5M IIA
CX-5M IIB
CX-5M IIP

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SINCE 1887



YAMAHA

NIPPON GAKKI CO., LTD. HAMAMATSU, JAPAN
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■ MSX COMPUTER ACCORDING TO AREA

There are different models of YAMAHA MSX COMPUTER according to area, this manual refer to the computer as only the CX-5MII, referring to all models. Where reference to particular model is called for, the specific model number pertaining to the area in question will be used. The different model numbers, and the area to which they pertain, are as follows.

| | | |
|--------------------|-------------------------------------|---------|
| CX-5MIIC | Canada | (NTSC) |
| CX-5MIIE | United Kingdom | (PAL-I) |
| CX-5MIIA | Australia and New Zealand | (PAL-B) |
| CX-5MIIF | France | (PAL-G) |
| CX-5MIIB | Italy | (PAL-G) |
| CX-5MIIP | Spain | (PAL-G) |

■ SCREEN DISPLAY

Display mode (on the BASIC language mode)

| MODE | | Resolution | Size | Patterns Number | Specified Color | Sprite | Characters |
|---------------------------|------------------|------------|-----------------|-----------------|--------------------|--------|------------|
| Text I (Screen 0) | MAX | 256 x 192 | 6 x 8 | 256 | 2 out of 16 colors | No | 40 x 24 |
| | Suggested values | 240 x 192 | | | | | 37 x 24 |
| Text II (Screen 0) | MAX | 512 x 192 | 6 x 8 | 256 | 2 out of 16 colors | No | 80 x 24 |
| | Suggested values | 480 x 192 | | | | | |
| Text (Screen 1) | MAX | 256 x 192 | 8 x 8 | 256 | 16 colors | Yes | 32 x 24 |
| | Suggested values | 240 x 192 | | | | | 29 x 24 |
| Graphic (Screen 2) | MAX | 256 x 192 | 8 x 8 | 768 | 16 colors | Yes | 32 x 24 |
| | Suggested values | 240 x 192 | | | | | 29 x 24 |
| Multi-color (Screen 3) | MAX | 64 x 48blk | 4 x 4 per block | — | 16 colors | Yes | — |
| | Suggested values | 60 x 40blk | | | | | |

Suggested values: The eight pixels from the left and the sixteen pixels from the right of the horizontal line are not used by the software.

■ SPECIFICATION

CPU

Type: LH0080A (Z80A compatible)
Clock: 3.579545MHz
Wait: 1 wait in M1 cycle
Interrupt: NMI-not used
 INT-accept interrupts from VDP and cartridge SLOT
 The interrupt mode is Z80 mode 1.
 The interval of the interrupt is 50Hz (NTSC: 60Hz).
Reset: Power on reset and reset switch.

MEMORY

Main Memory: 128 Kbyte (128 Model)
 (RAM) 64 Kbyte (64 Model)
BASIC ROM: 32 Kbyte (MSX1-BASIC)
Sub ROM: 16 Kbyte (for 80 Chara)
Video RAM: 16 Kbyte

VIDEO DISPLAY Video Display Processor (VDP)

Type: V9938
Character Set: 256 alphanumeric and graphic characters
Color: 16 colors
Text mode: SCREEN 0 or SCREEN 1
Capability: 24 lines by up to 80 columns
 (Software selectable)
Resolution: 256 x 192 pixels (non interlace)

INPUTS AND OUTPUTS

Keyboard: Stroke type step sculpture keyboard.
 Alphanumeric and special characters . 48
 Control and special effect keys 16
 Cursor movement keys 4
 Function keys (programmable) 5
 CAPS lock key with LED indicator

Cassette Interface: 8 pin DIN female connector
 Baud rate 1200/2400 BPS selectable by software, FSK format. With remote control (Cassette motor ON/OFF)

Printer Interface: Standard centronics 8-bit parallel TTL logic level
 14 pin female connector

Univarsal I/O Interface: 2 ports (JOYSTICK)
 9 pin male connectors TTL logic level

Audio/Video Output:

- 1) MONITOR output
 RCA type pin connector
 CX-5MIIE, F, A, B, P
 PAL composite video output 75 ohm
 CX-5MIIC
 NTSC composite video output 75 ohm
- 2) SOUND output
 RCA type pin connector
 CX-5MIIC, E, F, A, B, P
 8 octaves 3 tones + noise
 BEEP sound
- 3) RF output
 RCA type pin connector
 CX-5MIIC: NTSC (VHF3, 4)
 CX-5MIIA: PAL (VHF3, 4)
 CX-5MIIE, F, B, P: PAL (UHF36)
- 4) RGB output
 8 pin DIN female connector
 CX-5MIIC, E, F, A, B, P
- 5) Color or Block/White switch
 Monitor and RF output used

Upper SLOT A, B: SLOT 1, 2
 50 pin MSX standard female connector

SIDE SLOT: SLOT 33
 60 pin edge card connector FM sound unit

BILT in ROM SOCKET: SLOT 30
 30 pin plug right angle type

FM SOUND SYNTHESIZER UNIT

Number of Preset Voices: 46
Simultaneous Notes: Up to 8 notes
Audio L/R Outputs: $-9 \pm 2\text{dB}$, $1.8\text{k}\Omega$ RCA-pin jacks
MIDI IN/OUT: 5 pin DIN female connectors
Music Keyboard: For connection to an optional YK-01 or YK-10, 20 music keyboard.
 20 pin male connector

POWER SUPPLY UNIT CAPACITY

+5V $\pm 5\%$ 2.0A
 +12V $\pm 10\%$ 0.3A
 -12V $\pm 10\%$ 0.16A

GENERAL SPECIFICATIONS

Line voltage: CX-5MIIC
 117V $\pm 15\%$, 50/60Hz
 CX-5MIIE, F, A
 220 ~ 240V, 50/60Hz
 CX-5MIIB, P
 120V $\pm 10\%$, 50/60Hz
 220V $\pm 10\%$, 50/60Hz
 Switchable

Power input: 10W
 18W MAX

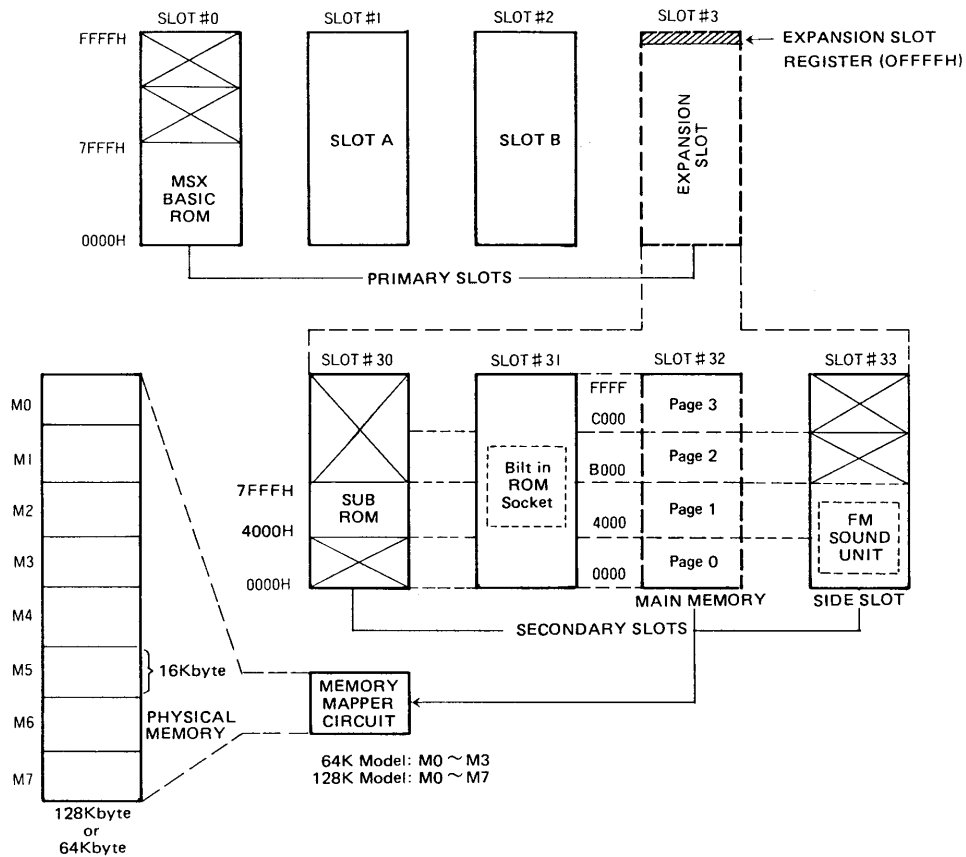
Measurement: 440(W) x 285(D) x 98(H)

Weight: 3.5 kg (about)

AC cable: 2,000 mm + 50 mm
 with AC plug (CX-5MIIC, F, A, B, P)

■ CX-5M II BRIEF DESCRIPTION

• Memory map and slot area



* Terminology: Primary slot Slot which is enabled by slot select register with in MPS chips (I/O address 0A8H)
 Secondary slot Slot which is enabled by expansion slot register placed at 0FFFH (Memory address)
 Page Block of memory (maximum 16KB) in each slot. A slot is divided into 4 pages.

* Every select signal of each slot is output from MPS (100 pin LSI: S-3527)

| | |
|-------------------------------|--|
| MSX BASIC ROM | $\overline{\text{ROMCS}}$ |
| SLOT A, SLOT B | $\overline{\text{SLT1}}, \overline{\text{SLT2}}, \overline{\text{CS1}}, \overline{\text{CS2}}, \overline{\text{CS12}}$ |
| Extended BASIC ROM | $\overline{\text{SLT30}} (\text{SUB ROM})$ |
| Built-in ROM socket | $\overline{\text{SLT31}}, \overline{\text{CS1}}, \overline{\text{CS2}}, \overline{\text{CS12}}$ |
| Main memory area | $\overline{\text{MPX}}, \overline{\text{WE}}, \overline{\text{RAS}}, \overline{\text{CAS2}}$ |
| Side slot | $\overline{\text{SLT33}}, \overline{\text{CS1}}, \overline{\text{CS2}}, \overline{\text{CS12}}$ |

* With the memory mapper circuit, the block by the unit of 16K bytes in the PHYSICAL MEMORY space can be mapped freely on each page of the MAIN MEMORY space.

• **I/O port area map**

The CPU (Z80A) has a 256-bytes area as I/O ports. Under the MSX specification, the 256-bytes (00H ~ FFH) are reserved in the following way:

| | | Address | R/W | Functions | |
|-----|--------------|---------|-----|------------------------------------|-----------------------------------|
| FFH | MAP Register | FFH | R/W | Map register for PAGE 3 | MAP Register |
| F0H | | FEH | R/W | Map register for PAGE 2 | |
| E0H | | FDH | R/W | Map register for PAGE 1 | |
| D0H | | FCH | R/W | Map register for PAGE ϕ | |
| B0H | | ABH | W | Command register | PPI chips Compatible in MPS clips |
| A8H | PPI | AAH | W | MSX system control output | |
| A0H | SSG | A9H | R | Reads return signals from keyboard | |
| 98H | VDP | A8H | R/W | Primary SLOT select register | |
| 90H | Printer | A2H | R | DATA read | SSG chips Compatible in MPS chips |
| 88H | | A1H | W | DATA write | |
| 80H | | A0H | W | SSG register address latch | |
| 98H | | 9BH | R/W | DATA register Read/write | VDP (V9938) |
| | | 9AH | W | DATA write | TMS9918 Compatible |
| | | 99H | R/W | Status read/command write | |
| | | 98H | R/W | V-RAM DATA read/write | |
| | | 91H | W | Print DATA latch output | TTL Logic level |
| 00H | | 90H | R/W | Strobe out/status in | in MPS chips |

All I/O port addresses shown in the above I/O port area map are located within the 100-pin LSI (S-3527). The LSI encloses the μ PD-8255A (PPI), YM2149 (SSG), and printer control circuit shown in the map. In addition, it has memory area and slot control functions.

* **MPS (S-3527) I/O ports register**

All the following MPS (S-3527) I/O ports provide the same port control functions as the PPI (μ PD-8255AC) and SSG (YM2149):

I/O address A8H (PA0 ~ PA7): Slot select data register

A9H (PB0 ~ PB7): Keyboard scanning data input (return) port

AAH (PC0 ~ PC3): Keyboard scanning data output port

(PC4): Data recorder (cassette recorder) motor ON/OFF control bit

(PC5): Output FSK specification data to data recorder (cassette)

(PC6): CAPS LED control bit (on when "L")

(PC7): Emits beeping sound through 1 bit output

I/O address A0H ~ A2H

Internal SSG register number: 10H

(IOA0 ~ IOA5): Input port for general purpose. Input/output port (JOYSTICK 1, 2) data scanning.

(IOA6): Not used

(IOA7): Input port for data from data recorder (cassette).

Internal SSG register number: 11H

(IOB0 ~ IOB3): JOYSTICK port scanning data output.

(IOB4): JOYSTICK 1 strobe signal output.

(IOB5): JOYSTICK 2 strobe signal output.

(IOB6): JOYSTICK 1 or 2 select signal

"L" JOYSTICK 1 selected

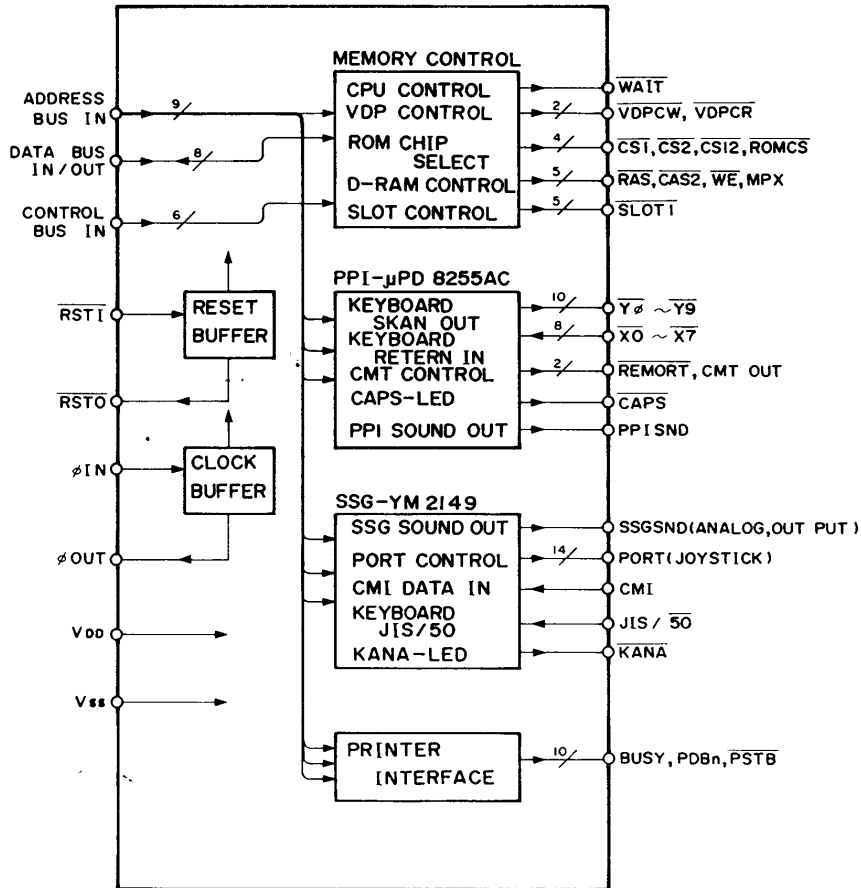
"H" JOYSTICK 2 selected

- MPS (MSX Port Controller and Sound Generator): S-3527

The MPS (S-3527) is a 100-pin CMOS LSI specifically developed to support MSX. With a built-in PPI (μ PD-8255) and SSG (YM-2149), the MPS provides the following system controller functions:

- Memory and slot area control
- ROM (MSX-BASIC ROM: 32K bytes) access
ROMCS
- RAM (D-RAM: 64K bytes) access
RAS, MPX, WE, CAS2
- Basic slot (# 1, # 2, # 3) control . . . Primary slot control
- Selection and control of expansion slots (# 00, # 01, # 02, # 03) . . . Secondary slot
- I/O area (I/O peripheral) control
- Printer control
BUSY, PDBn, PSTB
- VDP (video display processor) control
VDPCW, VDPCR
- With a built-in PPI (μ PD-8255) and SSG (YM-2149)
- 3-Channel 3-level voice and noise output
- Dual joystick (or general-purpose port) control
- Data recorder I/O control
- Keyboard control
- Insertion of 1 WAIT in the CPU M1 cycle
- RESET signal processing
- CPU clock (3,57954 MHz) input

« MPS Block Diagram »



* Removing MPS

- 1 Cut the legs with a cutter, being careful not to damage the pattern, as show in Figure A or fuse the solder with a special soldering iron as in Figure B.
- 2 After removing the MPS, desolder it with care not to damage the pattern.

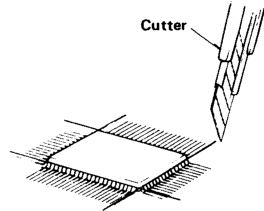


Fig. A

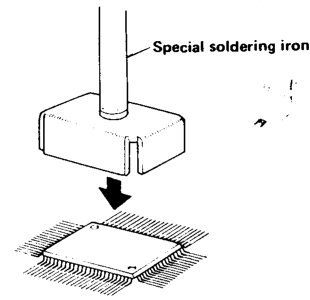


Fig. B

• VDP (Video Display Processor): V-9938

The VDP (V-9938) is a 64-pin MOS LSI developed for MSX2 concurrently with the MPS. The VDP is run on the MSX1 specifications. It provides the following functions:

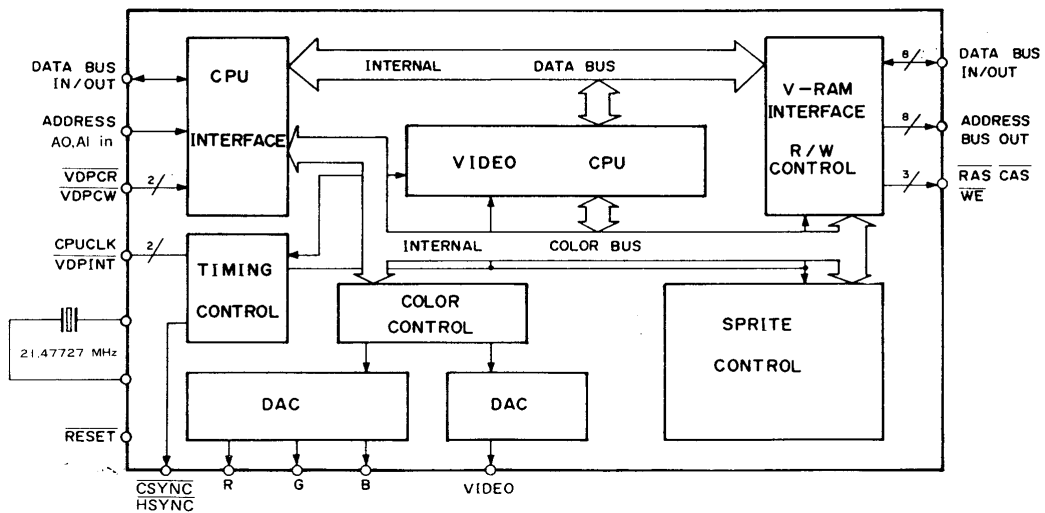
To provide software compatibility with the VDP (TMS9918A).

To generate linear RGB signals and composite video signals. Here, various video signals are produced from the linear RGB signals without using the composite video signals.

To use 16K bytes as video-RAM.

To supply a CPU clock (3.579545 MHz). The clock generated by a quartz oscillator (21.47727 MHz) connected to pins 63 and 64 is internally demultiplied and output to CPU clock pin 8.

« VDP Block Diagram »



■ MUSIC FUNCTIONS (SFG-05 COMPATIBLE)

● Audio characteristics

| Output level | 1 tone | 4 tone | 8 tone |
|----------------------|-------------|-------------|-------------|
| LINE OUT (L, R) | - 16 ± 2dBm | - 11 ± 2dBm | - 9 ± 2dBm |
| Standard BUS (59PIN) | - 17 ± 2dBm | - 12 ± 2dBm | - 10 ± 2dBm |

Condition : KEY 440Hz to 880Hz, 1 to 8 tones when FM standard FLUTE tone is selected.

Note : SOUND-IN of standard BUS is 49 pin and that of SIDE SLOT is 59 pin.

● Filter characteristics

| Condition | 440Hz | 1KHz | 2.7KHz | 10KHz | 16KHz | 20KHz |
|-------------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|
| CTI [iC101 9pin] OFF (L or R-ch) | + 7.5 ± 1dB | | | + 6.0 ± 1dB | + 4.2 ± 1dB | + 2.8 ± 1dB |
| CTI [iC101 9pin] ON (R-ch only) | + 7.5 ± 1dB | + 6.3 ± 1dB | + 1.5 ± 1dB | - 9.5 ± 1dB | | |

● Output impedance

| | |
|----------|-------|
| LINE OUT | 1.8KΩ |
| BUS OUT | 1.0KΩ |

● Music function I/O address map

| Address | Input | | | | | | OUTPUT | Internal register |
|---------|-------|----|----|----|----|----|--------|--|
| | CS0 | RD | WT | A2 | A1 | A0 | OPM | |
| | / | / | / | / | / | / | 1 | / |
| | | 1 | 1 | / | / | / | | / |
| 3FF0H | 0 | 0 | 1 | 0 | 0 | 0 | 0 | OPM STATUS REGISTER * in YM2195 (OPM) |
| | 0 | 1 | 0 | 0 | 0 | 0 | | OPM ADDRESS REGISTER * in YM2195 (OPM) |
| 3FF1H | 0 | 0 | 1 | 0 | 0 | 1 | 0 | OPM DATA REGISTER * in YM2195 (OPM) |
| | 0 | 1 | 0 | 0 | 0 | 1 | | OPM DATA REGISTER * in YM2195 (OPM) |
| 3FF2H | 0 | 1 | 0 | 0 | 1 | 0 | 1 | Register for data latched to ST0 to ST7 output ports |
| | 0 | 0 | 1 | 0 | 1 | 0 | | Data buffer for SD0 to SD7 input ports |
| 3FF3H | 0 | 1 | 0 | 0 | 1 | 1 | 1 | MIDI IRQ VECTOR ADDRESS REGISTER |
| | / | / | 1 | 0 | 1 | 1 | | / |
| 3FF4H | 0 | 1 | 0 | 1 | 0 | 0 | 1 | EXTERNAL IRQ VECTOR ADDRESS REGISTER |
| | / | 0 | 1 | 1 | 0 | 0 | | / |
| 3FF5H | 0 | 0 | 1 | 1 | 0 | 1 | 1 | MIDI standard UART DATA READ BUFFER |
| | 0 | 1 | 0 | 1 | 0 | 1 | | MIDI standard UART DATA WRITE BUFFER |
| 3FF6H | 0 | 0 | 1 | 1 | 1 | 0 | 1 | MIDI standard UART STATUS REGISTER |
| | 0 | 1 | 0 | 1 | 1 | 0 | | MIDI standard UART COMMAND REGISTER |
| 3FF7H | / | / | / | 1 | 1 | 1 | 1 | / |

■ MIDI RECEIVING AND TRANSMITTING DATA

The unit receives the following MIDI signals (when CALL MUSIC is functioning).

● MIDI receiving data

● Channel message

When the MIDI receiving channel is specified for each instrument, the unit receives the following MIDI signals transmitted through the specified channel.

① Key-OFF

| | | |
|----------|-------------------------|------------------------|
| Status | 1 0 0 0 n n n n (8 n H) | n = channel No. |
| Note No. | 0 k k k k k k k | k = 0 (C-2) ~ 127 (G8) |
| Velocity | 0 v v v v v v v | v : Neglected |

② Key-ON

| | | |
|----------|-------------------------|-------------------------------------|
| Status | 1 0 0 1 n n n n (9 n H) | n = channel No. |
| Note No. | 0 k k k k k k k | k = 0 (C-2) ~ 127 (G8) |
| Velocity | 0 v v v v v v v | v = 0 Key-OFF v = 1 ~ 127 Key-ON |

③ Control change

| | | |
|---------------|-------------------------|-----------------|
| Status | 1 0 1 1 n n n n (B n H) | n = channel No. |
| Control No. | 0 c c c c c c c | c = control No. |
| Control Value | 0 v v v v v v v | |

C = 5 Portamento time (SOLO mode only)
C = 7 Volume
C = 64 Sustain switch
C = 65 Portamento switch (SOLO mode only)
C = 125 All notes OFF

④ Program change

| | | |
|-------------|-------------------------|--------------------------|
| Status | 1 1 0 0 n n n n (C n H) | n = channel No. |
| Program No. | 0 p p p p p p p | p = program No. (0 ~ 47) |

● System real time message

The unit receives the following system real time messages when the play clock is MIDI.

① Timing clock

| | |
|--------|-------------------------|
| Status | 1 1 1 1 1 0 0 0 (F 8 H) |
|--------|-------------------------|

② Start

| | |
|--------|-------------------------|
| Status | 1 1 1 1 1 0 1 0 (F A H) |
|--------|-------------------------|

③ Continue start

| | |
|--------|-------------------------|
| Status | 1 1 1 1 1 0 1 1 (F B H) |
|--------|-------------------------|

④ Stop

| | |
|--------|-------------------------|
| Status | 1 1 1 1 1 1 0 0 (F C H) |
|--------|-------------------------|

● MIDI transmitting data

The unit transmits the content played by the music keyboard and reproduction data through MIDI channel 1.

● Channel voice message

① Key-OFF/Key-ON

| | | |
|----------|------------------------|-------------------------------------|
| Status | 1 0 0 1 0 0 0 0 (90 H) | |
| Note No. | 0 k k k k k k k | k = 0 (C-2) ~ 127 (G8) |
| Velocity | 0 v v v v v v v | v = 0 key-OFF v = 1 ~ 127 key-ON |

● System real time message

The unit outputs the following system real time messages when the play clock is INTERNAL..

① Timing clock

| | |
|--------|-------------------------|
| Status | 1 1 1 1 1 0 0 0 (F 8 H) |
|--------|-------------------------|

② Start

| | |
|--------|-------------------------|
| Status | 1 1 1 1 1 0 1 0 (F A H) |
|--------|-------------------------|

③ Stop

| | |
|--------|-------------------------|
| Status | 1 1 1 1 1 1 0 0 (F C H) |
|--------|-------------------------|

| Function ... | Transmitted | | Recognized | | | Remarks | |
|----------------------|---|-----------|---------------|------|------|---------|-------------------|
| | Synthe. | Sequencer | Solo | Poly | Seq | | Rh. |
| Basic Default | 1 | | 1 | 1* | Same | X | * #2, #4 off |
| Channel Changed | 1-16 | | 1-16 | 1-16 | as#1 | X | |
| Default | 3 | | 3 | | | X | |
| Mode Messages | X | | X | | | X | |
| Altered | ***** | | X | | * | X | |
| Note | 36-84 | 0-127 | 0-127 | | | X | |
| Number : True voice | ***** | | 0-127 | * | | X | |
| Velocity Note ON | X V=64 | 0 V=1-127 | O | | | X | |
| Note OFF | X 9nH | V=0 | X | | | X | |
| After Key's | X | | X | | | | |
| Touch Ch's | X | | X | | | | |
| Pitch Bender | X | | X | | | | |
| Control (5) | X | | O | X | X | | Portamento Speed |
| (7) | X | | O | O | X | | Volume |
| (64) | X | | O | O | X | | Sustain ON/OFF |
| (65) | X | | O | X | X | | Portamento ON/OFF |
| Change | | | | | | | |
| Prog | X | | O | 0-47 | X | | |
| Change : True # | ***** | | O | 0-47 | X | | |
| System Exclusive | X | | X | | | | |
| System : Song Pos | X | | X | | | | |
| : Song Sel | X | | X | | | | |
| Common : Tune | X | | X | | | | |
| System : Clock | O (Internal Mode) | | O (MIDI Mode) | | | | |
| Real Time : Commands | O (Internal Mode) | * | O (MIDI Mode) | | | * | Except FBH |
| Aux : Local ON/OFF | X | | X | | X | | |
| : All Notes OFF | O (126, 127, 123) | | O (123) | | X | | |
| Mes- : Active Sense | X | | X | | X | | |
| sages : Reset | X | | X | | X | | |
| Notes | In Split/Dual-Mode (of POLY Mode), MIDI Ch# of Inst#2 is same as Inst#1'S | | | | | | |
| | In order to clear all notes, we send [A11 notes OFF (126, 127, 123)] | | | | | | |

9 Mode 1 : OMNI ON, POLY Mode 2 : OMNI ON, MONO Mode 3 : OMNI OFF, POLY Mode 4 : OMNI OFF, MONO O : Yes X : No

■ SLOT A AND SLOT B ASSIGNMENT

| Pin No. | Pin Name | I/O | Description |
|---------|----------|-----|--|
| 1 | CS1 | O | Select Signal for ROM 4000H-7FFFH |
| 2 | CS2 | O | Select Signal for ROM 8000H-BFFFH |
| 3 | CS1, 2 | O | Select Signal for ROM 4000H-BFFFH |
| 4 | SLTSL | O | Slot Select Signal |
| 5 | N/C | - | Inhibited to use |
| 6 | RFSH | O | Dinamic RAM refresh signal |
| 7 | EXT WAIT | I | WAIT request, open collector signal |
| 8 | EXT INT | I | Maskable interrupt request, open collector signal |
| 9 | MT | O | M1 signal from CPU |
| 10 | BUSDIR | I | Direction Control for external Bus Buffer |
| 11 | TORQ | O | I/O request from CPU |
| 12 | MERQ | O | Internal memory request from CPU |
| 13 | WR | O | Write request from CPU |
| 14 | RD | O | Read request from CPU |
| 15 | RESET | O | System Preset signal |
| 16 | N/C | - | Inhibited to use |
| 17 | A9 | O | } Address Bus signal |
| 18 | A15 | O | |
| 19 | A11 | O | |
| 20 | A10 | O | |
| 21 | A7 | O | |
| 22 | A6 | O | |
| 23 | A12 | O | |
| 24 | A8 | O | |
| 25 | A14 | O | |
| 26 | A13 | O | |
| 27 | A1 | O | |
| 28 | A0 | O | |
| 29 | A3 | O | |
| 30 | A2 | O | |
| 31 | A5 | O | } Data Bus signal |
| 32 | A4 | O | |
| 33 | D1 | I/O | |
| 34 | D0 | I/O | |
| 35 | D3 | I/O | |
| 36 | D2 | I/O | |
| 37 | D5 | I/O | |
| 38 | D4 | I/O | |
| 39 | D7 | I/O | |
| 40 | D6 | I/O | |
| 41 | GND | - | Ground |
| 42 | CLOCK | O | System Clock 3.579545MHz |
| 43 | GND | - | Ground |
| 44 | SW1 | - | System protection |
| 45 | +5 | - | Power Supply +5V |
| 46 | SW2 | - | System protection (Note: SW1 and SW2 is in connection when Cartridge is inserted.) |
| 47 | +5 | - | Power Supply +5V |
| 48 | +12 | - | Power Supply +12V |
| 49 | SOUND IN | I | Sound input line (-5dbm) mixed with PSG sound and output |
| 50 | -12 | - | Power Supply -12V |

• SIDE SLOT assignment

| Pin No. | Pin Name | I/O | Description |
|---------|-----------|-----|------------------------------|
| 1 | SOUND OUT | O | Mixing Sound out of SSG, PP1 |
| 2 | GND | - | Ground |
| 3 | GND | - | Ground |
| 4 | NC | - | } Non connect |
| 5 | NC | - | |
| 6 | NC | - | |
| 7 | VIDEO | O | Video Out |
| 8 | NC | - | } Non connect |
| 9 | NC | - | |
| 10 | NC | - | |
| 11-60 | | | Exactly same as regular slot |

■ DISASSEMBLY PROCEDURES

● Before Proceeding with Repair:

- 1 Detach the side slot unit or cover.
- 2 Remove the screw in the center of the bottom case.
- 3 Remove the built-in ROM cartridge cover. If a ROM cartridge has been installed, remove it also.
- 4 Uncover the backup battery cover, remove the battery. (only MSX₂ Version)

1) Top Case Removal

- 1 The top case can be lifted by pushing it at claws with a standard screwdriver as shown in Figure A. Release them one by one.
- 2 After releasing all the four claws, detach the top case by lifting it a little on the rear side. The top case is fixed on the front side at the claw as shown in Figure B. Never use undue force to release it.

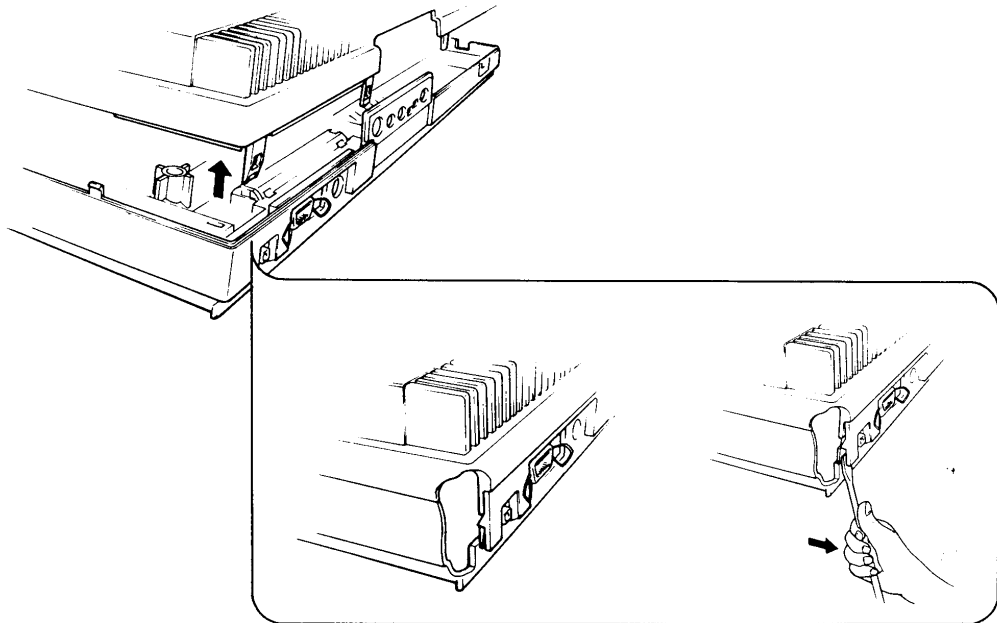


Fig. A

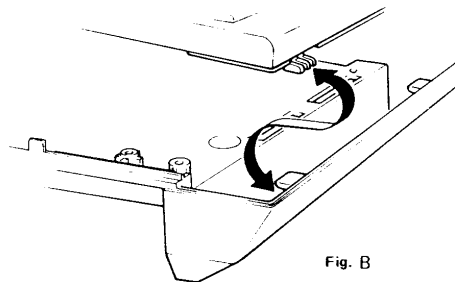
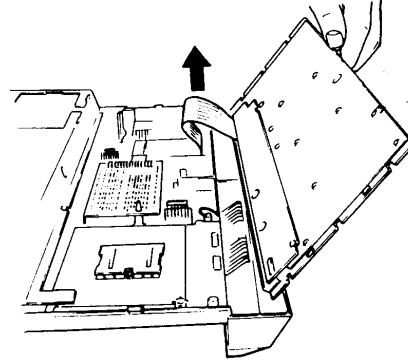
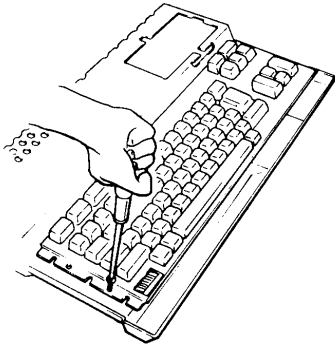


Fig. B

2) Keyboard Unit Removal

- 1 Remove four screws on both sides (four in total) of the keyboard unit.
- 2 Lift off the keyboard unit, slowly removing the flat cable from the CPU circuit board.
- 3 Remove Upper shield (only CX-5MIU, G)



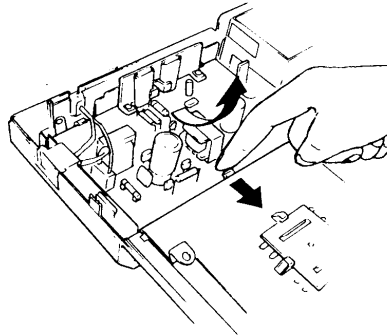
• Board and Unit Removal Procedures

Remove the boards and units in the following sequence. Reverse the removal procedures to reinstall them.

- Step 1) Power supply unit removal
- Step 2) Video module unit removal
- Step 3) Side slot earth plate removal
- Step 4) Main CPU board removal
- Step 5) Bottom shield removal

3) Power Supply Unit Removal

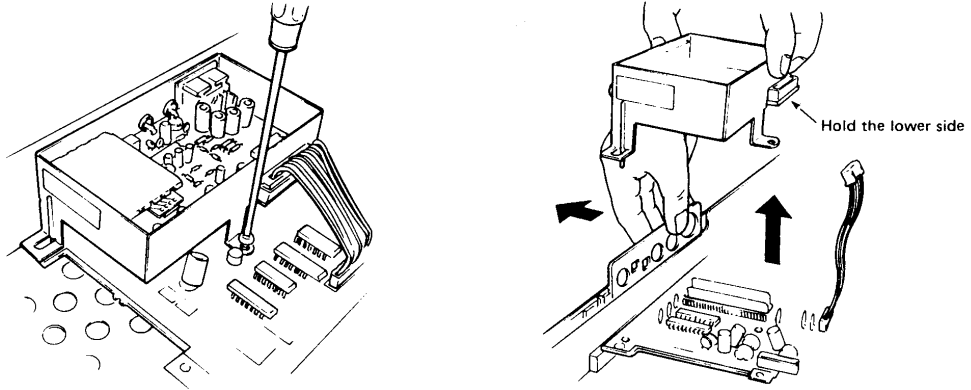
- 1 Pull out the power connector attached to the power supply unit. Next, disconnect the AC inlet (power switch and power cable). Then, pull out the connector (bundled wires) from the CPU circuit board.
- 2 Remove four screws. Next, pulling forward the stopper claw extending from the bottom case, lift the CPU board on the front side. Then, remove the power supply unit by pulling it forward as a whole.



4) Video Module Unit Removal

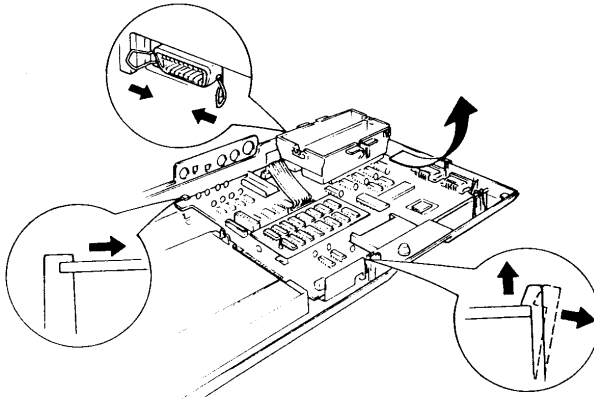
- 1 Pull out the connector from the CPU circuit board.
- 2 Remove two screws.
- 3 Pushing the rear panel inward a little, lift off the video module unit.
(The video module unit has legs as shown. Be careful not to damage them during removal.)

* In attaching the connector to the video module unit, insert it while holding the lower side of the circuit board as it is easily cracked.



5) CPU Circuit Board Removal

- 1 Remove seven screws securing the CPU circuit board in position.
- 2 Remove the side slot earth plate.
- 3 Release the two stopper claws extending from the bottom case by lifting the board a little on the front side. Then, remove the CPU circuit board by pulling it forward. Note that the in CPU circuit board is also secured in position by two stopper claws from the bottom case. The printer connector stoppers may be secured with a rubber band to facilitate servicing.



* The video RAM circuit board and the main RAM circuit board are screwed to the bottom case by a grounding plate each. Follow the steps below to remove these boards.

6) Video RAM Circuit Board Removal

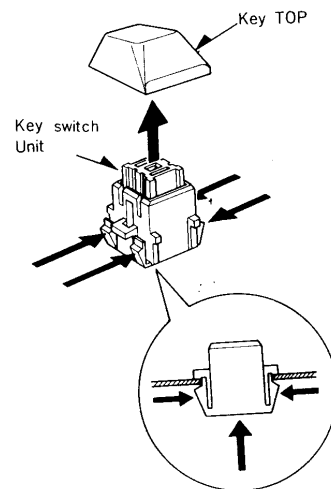
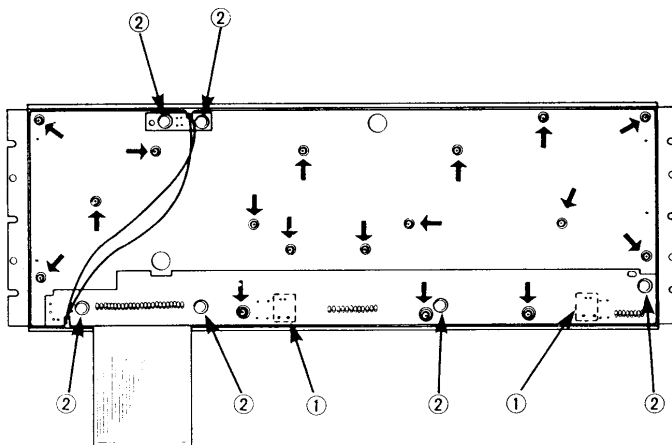
- 1 Remove one screw securing the video modulation unit, or remove the video modulation unit. Next, release the board stopper claws.
- 2 Detach the video RAM circuit board from the CPU circuit board connector.

7) Main RAM Circuit Board Removal

- 1 Remove one screw securing the power supply unit, or remove the power supply unit.
- 2 Remove the side slot earth plate.
- 3 Next, release the board stopper claws and detach the main RAM circuit board from the CPU circuit board connector.

8) Overhauling Keyboard Unit

- 1 Desolder S64, S63, D2, and D1 (CAPS and CODE key switches and LEDs) on the sub-circuit board ① .
- 2 Raise the sub-circuit board by removing the six plastic pins securing the sub-circuit board and the power LED. Extract the CN2 and CN3 flat cables at this time ② .
- 3 Remove the switch frame by unscrewing 17 special screws.
- 4 Pull out the keytops slowly as shown.
- 5 The key switch unit can be removed by holding it on the left and right claws and pushing them inward.



■ ADJUSTMENTS

| Adjustment | Equipment required | Measure at | Adjust | Readings |
|--------------------|----------------------------|--|--------------------|---------------------|
| +5V supply voltage | DVM (Digital voltmeter) | Pin #4 and 7 of connector CN2, CPU board | VR101 power supply | +5V ± 0.25V |
| Clock frequency | Frequency counter | Pin #6 of Z80A CPU | | 3.579545MHz ± 500Hz |

Notes) Check AC line voltage to insure that it is specification voltage ± 10%.
The adjustment for +5V supply voltage should be made while the circuitry of the CX-5MII is connected.

● Measurement

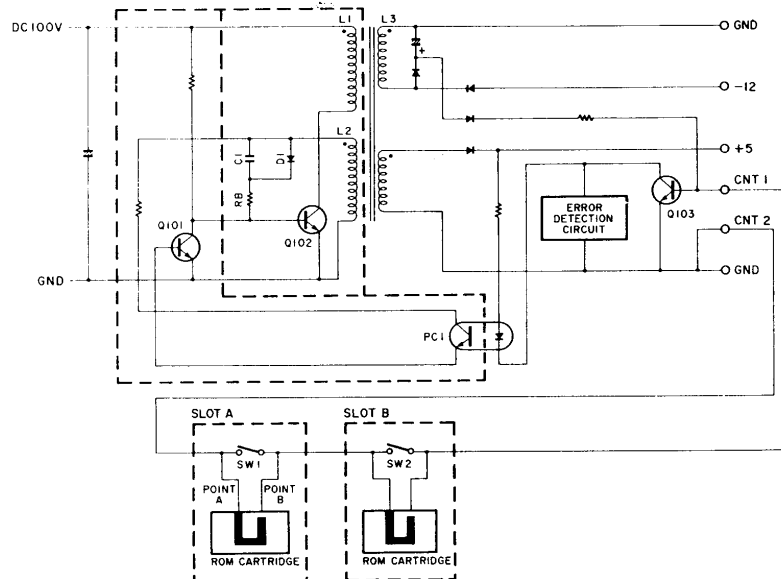
| Item | |
|-------------------------|--|
| Conditions | <ul style="list-style-type: none"> • Connect power circuit to CPU board. • Apply no load to each slot (game cartridge, etc.) of CPU board. • Don't connect peripheral equipments (printer, JOYSTICK, etc.). |
| Voltage | +5V ± 5% |
| Voltage to be confirmed | <ul style="list-style-type: none"> • -12V (1 pin) & GND: -12V ± 12.5% • +12V (2, 3 pin) & GND: +12V ± 12.5% |

• Adjust VR101 so that the above listed voltages are obtained at each voltage output pin with each unit connected. Also, confirm that the output voltage is within the tolerance range even when the power voltage is 220 to 240V or 117V.

• Check to make sure that each output voltage is within the cartridge protect voltage when the micro switch of the upper slot is turned OFF (pressed) or the 9 pin circuit of CN102 is opened.

| Circuit name | Voltage | Tolerance range | Cartridge protect voltage |
|--------------|---------|-----------------|---------------------------|
| -5V | +5V | ± 5V | Within 1V |
| +12V | +12V | ± 12.5V | Within 2V |
| -12V | -12V | ± 12.5V | Within 2V |

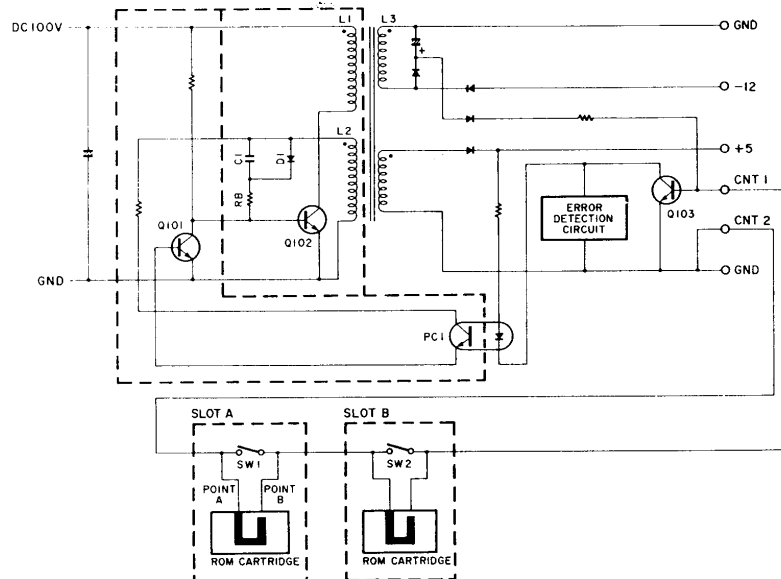
■ OPERATION OF POWER SUPPLY CIRCUIT



The following is the destination and operation of the circuit.

1. In D1, C1 and RB are the base drive circuits, and the base current of Q102 is determined by RB.
2. Q101 operates as a voltage controller and cartridge protector.
3. The photocoupler (PC1) feeds the voltage fluctuation of +5V back to the control circuit through the error detection circuit at all times. The control circuit controls output, based on the information fed back, by increasing and decreasing the base current of Q101 changing the oscillating frequency of Q102.
4. SW1, SW2 connected to Q103 in the cartridge protector circuit is ON at all times.
5. When Q103 is ON and the ROM cartridge is set in the slot-A erroneously, SW1 is turned OFF. Next, Q103 is turned ON, and the current flowing in the photocoupler (PC1) increases. Then, the photocoupler (PC1) on the control circuit is turned ON to turn ON Q101. The oscillating frequency of Q102 increases, the energy stored in L1 decreases, and output voltage lowers. When the ROM cartridge is properly set afterwards, A and B points in Fig. A are short-circuited, and voltage increases again.

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■ LSI DATA TABLE

● CPU (LH0080A)

| PIN NO. | PIN NAME | I/O | ACTIVE | FUNCTION |
|---------|-----------------------------------|-----|--------|---|
| 1 ~ 5 | A11, 12, 13, 14, 15 | O | | Address bus |
| 6 | ϕ | I | | CPU clock input (3.579545MHz) |
| 7 ~ 10 | CD4, 3, 5, 6 | I/O | | Data bus |
| 11 | VDD | I | | Voltage Supply +5V |
| 12 ~ 15 | CD2, 7, 0, 1 | I/O | | Data bus |
| 16 | $\overline{\text{INT}}$ | I | L | Mask-able interrupt input pin: Mode 1 is used for interrupt of MSX-BASIC which is input by taking the logic OR of the VDP interrupt output (every 1/60s.) and the cartridge interrupt input (EXT INT) |
| 17 | $\overline{\text{NMI}}$ | | | Non-connect |
| 18 | $\overline{\text{HALT}}$ | | | Non-connect |
| 19 | $\overline{\text{MREQ}}$ | O | L | Active when the effective address for memory access is on the address bus. |
| 20 | $\overline{\text{IORQ}}$ | O | L | Active when the effective address for the input/output port access is on the address bus (also active when in INT or ACK cycle) |
| 21 | $\overline{\text{RD}}$ | O | L | Active during the period when the CPU can receive data from the memory and input/output port. |
| 22 | $\overline{\text{WR}}$ | O | L | Active when the CPU sends data to be stored in the memory and input/output port to the data bus. |
| 23 | $\overline{\text{BUSAk}}$ | | | Pull up (+5V) |
| 24 | $\overline{\text{WAIT}}$ | I | L | CPU remains in the wait state as long as this signal is active "L". (No refresh signal is generated when in the WAIT state.) |
| 25 | $\overline{\text{BUSRO}}$ | | | Non-connect |
| 26 | $\overline{\text{RESET}}$ | I | L | The program counter becomes "0" at the $\overline{\text{RESET}}$ input and the CPU is initialized. |
| 27 | $\overline{\text{M1}}$ | O | L | One "L" pulse is output at each instruction fetch cycle (also active when in the INT or ACK cycle) |
| 28 | $\overline{\text{RFSH}}$ | O | L | Active when the low order 7 bit refresh address for D-RAM is on the address bus |
| 29 | Vss | I | | Ground |
| 30 ~ 40 | A0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 | O | | Address bus |

● MPS (S3527)

| PIN NO. | PIN NAME | I/O | ACTIVE | FUNCTION |
|---------|------------------------------|-----|--------|--|
| 1 | CMI | I | | Read signal input from cassette tape |
| 2 | CMO | O | | Write output to cassette tape |
| 3 | REM | O | | Cassette control signal output (motor ON/OFF control) |
| 4 | PRISND | O | | Software-controlled sound output |
| 5 | SSGSND | O | | SSG analog sound output |
| 6 | Vss | | | 0V SSG ground |
| 7 | $\overline{\text{VDPCW}}$ | O | | VDP (Video Display Processor) write timing signal output |
| 8 | $\overline{\text{VDPCR}}$ | O | | VDP read timing signal output |
| 9 | $\overline{\text{RSEL}}$ | I | * | Slot expansion address input |
| 10 ~ 18 | AB15 ~ AB0 | I | | Z80A CPU address bus input (9 bits) (AB15, AB14, AB7, AB6, AB5, AB4, AB3, AB1, AB0) |
| 19 ~ 26 | DB7 ~ DB0 | I/O | | Z80A CPU data bus I/O (8 bit) |
| 27 | $\overline{\text{SLT03/33}}$ | O | | Expanded slot 03 select signal |
| 28 | $\overline{\text{SLT01/31}}$ | O | | Expanded slot 01 select signal |
| 29 | ϕOUT | O | | Z80A CPU clock output |
| 30 | ϕIN | I | | Clock input (This signal is used via a buffer for clock input to other than the Z80A). |
| 31 | Vss | | | 0V ground |
| 32 | $\overline{\text{RST O}}$ | O | | Slot expansion initialization signal input |
| 33 | $\overline{\text{RST I}}$ | I | * | Slot expansion initialization signal input (RESET signal input) |
| 34 | $\overline{\text{M1}}$ | I | | Z80A CPU M1 input |
| 35 | $\overline{\text{RFSH}}$ | I | | Z80A CPU RFSH input |
| 36 | $\overline{\text{MREQ}}$ | I | | Z80A CPU input |
| 37 | $\overline{\text{IORQ}}$ | I | | Z80A CPU IORQ input |
| 38 | $\overline{\text{RD}}$ | I | | Z80A CPU RD input |
| 39 | $\overline{\text{WR}}$ | I | | Z80A CPU WR input |
| 40 | VDD | | | +5V power supply |

| PIN NO. | PIN NAME | I/O | ACTIVE | FUNCTION |
|---------|-------------|-----|-------------|--|
| 41 | WAIT | O | */ Δ | 1WAIT request signal output in M1 cycle (Wired logic with external WAIT signal possible) |
| 42 | ROMCS | O | | MSX BASIC ROM select signal output |
| 43 | RAS | O | | D-RAM RAS signal output (with Z80 RAS only refresh function) |
| 44 | MPX | O | | D-RAM address multiplex signal output |
| 45 | CAS3 | O | | D-RAM CAS signal output (CAS3: SLOT #0 C000 ~ FFFF) |
| 46 | CAS2/E | O | | D-RAM CAS signal output (CAS2/E: SLOT #32 0000 ~ FFFF) |
| 47 | WE | O | | D-RAM write enable signal output |
| 48 | FWD 1 | I | * | JOYSTICK FWD 1 signal or general-purpose port input |
| 49 | BACK 1 | I | * | JOYSTICK BACK 1 signal or general-purpose port input |
| 50 | LEFT 1 | I | * | JOYSTICK LEFT 1 signal or general-purpose port input |
| 51 | RIGHT 1 | I | * | JOYSTICK RIGHT 1 signal or general-purpose port input |
| 52 | TRGA 1 | I/O | */ Δ | JOYSTICK TRGA 1 signal or general-purpose port output (I/O by wired logic) |
| 53 | TRGB 1 | I/O | */ Δ | JOYSTICK TRGB 1 signal or general-purpose port output (I/O by wired logic) |
| 54 | STB 1 | O | | General-purpose port output |
| 55 | FWD 2 | I | * | JOYSTICK FWD 2 signal or general-purpose port input |
| 56 | BACK 2 | I | * | JOYSTICK BACK 2 signal or general-purpose port input |
| 57 | LEFT 2 | I | * | JOYSTICK LEFT 2 signal or general-purpose port input |
| 58 | RIGHT 2 | I | * | JOYSTICK RIGHT 2 signal or general-purpose port input |
| 59 | TRGA 2 | I/O | */ Δ | JOYSTICK TRGA 2 signal or general-purpose port output (I/O by wired logic) |
| 60 | TRGB 2 | I/O | */ Δ | JOYSTICK TRGB 2 signal or general-purpose port output (I/O by wired logic) |
| 61 | STB 2 | O | | General-purpose port output |
| 62 | Y10/SK | | */ Δ | Not used (Keyboard scanning signal output (1 bit)) |
| 63 | JIS/50 | I | * | Keyboard layout control input |
| 64 | CAPS | O | Δ | CAPS LED control signal output (Direct lighting of LED possible) |
| 65 | CODE | O | Δ | CODE LED control signal output (Direct lighting of LED possible) |
| 66 ~ 73 | X0 ~ X7 | I | * | Keyboard return signal input (8 bits) (X6 serves as function select input on a reset.) |
| 74 ~ 83 | Y0 ~ Y9 | O | Δ | Keyboard scanning signal output (10 bits) |
| 84 | CS1 | O | | ROM select signal output (4000 ~ 7FFF) |
| 85 | CS2 | O | | ROM select signal output (8000 ~ BFFF) |
| 86 | CS12 | O | | ROM select signal output (4000 ~ BFFF) |
| 87 | SLT1 | O | | Slot select signal output (SLOT #1) |
| 88 | SLT2 | O | | Slot select signal output (SLOT #2) |
| 89 | SLT3/30 | O | | Slot select signal output (SLOT #3) |
| 90 | VDD | | | +5V power supply |
| 91 | BUSY | I | * | Printer status input |
| 92 ~ 99 | PD87 ~ PD80 | O | | Print data output (8 bits) |
| 100 | PSTB | O | | Printer strobe output |

Note) * With pullup resistor ($\approx 22K$) Δ Open Drain (Pull Down) OUTPUT

• VDP (V9938)

| PIN NO. | PIN NAME | I/O | FUNCTION |
|---------|-----------|-----|---|
| 1 | GND | | Ground |
| 2 | DHCLK | O | Not used |
| 3 | DLCKL | I/O | |
| 4 | VDS | O | Not used |
| 5 | HSYNC | I/O | High level (high to middle): output, low level (middle to low): input (High: Non-HSYNC timing or color burst timing Middle: HSYNC timing or color burst timing Low: HSYNC input) |
| 6 | CSYNC | I/O | High level: composite SYNC output, low level: VSYNC input |
| 7 | BLEO | O | Not used |
| 8 | CPU CLK | O | 1/6 X'TAL frequency output |
| 9 | RESET | I | MSX-VIDEO circuit initialization |
| 10 | YS | O | Not used |
| 11 | CBDR | O | Not used |
| 12 ~ 19 | C7 ~ C0 | I/O | Not used |
| 20 | GND | | DAC ground |
| 21 | VIDEO | O | Not used (Composite video signal output) |
| 22 | G | O | Linear RGB signal output |
| 23 | R | O | Linear RGB signal output |
| 24 | B | O | Linear RGB signal output |
| 25 | INT | O | CPU interrupt request signal output (low: Interrupt-request) |
| 26 | LPS | I | Not used |
| 27 | LPD | I | Not used |
| 28 | MODE 1 | I | CPU interface mode select signal |
| 29 | MODE 0 | I | CPU interface mode select signal |
| 30 | CSW | I | CPU-VDP write strobe |
| 31 | CSR | I | CPU-VDP read strobe |
| 32 | CD7 | I/O | CPU-data bus |
| 33 | VBB | O | Circuit board voltage |
| 34 ~ 40 | CD0 ~ CD6 | I/O | CPU data bus |
| 41 ~ 48 | RD0 ~ RD7 | I/O | VRAM data bus |
| 49 ~ 56 | AD0 ~ AD7 | O | VRAM address bus |
| 57 | R/W | O | VRAM write strobe |
| 58 | Vcc | | +5V power supply |
| 59 | CASX | O | Not used |
| 60 | CAS1 | O | Not used |
| 61 | CAS0 | O | VRAM column address strobe |
| 62 | RAS | O | VRAM low address strobe |
| 63 | XTAL 1 | I | X'TAL connection (Externally oscillated clock is input to this pin.) |
| 64 | XTAL 2 | I | X'TAL connection (Externally oscillated clock is input to this pin.) |

Note) * With pullup resistor ($\approx 22k$) Δ Open Drain (Pull Down) OUTPUT

• 16Kbit x 4 DRAM (MB81416-12)

| PIN NO. | PIN NAME | I/O | ACTIVE | FUNCTION |
|---------|----------------|-----|--------|--|
| 1 | OE | I | | Output enable |
| 2, 3 | DQ1, DQ2 | I/O | | Data output |
| 4 | WE | I | | Write enable, write mode at active "L" |
| 5 | RAS | I | | Lower address strobe |
| 6 ~ 8 | A6, 5, 4 | I | | Address input |
| 9 | VDD | | | Voltage Supply +5V |
| 10 ~ 14 | A7, 3, 2, 1, 0 | I | | Address input |
| 15 | DQ3 | I/O | | Data output |
| 16 | CAS | I | | Column address strobe |
| 17 | DQ4 | I/O | | Data output |
| 18 | Vss | | | Ground |

Note) MB81416 is an N channel MOS RAM consisting of 16384 word x 4 bit. RAS only refresh type, write cycle (early write) type.

• 64Kbit DRAM (MB8264)

| PIN NO. | PIN NAME | I/O | ACTIVE | FUNCTION |
|---------|----------------|-----|--------|---|
| 1 | N.C | | | Non-Connect |
| 2 | D in | I | | Data input |
| 3 | WE | I | L | Write enable, write mode to D-RAM at active "L" |
| 4 | RAS | I | L | Lower address strobe |
| 5~7 | A0, 2, 1 | I | | Address bus input |
| 8 | Vcc | | | +5V |
| 9~13 | A7, 5, 4, 3, 6 | I | | Address bus input |
| 14 | D out | O | | Data output |
| 15 | CAS | I | L | Column address strobe |
| 16 | Vss | | | Ground |

• DAC (YM3012)

| PIN NO. | PIN NAME | I/O | FUNCTION |
|---------|-------------------|-----|---|
| 1 | VDD | — | +5V power |
| 2 | CLOCK | I | Timing clock for synchronizing with OPE |
| 3 | GND | — | |
| 4 | DATA | I | Tone serial data |
| 5 | SAM2 | I | Sampling data (for LR separator) |
| 6 | SAM1 | I | Sampling data (for LR separator) |
| 7 | ICL | I | Initial clear |
| 8 | GND | — | Ground for analog |
| 9 | CH1 | O | 1CH (L-CH) analog signal |
| 10 | CH2 | O | 2CH (R-CH) analog signal |
| 11 | COM | O | Offset control |
| 12 | To BUF | O | Offset control |
| 13 | Mid-point | O | Offset control |
| 14 | BIAS compensation | O | Offset control |
| 15 | BIAS | O | Offset control |
| 16 | GND | — | |

• MKS (YM2148)

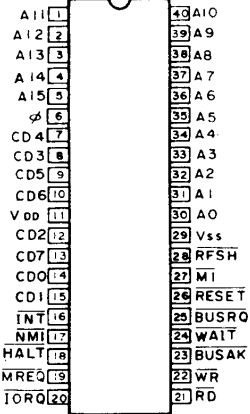
| PIN NO. | PIN NAME | I/O | FUNCTION | REMARKS |
|---------|----------------------------------|-----|---|---|
| 1 | V _{SS} | — | Ground | |
| 2~4 | A ₀ ~A ₂ | I | Selection signal for internal registers | |
| 5 | \overline{CS} | I | Chip select | |
| 6 | \overline{WT} | I | Write request for data from CPU | |
| 7 | \overline{RD} | I | Read request for data from CPU | |
| 8 | OPM | O | Address decode out to OPM | Output when A ₀ to A ₁ address input is 0 or 1. |
| 9~16 | ST ₀ ~ST ₇ | O | Used as strobe output to keyboard | Latch output ports in 2nd address |
| 17 | V _{DD} | — | +5V power | |
| 18 | RXD | I | MIDI serial data | |
| 19~26 | SD ₀ ~SD ₇ | I | Data input port | Data input ports to 2nd address |
| 27 | TXD | O | MIDI serial data | |
| 28~35 | D ₀ ~D ₇ | I/O | 3-state data bus I/O ports | |
| 36 | \overline{VR} | I | VECTOR ADDRESS REQUEST | Used for Z-80 MODE 2, IRQ |
| 37 | IRQ | O | Interrupt request generated when receiving and transmitting MIDI signal | Maskable |
| 38 | \overline{IC} | I | "L" reset data IRQ "H", OPM "H" | $\overline{ST_0} \sim \overline{ST_7}$ "H", D ₀ ~D ₇ "Hi impedance" |
| 39 | φA | I | Clock for MIDI baud rate generation | |
| 40 | φ | I | CPU Master clock for synchronizing with CPU | |

• OPM (YM2151)

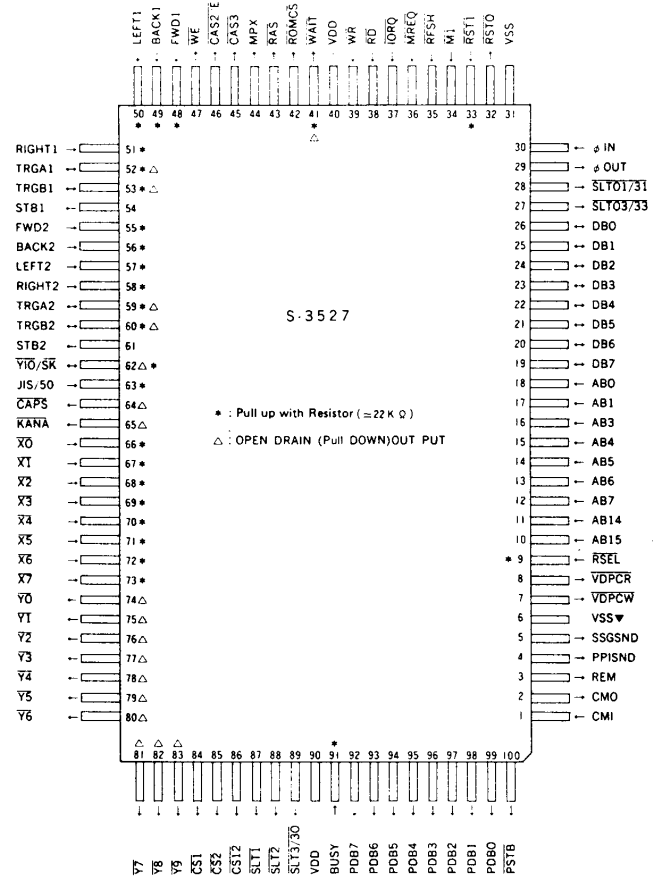
| PIN NO. | PIN NAME | I/O | FUNCTION | REMARKS |
|---------|--------------------------------|-----|---|---------|
| 1 | V _{SS} | — | Ground | |
| 2 | \overline{IRQ} | I | Interrupt request output port | |
| 3 | \overline{IC} | I | "L" reset | |
| 4 | A ₀ | I | Selection signal for internal register | |
| 5 | \overline{WT} | I | Write request for data from CPU | |
| 6 | \overline{RD} | I | Read request for data from CPU | |
| 7 | \overline{CS} | I | Chip select | |
| 8 | | | Not used | |
| 9 | $\overline{CT1}$ | O | Signal for switching voice synthesis filter characteristics | |
| 10 | D ₀ | I/O | 3-state data bus I/O port | |
| 11 | V _{SS} | — | Ground | |
| 12~18 | D ₁ ~D ₇ | I/O | 3-state data bus I/O ports | |
| 19 | SH1 | O | | |
| 20 | SH2 | O | Signal for separating L and R | |
| 21 | S ₀ | O | Serial data for sound source (L, R) | |
| 22 | V _{DD} | — | +5V power | |
| 23 | φ1 | O | Clock for DAC synchronization | |
| 24 | φ | I | CPU Master clock for synchronizing with CPU | |

LSI PIN CONFIGURATION

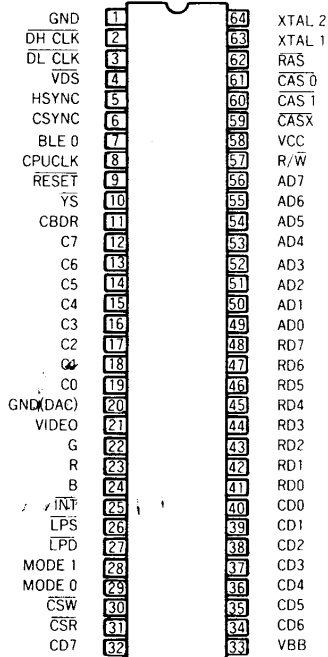
Z-80A (CPU)



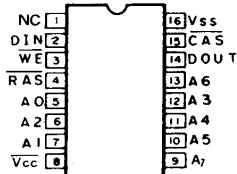
S3527 (MPS)



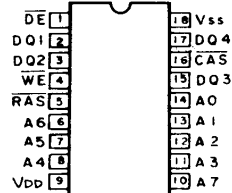
V9938 (VDP)



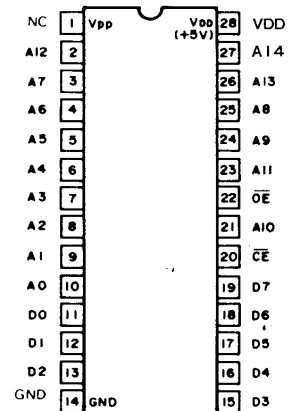
MB8264 (RAM)



MB81416-12 (RAM)

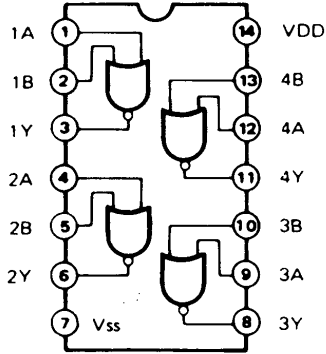


256K bit (EP-ROM)

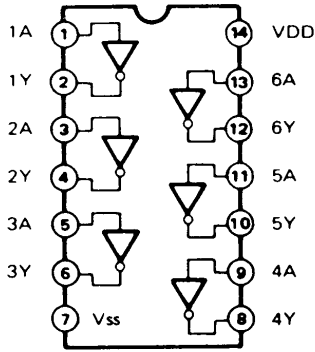


IC DIAGRAM

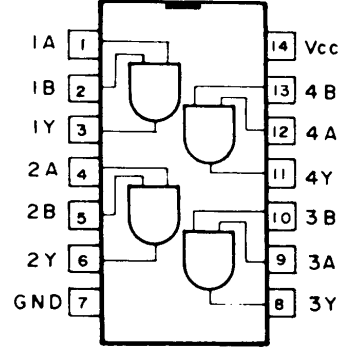
- HD74LS02
Quad 2-Input NOR



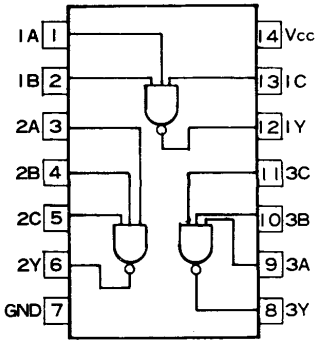
- HD74S04
• HD74LS04
Hex Inverters



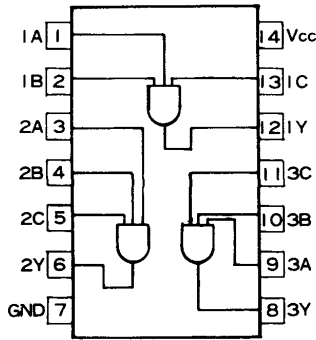
- 74LS08
Quad 2-Input NAND



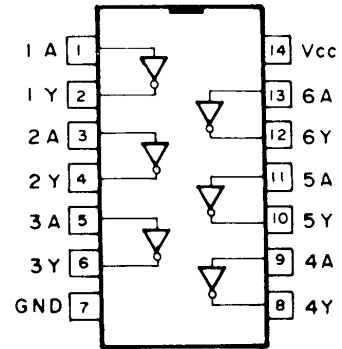
- 74LS10
Tri 3 Input NAND



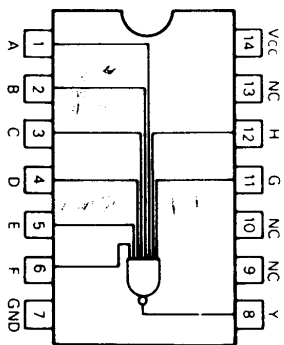
- HD74LS11
Tri 3-Input AND



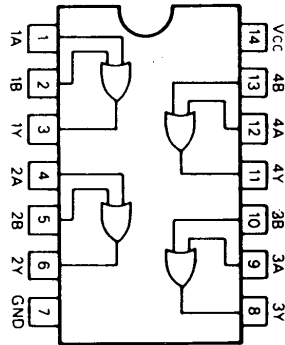
- 74LS14
Hex Schmitt
Trigger Inverters



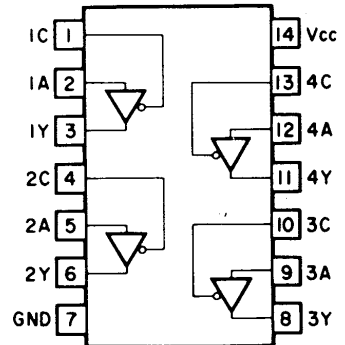
- 74LS30
8 Input NAND



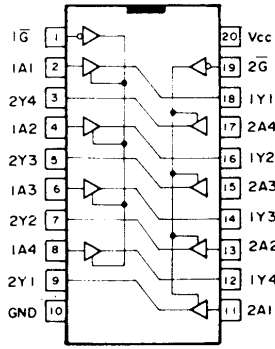
- 74LS32
Quad 2-Input OR



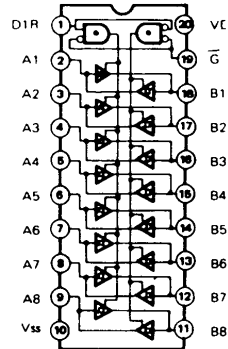
- 74LS125
Quad 3 State Bus Buffers



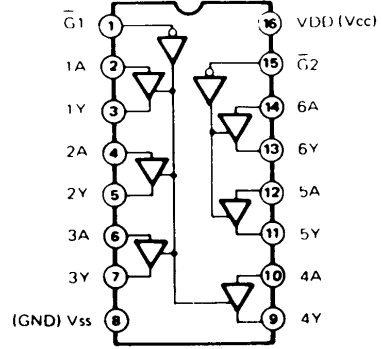
- 74LS244
Octal 3 State Bus Buffers



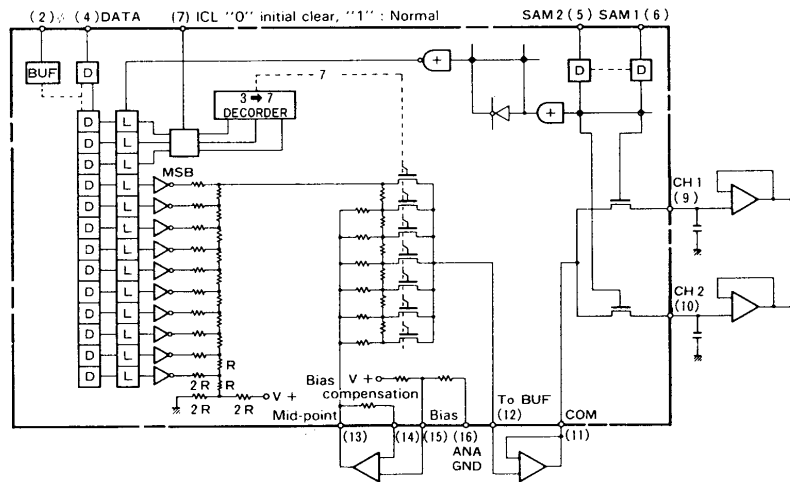
- 74LS245
Quad 3 State Bus Buffers

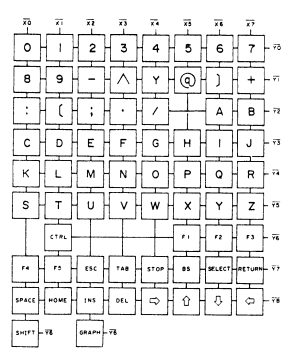
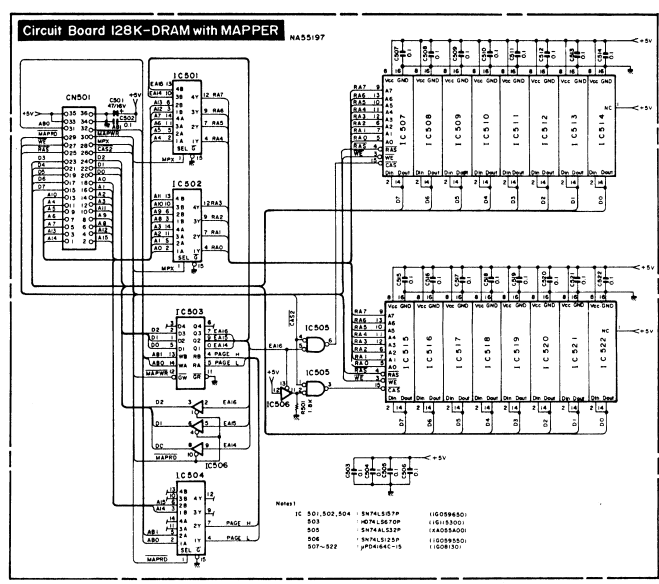
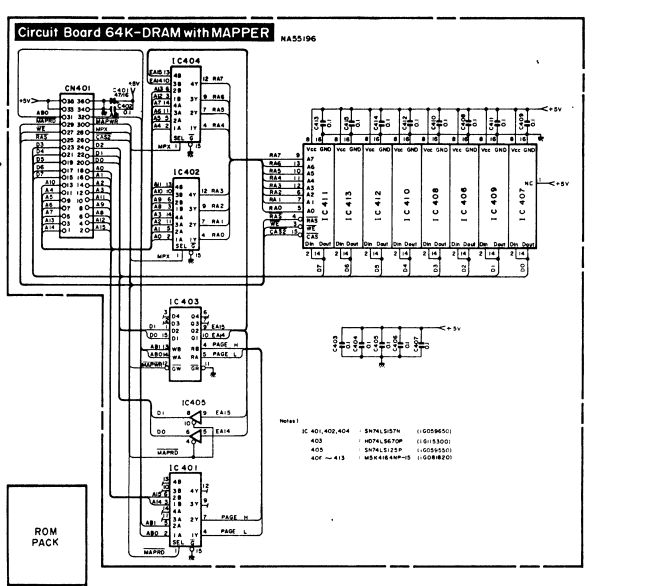
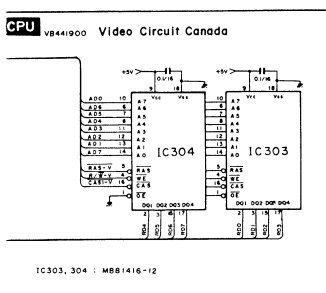
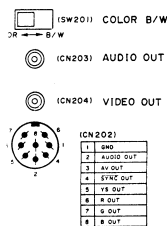
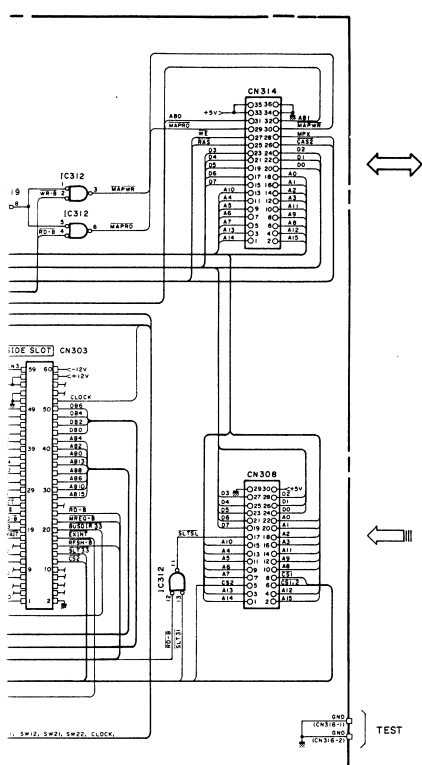


- 74LS367
Hex 3 State Bus Buffers

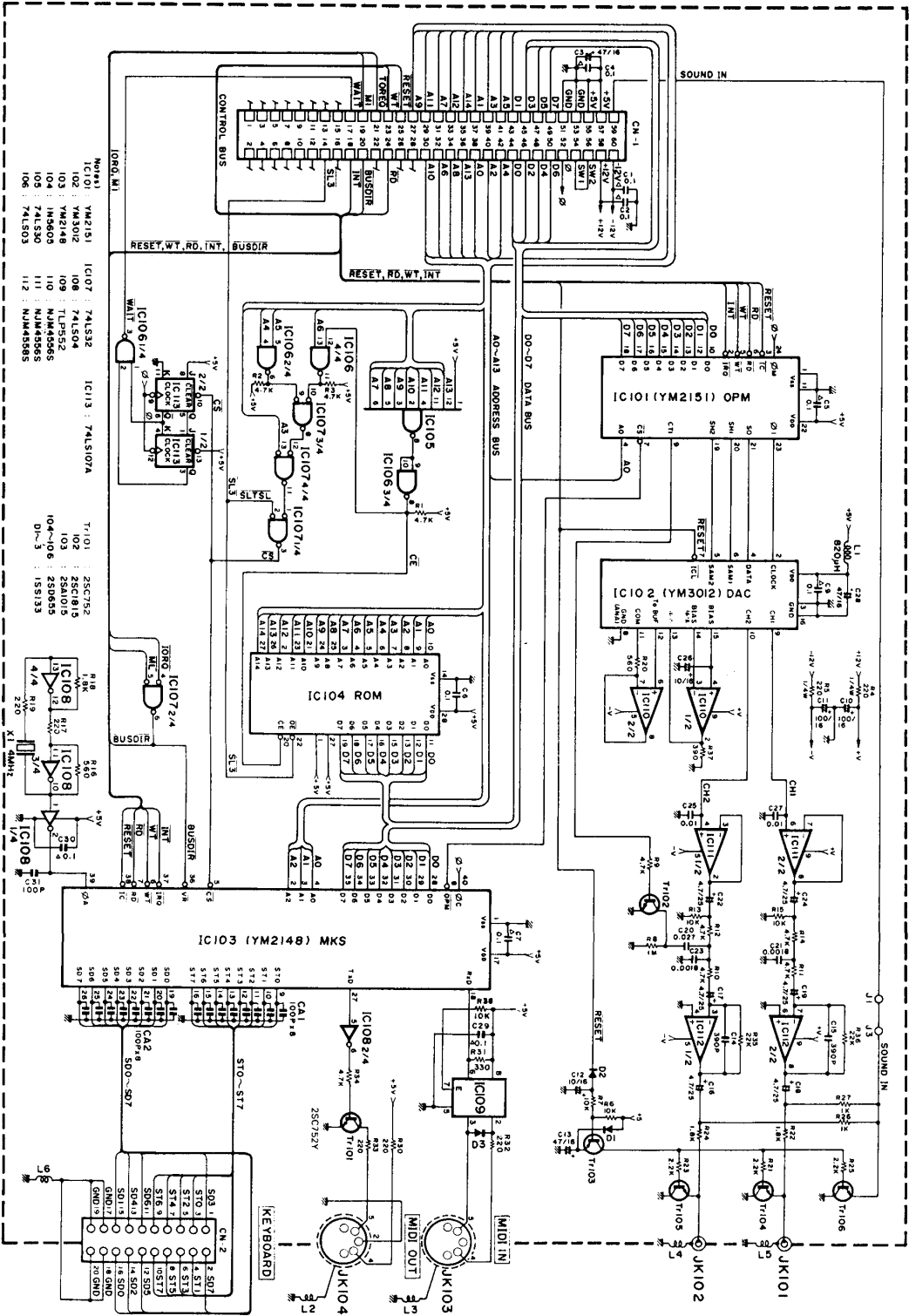


- DAC Diagram (YM3012)





■ CIRCUIT BOARD (FM SOUND UNIT)



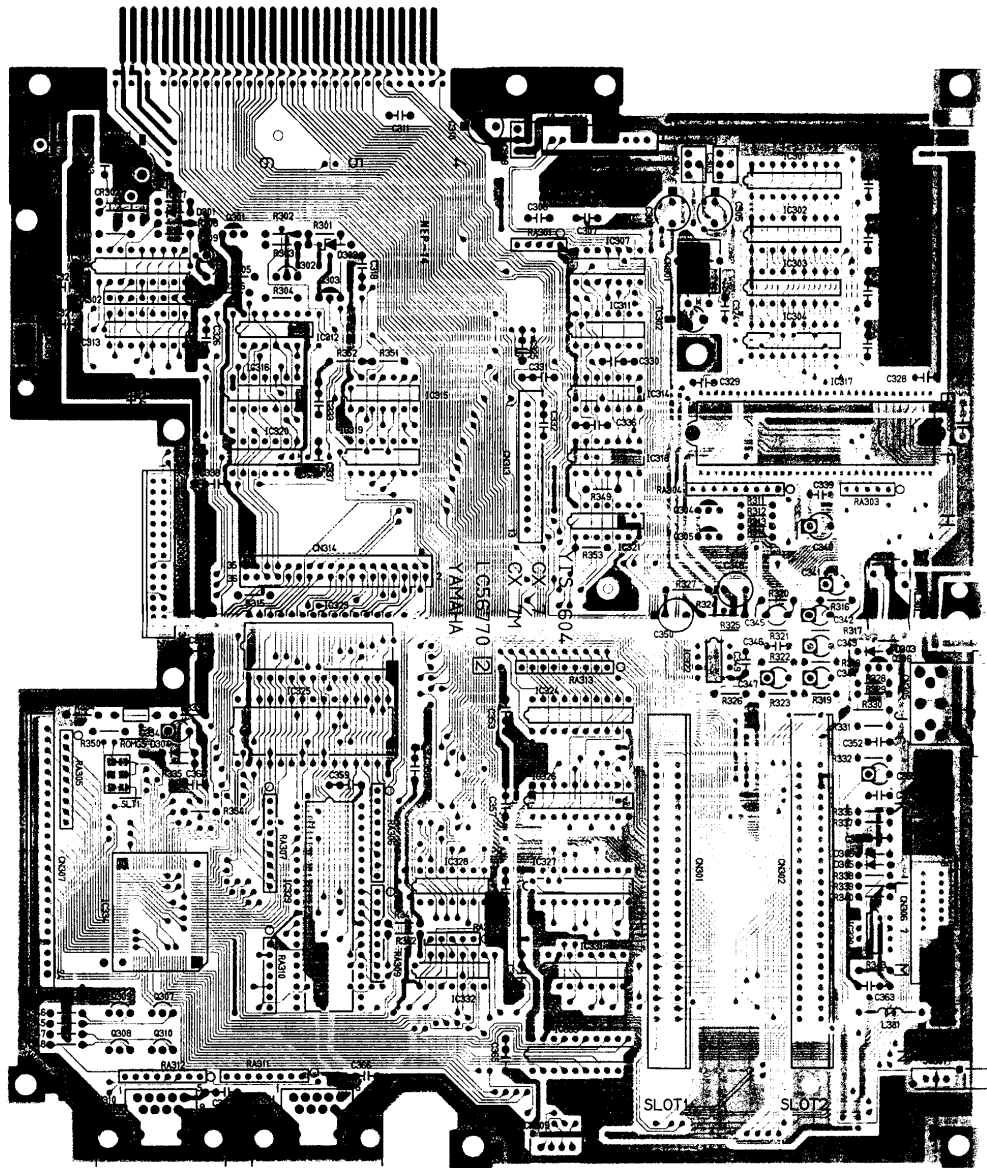
IC101: YM2151 IC102: YM3010
 IC103: T101 IC104: ROM
 IC105: T102 IC106: T103
 IC107: T104 IC108: T106
 IC109: T105
 IC110: T101
 IC111: T102
 IC112: T103

T101: 2SC752
 T102: 2SC752
 T103: 2SC752
 T104: 2SC752
 T105: 2SC752
 T106: 2SC752

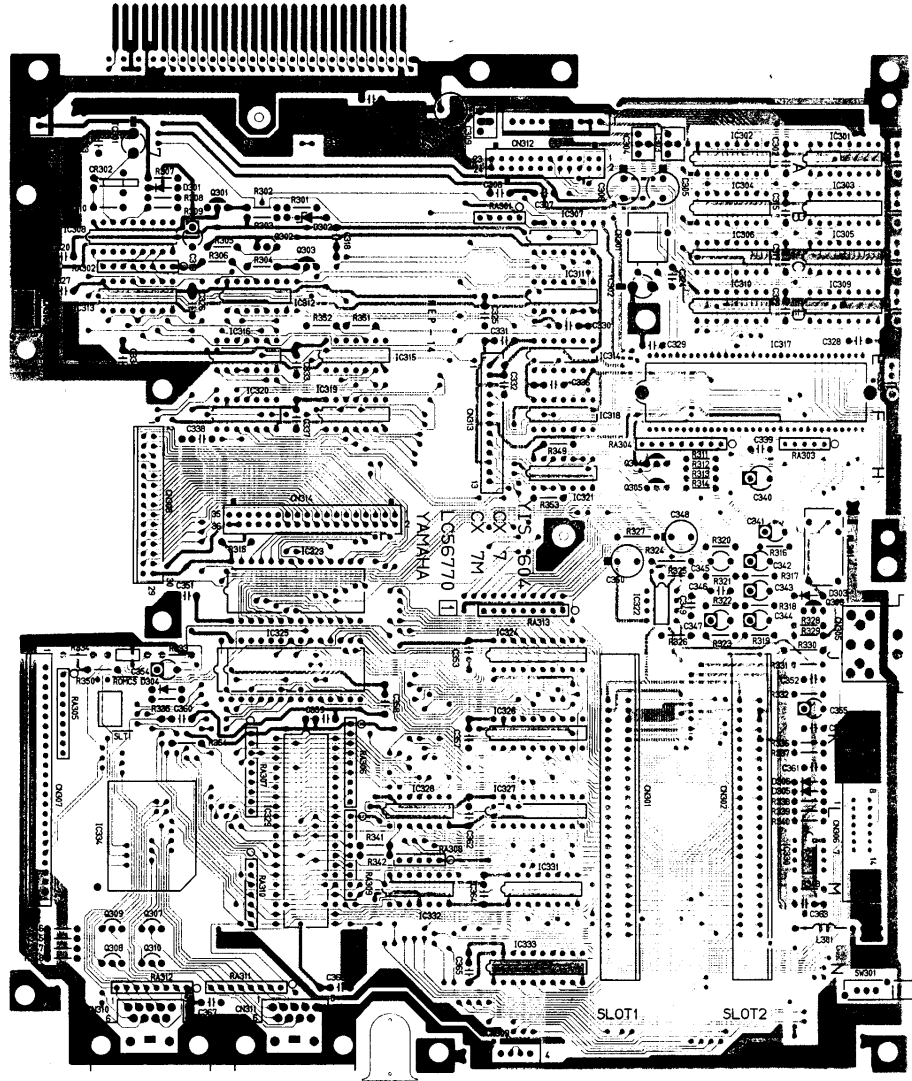
JK101: 1.50V
 JK102: 1.50V
 JK103: 1.50V
 JK104: 1.50V

JK101: 1.50V
 JK102: 1.50V
 JK103: 1.50V
 JK104: 1.50V

■ CX-5M11 C CIRCUIT BOARD



■ CX-5M II E, A, F, P CIRCUIT BOARD

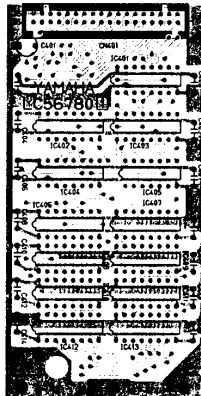


1
2
3
4
5
6

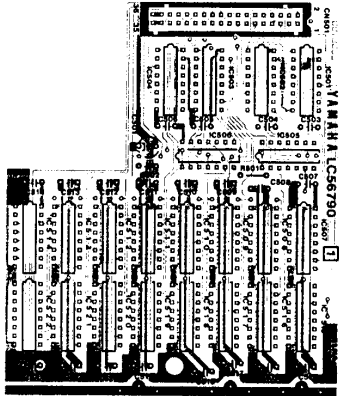
6 ■ 16K V-RAM CIRCUIT BOARD



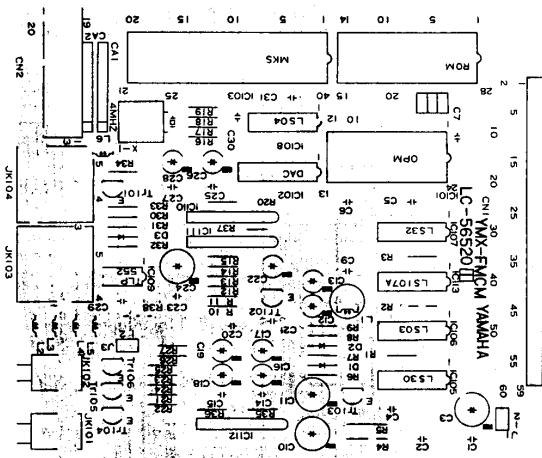
7 ■ 64K DRAM CIRCUIT BOARD



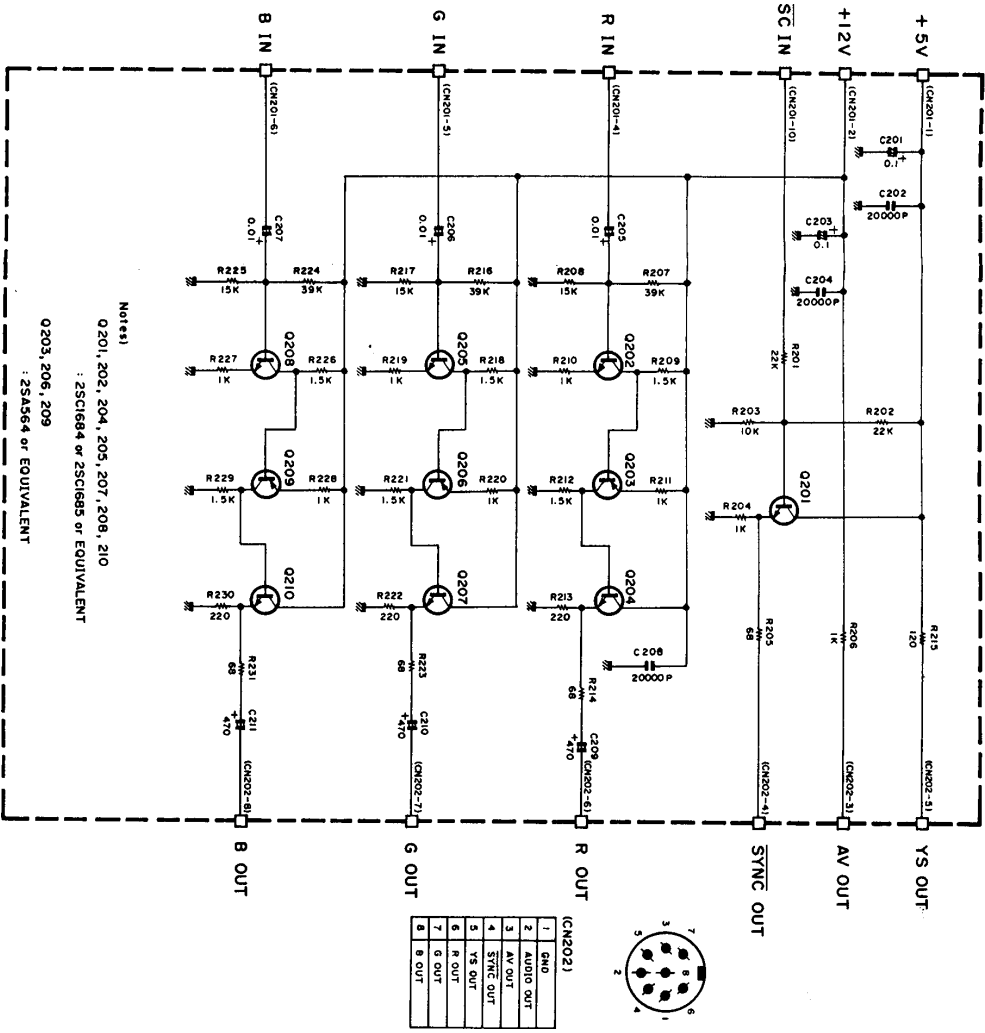
8 ■ 128K DRAM CIRCUIT BOARD WITH MAPPER



9 ■ CIRCUIT BOARD (FM SOUND UNIT)

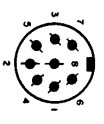


● PB551150 (CX-5M11F) old

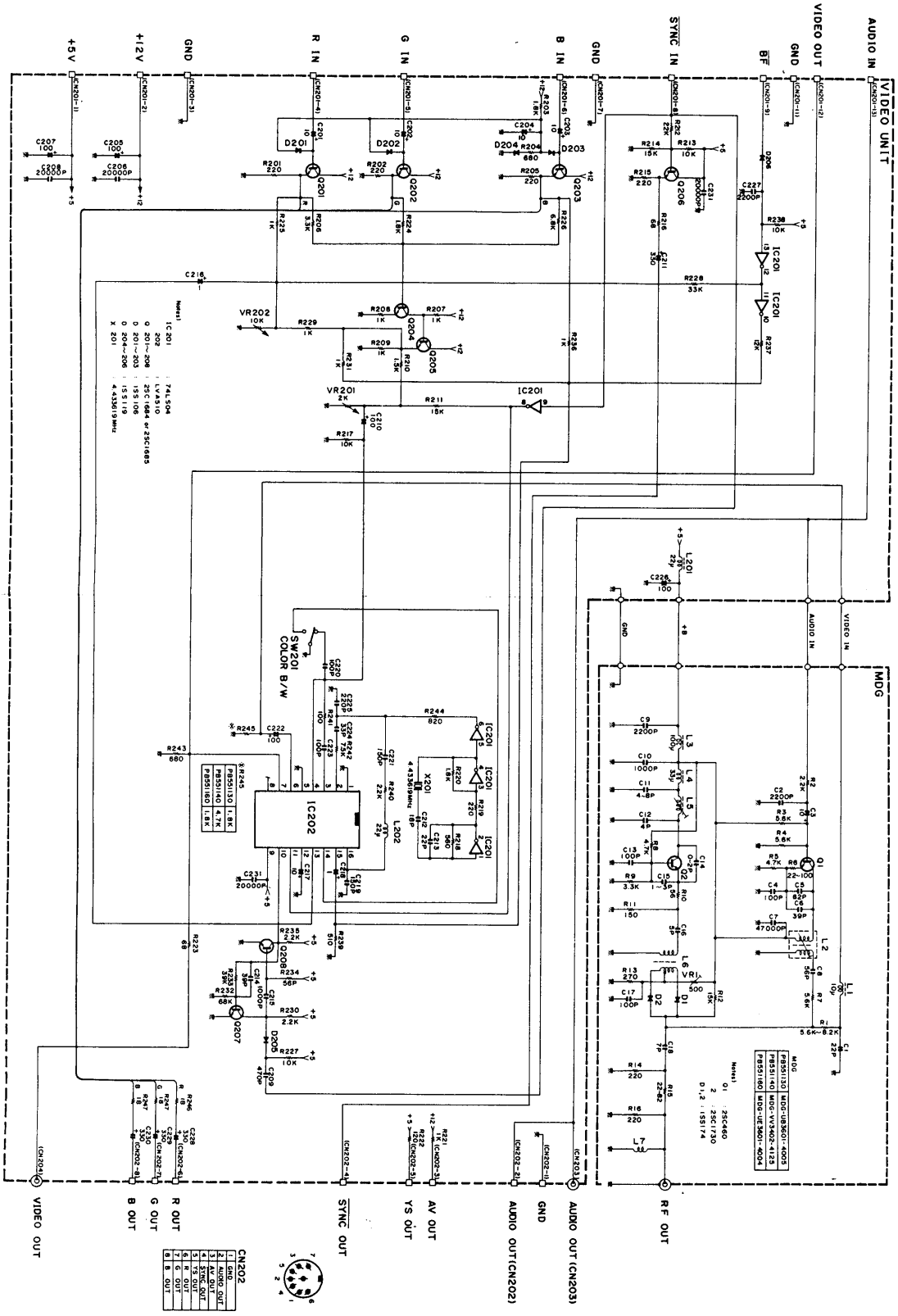


Notes)
 Q201, 202, 204, 205, 207, 208, 210 : 2SC1684 or 2SC1685 or EQUIVALENT
 Q203, 206, 209 : 2SA564 or EQUIVALENT

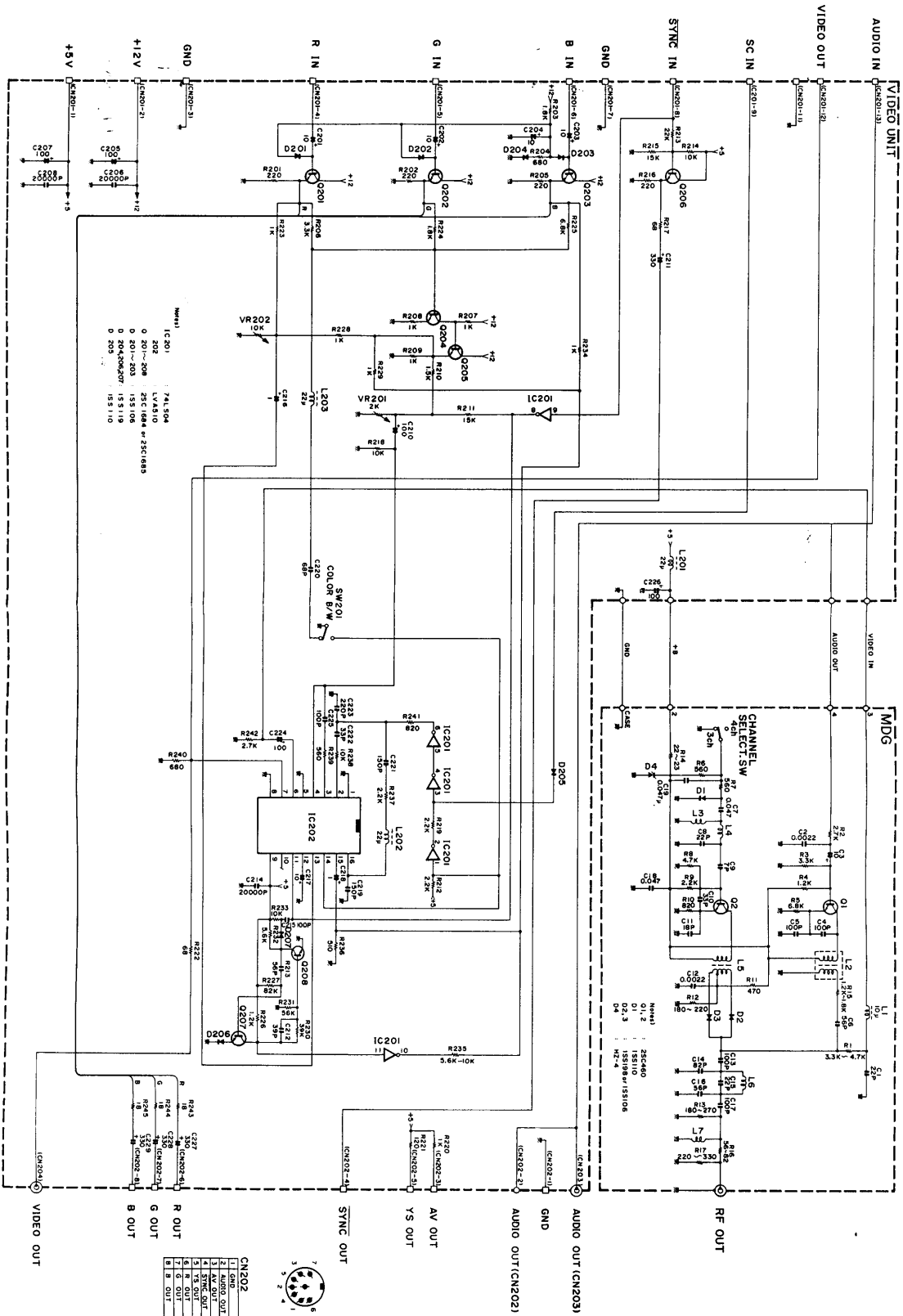
| | |
|---|-----------|
| 1 | GN0 |
| 2 | AUDIO OUT |
| 3 | AV OUT |
| 4 | SYNC OUT |
| 5 | YS OUT |
| 6 | R OUT |
| 7 | G OUT |
| 8 | B OUT |



VIDEO UNIT OVERALL CIRCUIT DIAGRAM
 • PB551130 (CX-SMILE), PB551140 (CX-SMILE A), PB551160 (CX-SMILE B, P)



● PB550990 (CX-SM11C)



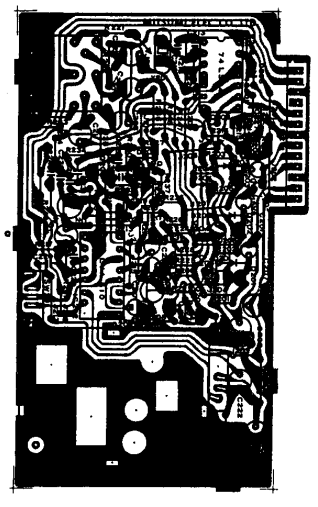
CN202

| | |
|---|-----------|
| 1 | GND |
| 2 | AUDIO OUT |
| 3 | VIDEO OUT |
| 4 | SYNC OUT |
| 5 | YS OUT |
| 6 | B OUT |
| 7 | R OUT |

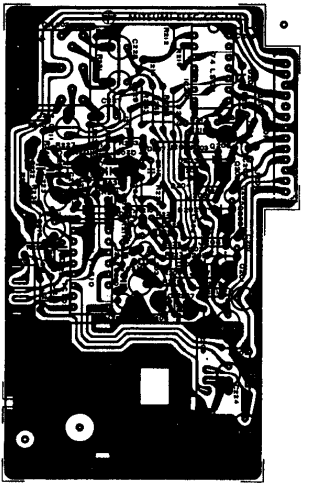


■ CX-5MII CIRCUIT BOARD

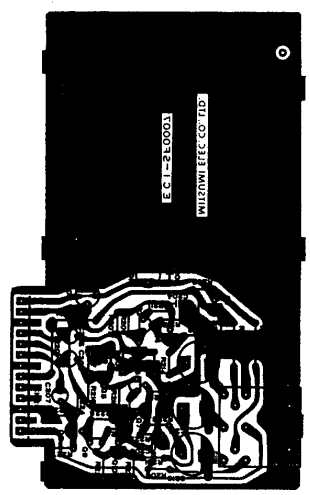
- PB551130 (CX-5MII E)
- PB551140 (CX-5MII A)
- PB551160 (CX5MII F, B, P)



- PB550990 (CX-5MII C)

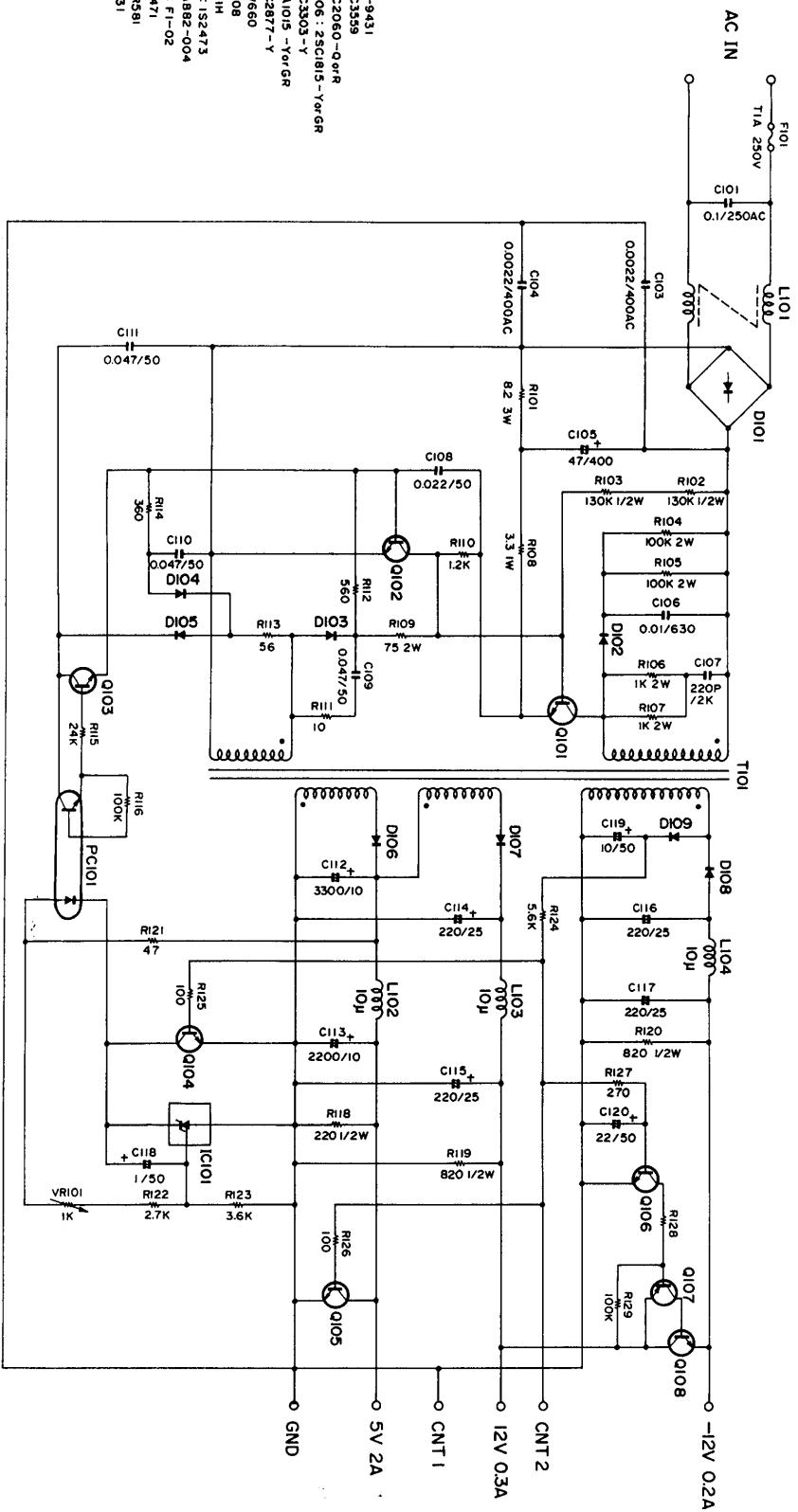


- PB551150 (CX5MII F) old

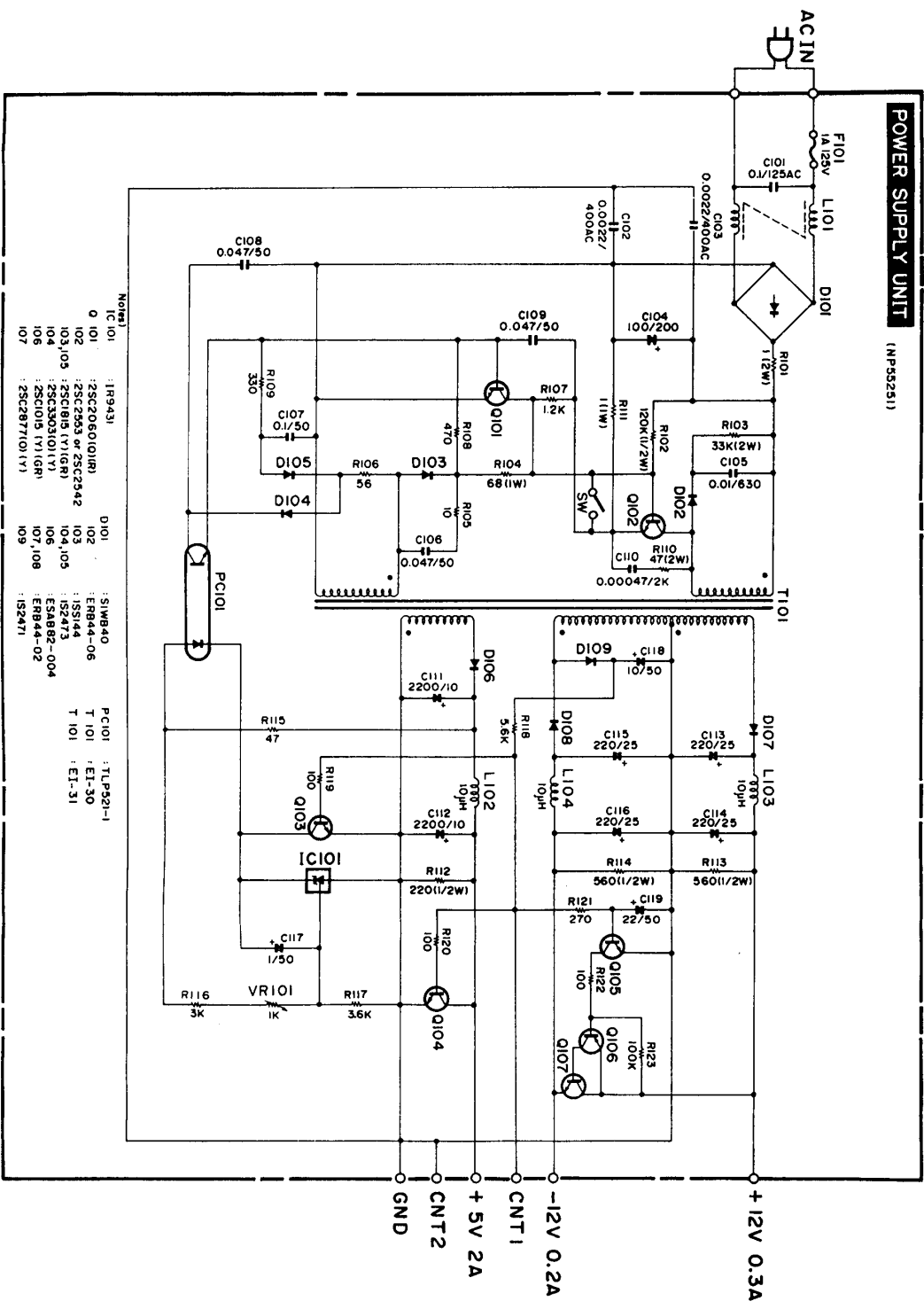


POWER SUPPLY UNIT OVERALL CIRCUIT DIAGRAM

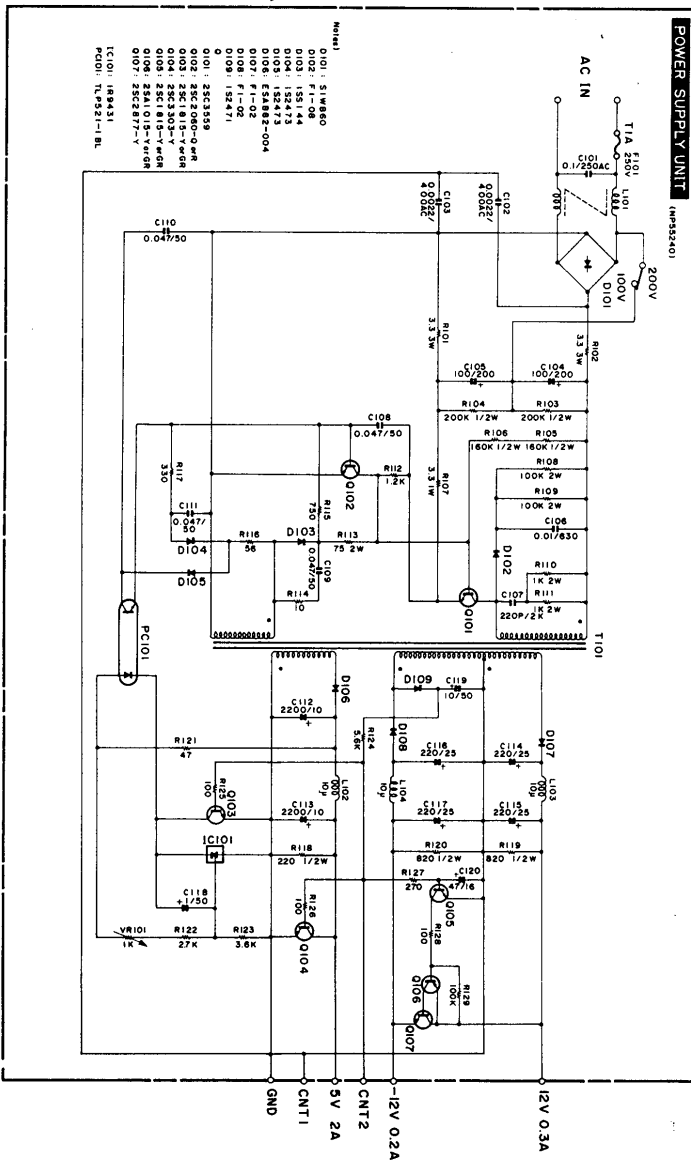
NP552200 (CX-5M E.A.F)



- Notes)
- IC101 : 1R-9431
 - Q101 : 2SC3359
 - Q102 : 2SC2060-QGR
 - Q103, Q104, Q106 : 2SC1815-YGR
 - Q105 : 2SC3303-Y
 - Q107 : 2SA1015-YGR
 - Q108 : 2SC2877-Y
 - Q101 : S1W660
 - D102 : FI-08
 - D103 : 1SS1H
 - D104, D105 : 1S2473
 - D106 : ESAB82-004
 - D107, D108 : FI-02
 - D109 : 1S2471
 - PC101 : TLRS81
 - T101 : EF-51



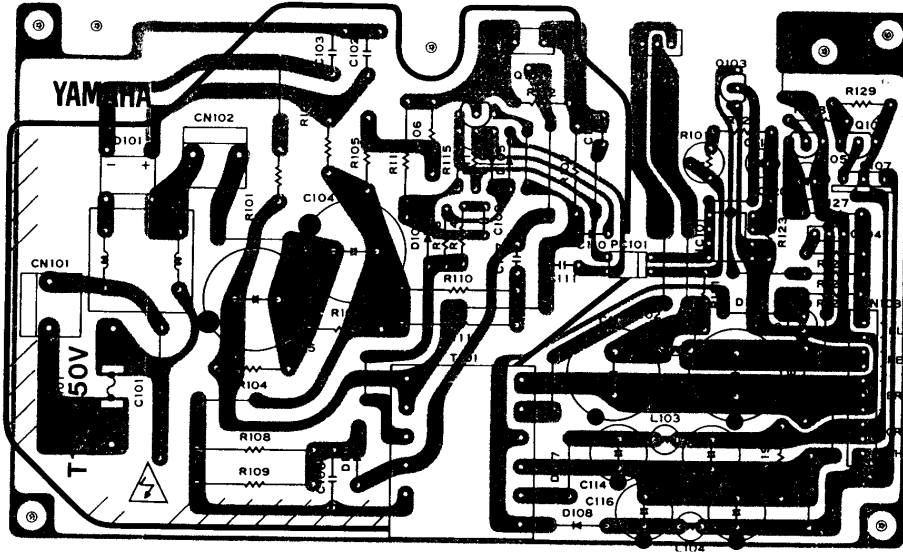
● NP552400 (CX-5M B.P)



SUPPLY UNIT CIRCUIT BOARD

POWER SUPPLY UNIT CIRCUIT BOARD

● NP552400 (CX-5M B,P)



● NP552500 (CX-5M C)

