ARP ODYSSEY

SERVICE MANUAL

MODELS 2800 THROUGH 2823

SECTION 1 PRELIMINARY INFORMATION

1.1 Introduction

This service manual is divided into three major sections: A) Circuit Descriptions, B) Trim Procedures, and C) Board Test Points. The circuit descriptions should be consulted when a problem is suspected in a particular area of the instrument. The trim procedures should be used to verify calibrations or when a component has been changed. The board test points are a quick reference to verify circuits with suspected problems and should be checked whenever a problem has been identified.

1.2 Board Identification

Three types of Odyssey models have been produced: 1) 2800, 2) 2810-2815 and 3) 2820-2823. The model and serial number are located at the rear or bottom of the Odyssey chassis. Except for 2800, a typical number might read: 2813-0490. For model 2800, the first two digits of the serial number denote the model, such as: 28490. Listed below are the board identification numbers for each model; they will be referenced in the service manual by model number for easy identification.

ODYSSEY-I

Model 2800

Board: A-1
B-1
C-1
PWR SUP-1

ODYSSEY-II

Model 2810-2813

Board: A-II
B-II
C-II
PWR SUP-II

Model 2820-2823

Board: A-II (with PPC)
B-II
C-II
PWR SUP-II

Note: Some Odyssey-2 models employ the older style Board B-I.

1.3 Model Changes

The Odyssey has undergone major cosmetic and electrical changes since its original production in 1972, however, the functional capabilities have remained virtually unchanged. The following are the most noticeable physical differences among models:

MODEL 2800

Black and white face panel (some later models have black and gold face panels).
Pitch Bend knob
No Factory installed interface jacks.
Wrap around vinyl bottom cover.

MODEL 2810-2813

Black and gold face panel.
New style power switch.
Factory installed interface jacks.
Pitch Bend knob. (Some later models have PPC.)
Wrap around vinyl bottom cover.

MODEL 2820-2823 (current model, Odyssey '78)

Black and orange face panel.
Steel chassis
Leather endblocks
PPC

The major electrical changes found in the Odyssey-II as compared to the Odyssey-I are:

1. Uses 24db/octave filter in place of 12db/octave.
2. Improved VCO design for better tracking and stability.
3. Improved power supply regulation.
4. Improved keyboard current source for CV generation.
5. Improved S/H memory circuit design.

1.4 Revisions/Changes

1.4.1 MODIFICATION KITS

The following modifications are available from the Factory for updating older style Odysseys:

Modification	For Model	Kit No.
Interface Jacks	2800	6800101
PPC	2810-2815	6800301
PPC	2800	6800501

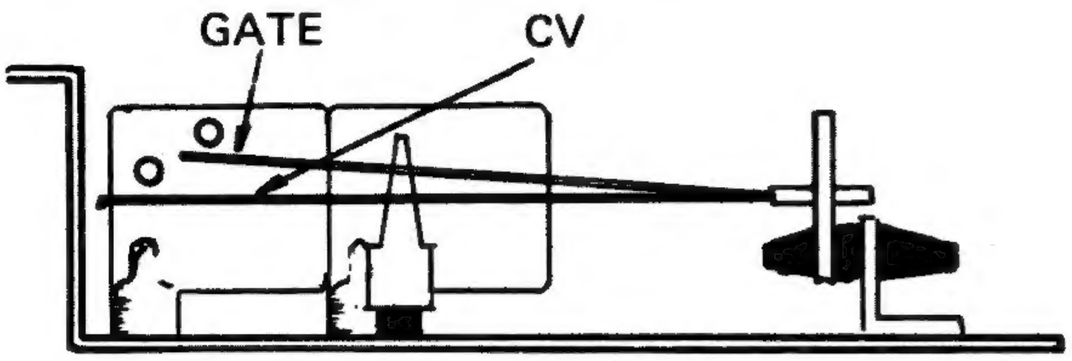
1.4.2 KEYBOARD CONVERSION

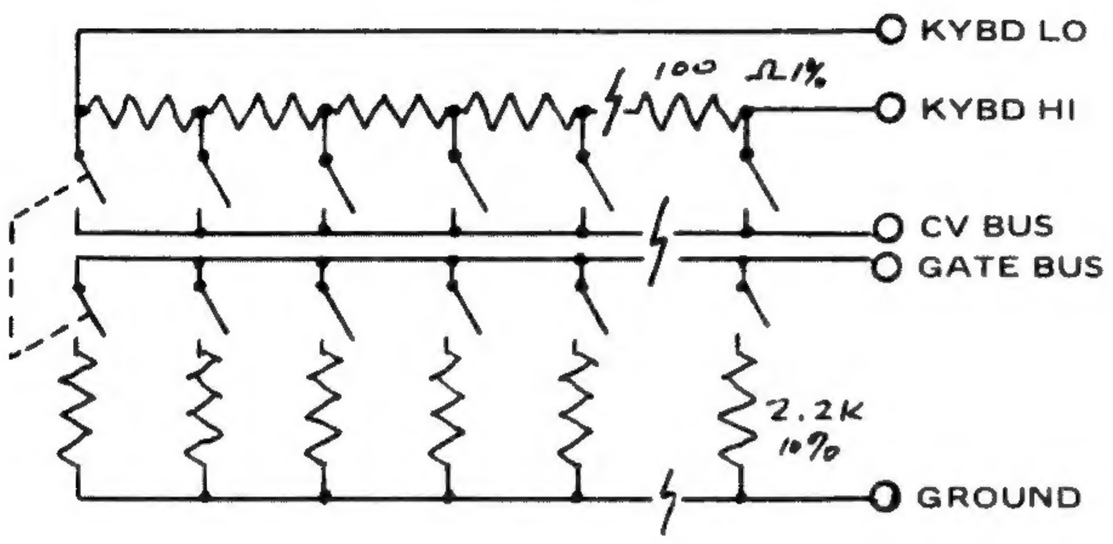
The Odyssey-II is designed to be used with a two bus keyboard. When an Odyssey-II is used with a three bus keyboard, an interface board is inserted on the molex pins on Board A-II to make the keyboard compatible with the electronics. Illustrated below

are the two types of keyboards employed in the Odyssey and their schematics.

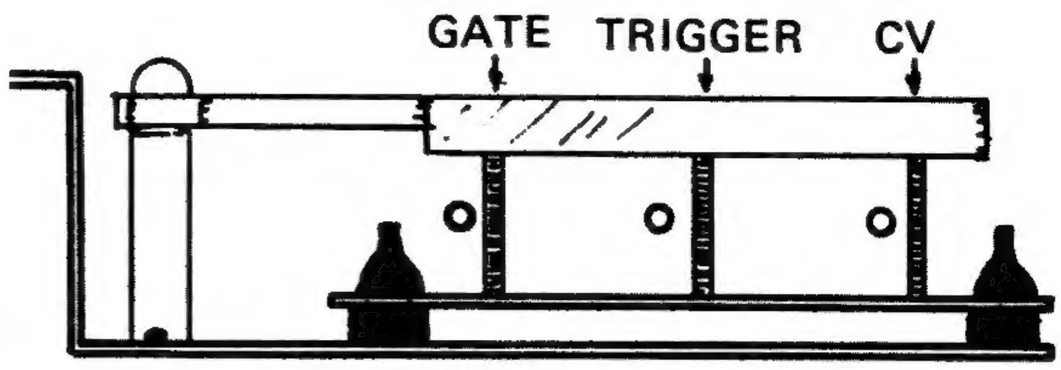
TWO BUS KEYBOARD Models 2810-2813

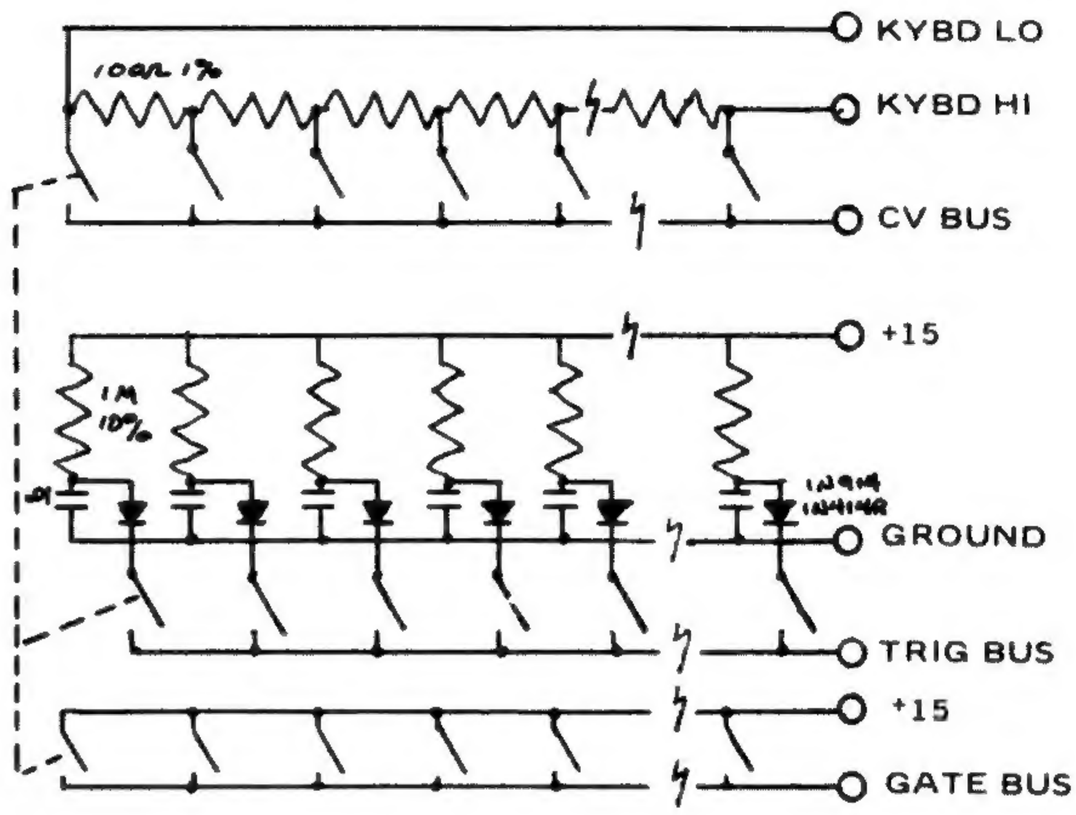
(Later models use cat-whisker style shown in maintenance section 6.2. Schematic remains the same.)



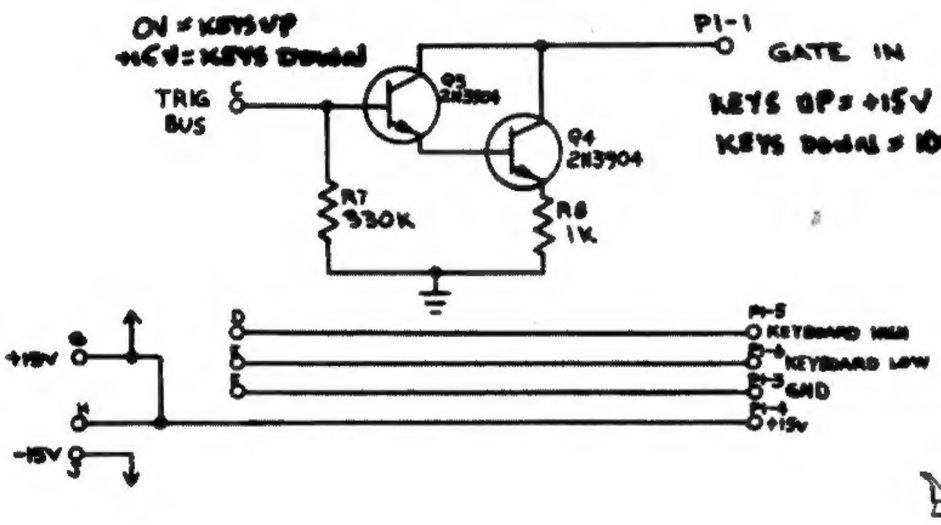


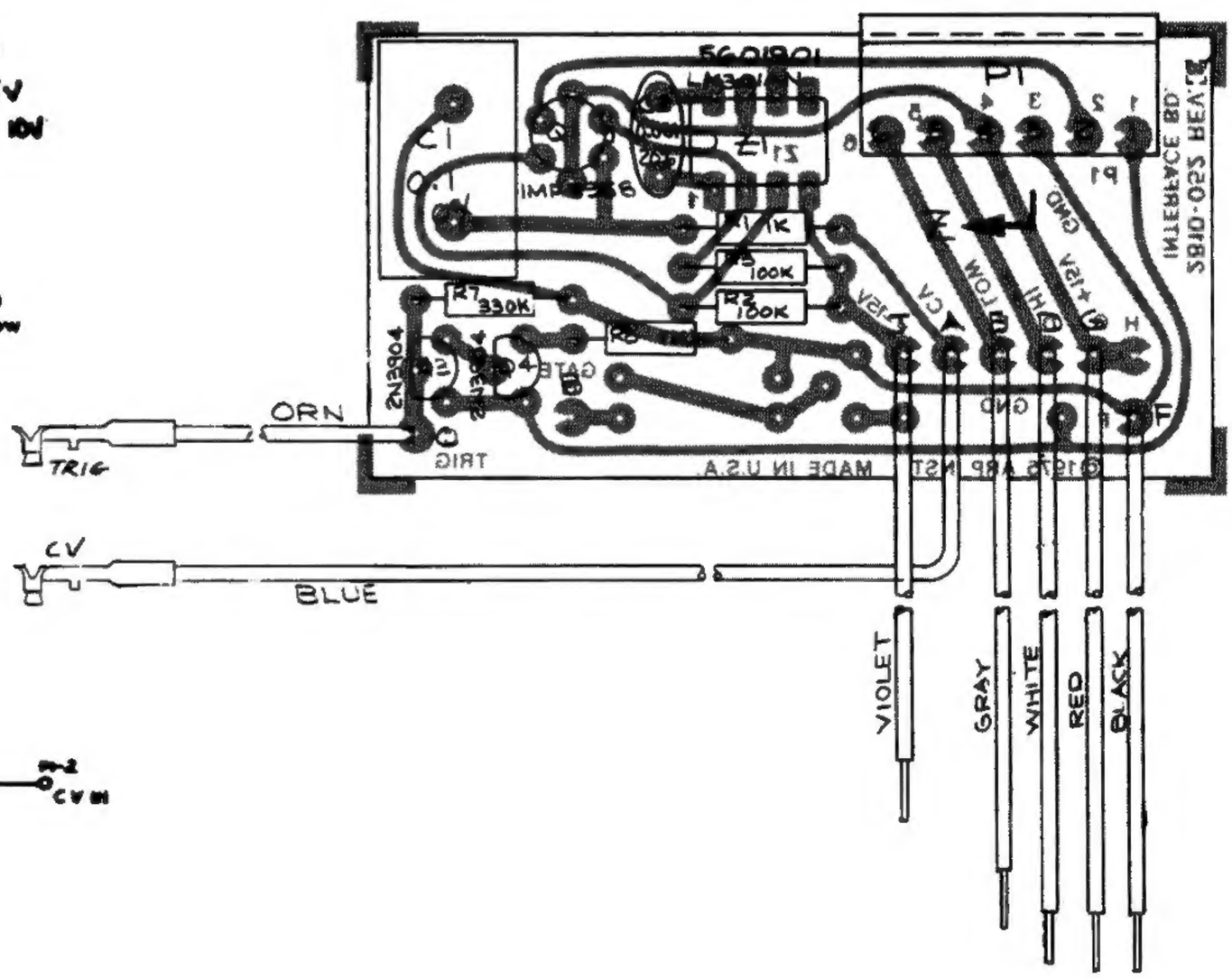
THREE BUS KEYBOARD

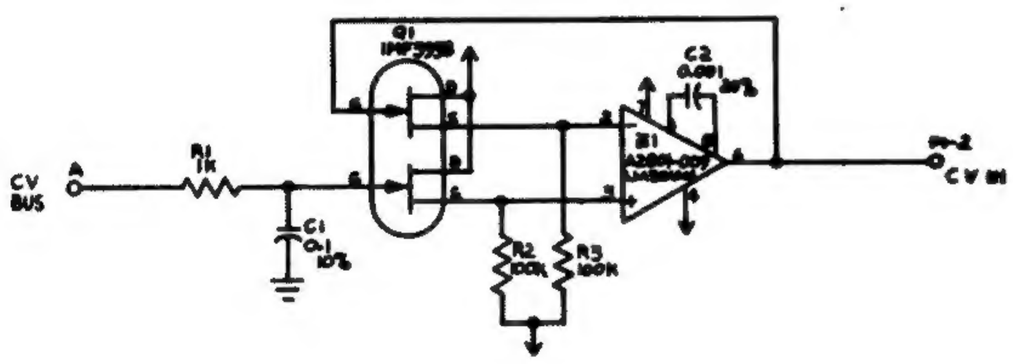




THREE BUS CONVERSION BOARD



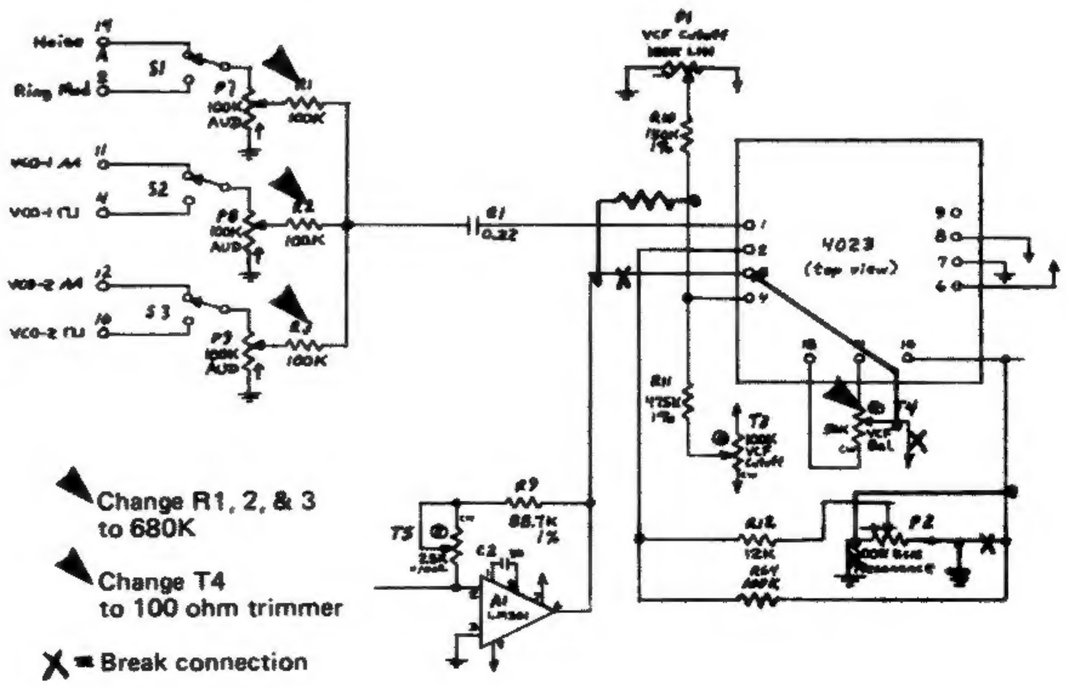




1.4.3 TYPES OF VOLTAGE CONTROLLED FILTERS

The 4023 voltage controlled filter is no longer available from the Factory. Instead, the newer 4075 filter can be used to replace the 4023 with the following modification (see Field Change Notice 007):

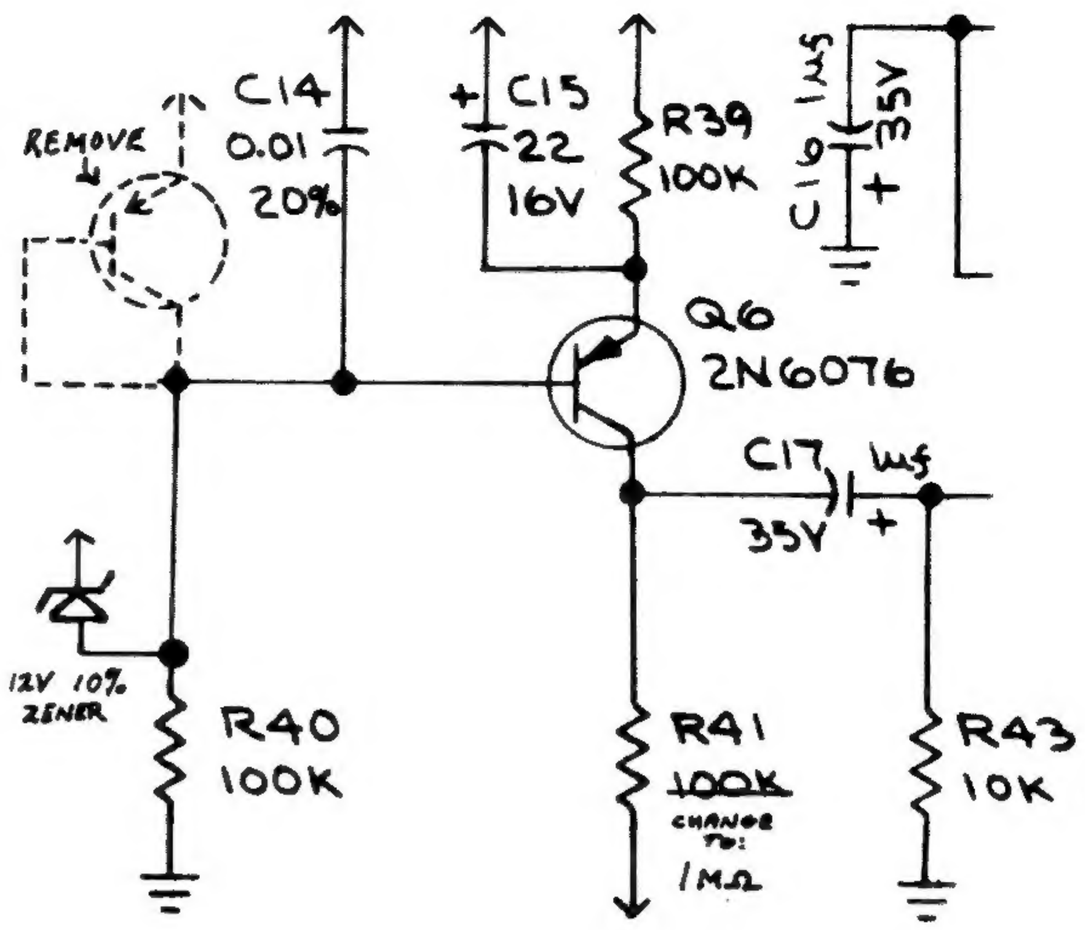
The earlier model Odyssey-IIs used a 4035 voltage controlled filter, which has since then been replaced by the 4075. No modifications are necessary when replacing a 4035 filter with a 4075.



1.4.4 NOISE MODIFICATION

The newer style Odysseys use a zener diode as a noise source instead of a noise transistor. Defective noise transistors can be replaced with a zener diode, provided the following circuit modification is performed:

Zener diodes tend to produce a greater spectrum of white noise with little or no noise break-up.



1.9 Specifications

Noise Generator
Noise spectrum types: White and Pink

Voltage Controlled Oscillators
Waveforms: Sawtooth, Square, Pulse, Dynamic Pulse
Frequency range: VCO 1 in low freq. mode, .2 Hz to 20 Hz; VCO 1 and VCO 2 (audio range), 20 Hz to 20 KHz
Warm up drift: 1/30 semitone from turn on max.
Pulse width: 50% to 5%
Pulse width modulation: ADSR, +45%; LFO, +15%
Voltage controlled response: 1V/oct.
Maximum frequency shifts: LFO sine wave, +½ oct.; LFO square wave, +1.5 oct.; ADSR +9oct.; S/H +2 oct.

Note: VCO 1 is a low note priority; VCO 2 is high note priority

Transpose
Positions: Down 2 octaves, normal, up 2 octaves

Pitch Bend
Frequency shift: About + 1 oct. (exactly 1 octave on Odyssey-2)

PPC
Frequency shift: About 5 semitones ±1 semitone.

Portamento
Maximum speed: About .01 msec./oct.
Minimum speed: About 1.5 seconds/oct.

Ring Modulator
Type: Digital
Input signals: VCO 1 and VCO 2 pulse waves

Voltage Controlled Filter
Type: Low pass
Frequency range: 16 Hz to 16 KHz
Maximum usable Q: 30
Resonance ½ to self oscillate
Voltage controlled response: 1V/oct.

Voltage Controlled Amplifier
Dynamic Range: 80dB

Sample and Hold
Command sources: Keyboard or LFO trigger
Sampled signals: VCO 1 square wave and sawtooth wave, VCO 2 square wave and pink noise

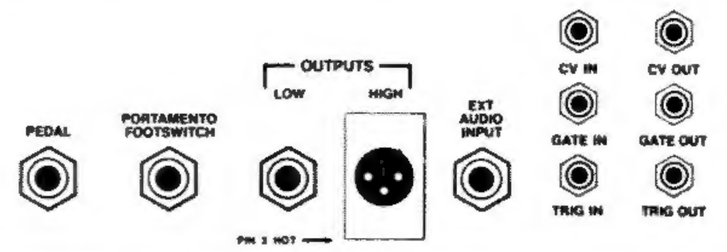
ADSR Envelope Generator
Attack time: 5 msec. to 5 seconds
Decay time: 10 msec. to 8 seconds
Sustain level: 0 to 100% of peak
Release time: 15 msec. to 10 seconds

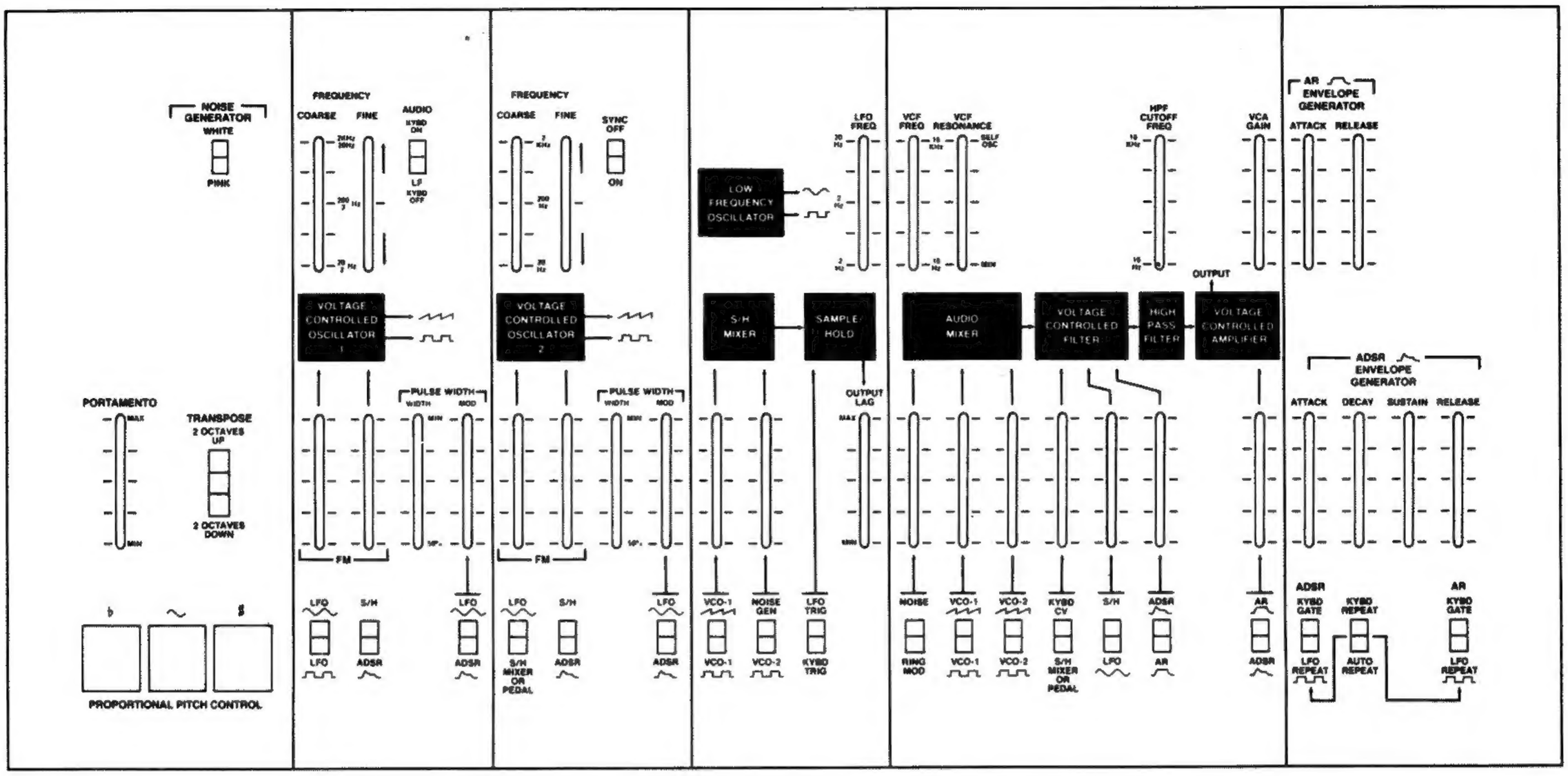
AR Envelope Generator
Attack time: 5 msec. to 5 seconds
Release time: 10 msec. to 8 seconds

Audio Outputs
High level: 2.5VPP max.; 100K impedance
Low level: .25VPP max.; 10K impedance

Interface Jacks
Keyboard CV IN/OUT: 1V/oct.
Gate OUT: +10V, key down; 0V all keys up
Gate IN: +8V minimum
Trigger OUT: +10V pulse on key depression, 10 microsec. duration
Trigger IN: +8V pulse min., 10 microsec. duration minimum
External Audio Input: 500 millivolts for full output

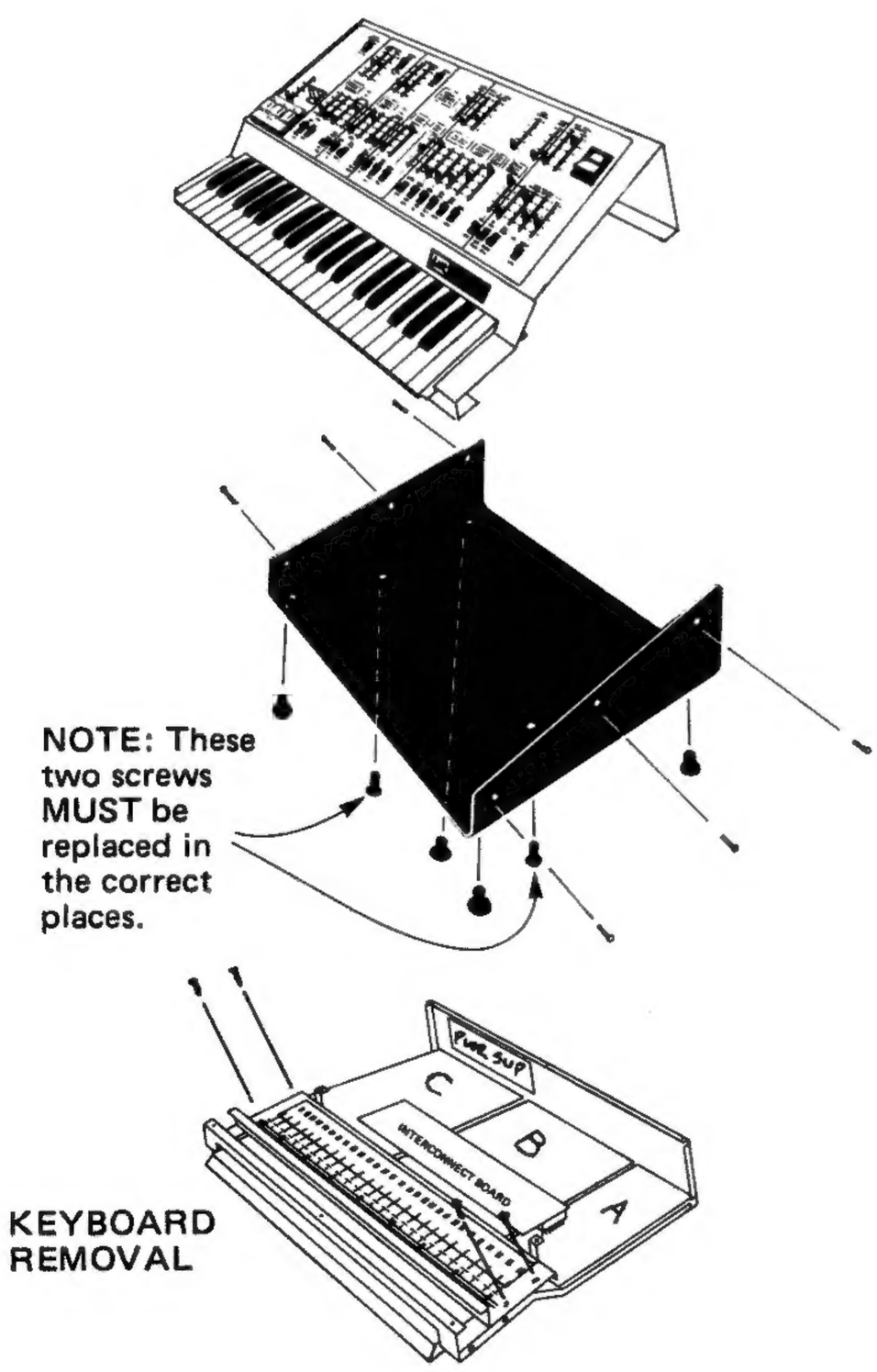
Front and Back Panel Configuration
Model 2823





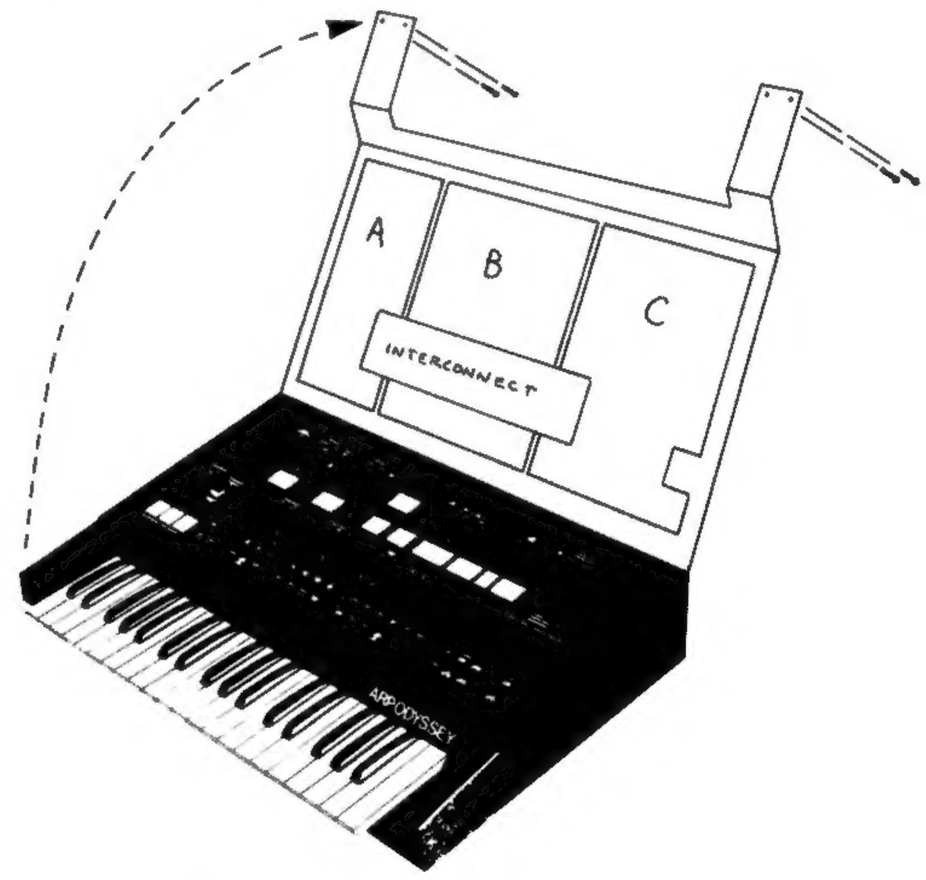
ASSEMBLY/DISSASSEMBLY

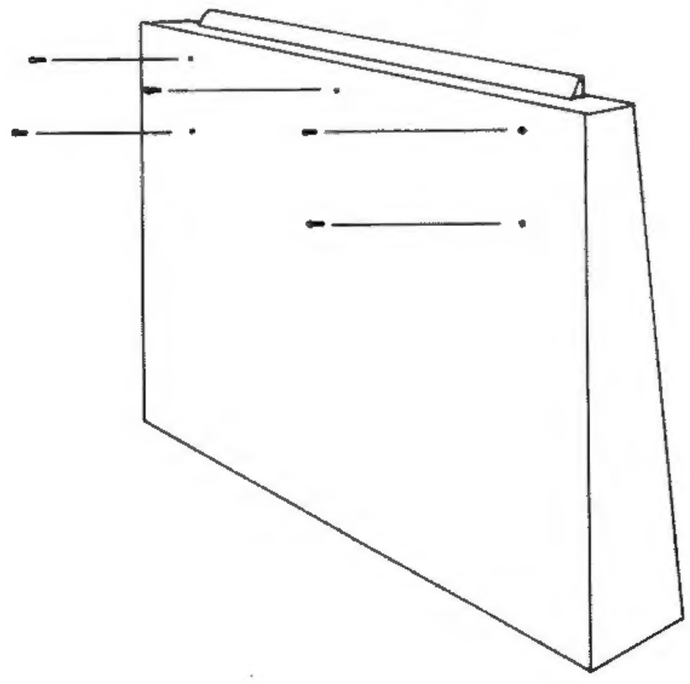
MODEL 2800 - 2815



KEYBOARD REMOVAL

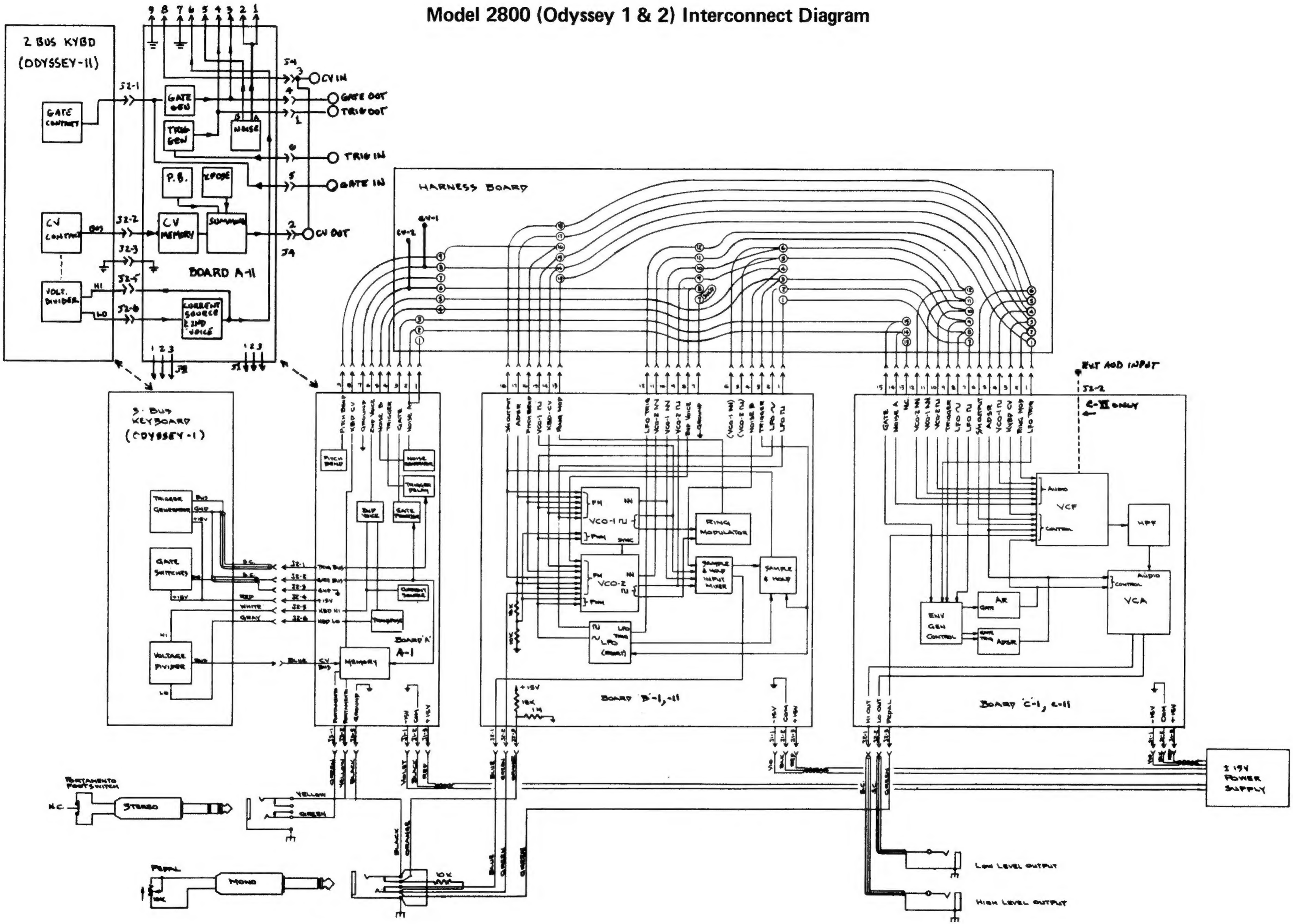
MODEL 2820 - 2823



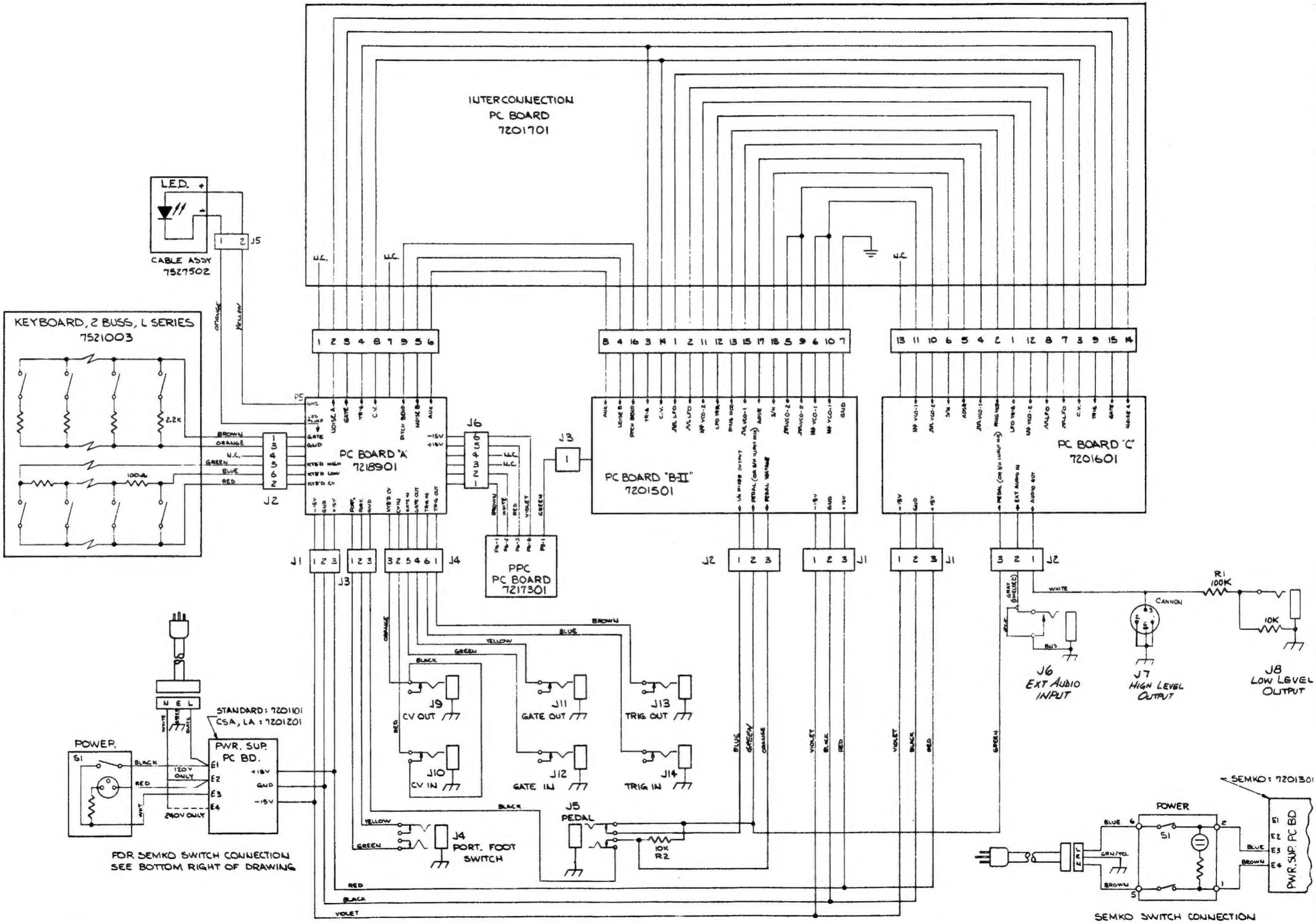


KEYBOARD REMOVAL

Model 2800 (Odyssey 1 & 2) Interconnect Diagram



Model 2820 - 2823 Interconnect Diagram



2.1.1 Trigger Circuit

Each key on the keyboard has its own capacitor-resistor-diode network. The capacitors are normally charged to +15 volts until a key is depressed at which time the capacitor discharges through the diode creating a trigger pulse on the trigger bus rod. Q1 through Q4 are a monostable multivibrator which delays the trigger pulses 15 milliseconds to allow the gate and CV to stabilize.

2.1.2 PITCH BEND

P1, the pitch bend control, supplies a control voltage to both VCOs on Board B. CR4 and CR5 create a 'dead' zone when the control is centered.

2.1.3. CURRENT SOURCE

Q5 supplies constant current to a resistor divider chain made up of thirty-six 100 ohm resistors connected in series. The CV contacts are located at the junction of each of the 100 ohm resistors to supply a specific voltage to the control voltage memory when a key is depressed. There is a three volt drop across the entire resistor chain, or one volt per octave. T1, the Volts/Octave trimmer, adjusts the current through the resistor chain to produce the correct voltage drop across the keyboard.

2.1.4. TRANSPOSE SWITCH

Half of the transpose switch is connected to the bottom end of the resistor chain to, in effect, add two or four octaves worth of resistance (about 1200 or 2400 ohms) to the resistor chain. This raises the control voltage level supplied to the CV memory. The following chart summarizes the CV output for low 'C' and high 'C' on the keyboard for each of the transpose switch positions:

TRANSPOSE SWITCH:	LOW 'C'	HIGH 'C'
DOWN 2 OCT.	0 V	+3 V
NORMAL	+2 V	+5 V
UP 2 OCT.	+4 V	+7 V

The remaining half of the transpose switch compensates the second voice control voltage for the difference in the resistor chain resistance.

2.1.5 CV Memory Circuit

Q6 and A1A are a FET input op amp which buffers the voltage from the keyboard CV bus and supplies it to the memory circuit through R23 and CR3. When a key is depressed, +15 volts is supplied from the keyboard gate through CR2 and R21 which reverse biases CR3 and allows Q7 to conduct. The control voltage from A1A is then allowed to charge the memory capacitor, C8. When a key is released, Q7 turns off to prevent C8 from discharging. Q8 and A1B are a FET op amp which buffers the control voltage on C8 and supplies it to the control input of VCO 1 and VCO 2 on Board B and to the VCF on Board C.

2.1.6 Second Voice CV Generator

When two or more keys are depressed, a section of the resistor chain is effectively shorted out which drops the voltage at the top end of the resistor chain. This voltage drop corresponds to the 'voltage difference' between two held keys. A2A is a unity gain buffer which monitors the voltage at the top of the resistor chain and supplies it to A2B. A2B sums the voltage from A2A with the voltage supplied by R31 and R30. These resistors are selected to produce zero volts on the output of A2B when either no keys or one key is depressed.

When two or more keys are depressed, the voltage at the top end of the resistor chain drops, which, in turn, decreases the voltage supplied to Z2B. Z2B then supplies the difference voltage to the control input of VCO 2 where it is summed with the control voltage from the CV memory circuit. This summation allows VCO 2 to be controlled by the highest key depressed. Since VCO 1 is fed the control voltage from the CV memory only, its pitch is controlled by the lowest key depressed.

2.1.7 Noise Generator

The noise generator circuit produces 10VPP white and pink noise signals which are supplied to the VCF audio input and the S/H mixer. The noise is obtained by amplifying a reversed biased transistor junction (Q9) in avalanche breakdown. Q9 is a transistor selected for optimum avalanche characteristics; and therefore, has good noise producing capability. A3 amplifies and clips the noise signal. A3 filters the noise to provide pink noise to the VCF and S/H.

2.2.1 Sample & Hold (S/H)

The sample and hold circuit provides a DC voltage output by sampling and storing the instantaneous voltage level of signals on its input each time a trigger pulse is provided. This stored voltage is held until the next trigger pulse occurs. Signals which are to be sampled and applied to pin 3 of A3. A3 is an operational transconductance amplifier (OTA), which is used as a gated voltage follower: when a pulse is applied to pin 5 of Z3, capacitor C7 charges to the voltage level on pin 3. This voltage level is held until another pulse is applied to pin 5. Q3 buffers the voltage on C7 and supplies it to A2B through the lag slider (P16). A2B is a unity gain buffer. The sample and hold output is supplied to the control inputs of VCO 1 and VCO2 and to the VCF on Board C.

2.2.2 Low Frequency Oscillator (LFO)

The LFO produces a triangle and square wave output in a frequency range from about .1 Hz to 25 Hz. Z1A and C3 are an integrator which charges from current passing through R11. Z1B is a hysteretic switch whose output switches from -15 volts to +15 volts when the output of Z1A reaches +5 volts. This then reverses the direction of current through R11 and the rate control (Z5) and thus the direction of integration at the output of Z1A. When the output of Z1A reaches -5 volts, the output of Z1B switches back to -15 volts and the cycle repeats.

An LFO reset pulse is supplied from the keyboard every time a key is depressed. Q1 and Q2 are turned on momentarily by the keyboard trigger pulse to discharge the integrating capacitor (C3) thus reinitializing the LFO to zero.

2.2.3 Voltage Controlled Oscillators (VCO)

Oscillator circuit (VCO 1 & 2): Control voltages from the keyboard, initial frequency and fine tune sliders, pitch bend (2800 only) and both FM input sliders are summed on the base of Q4. Q4 and Q5 are a linear voltage to exponential current generator; for every volt applied from the keyboard, the current through Q5 will double. C12 is the integrating capacitor; it is initially charged to +15 volts and discharges through R51 and Q5 toward ground. Q5 determines the discharge time of the capacitor and therefore the period of oscillation. Z1D is a CMOS nand gate used as a comparator. When the voltage on pin 12 of Z1D falls below +7.5 volts, the output of Z1 (pin 11) changes from zero volts to +15 volts which turns on Q10, Q7 and Q6. Q6 recharges the integrating capacitor (C12) to +15 volts to start the cycle over again.

Q8 buffers the sawtooth wave on C12 and supplies it to the sawtooth to pulse converter and Q9, the output emitter follower. The oscillator circuit for VCO 2 is the same as VCO 1. When the 'SYNC' switch is on, the reset pulse from VCO 1 is applied to Z2D which causes VCO 2 to reset at the same time as VCO 1, regardless of the voltage level on pin 12 of Z2D. The waveform on the output of VCO 2 is then synchronized with VCO 1.

Sawtooth to square wave converter: Z1A and Z1B are a R-S flip-flop with pin 8 used as a comparator. The reset pulse from Z1C is supplied to pin 1 and the sawtooth wave to pin 8. As the sawtooth wave is raised above the zero reference by the pulse width trimmer and sliders (T2, P8 and P9) the flip-flop will change state on a different point of the sawtooth slope resulting in a different pulse width. With all of the pulse width sliders on the front panel at minimum, the pulse wave should be square (50% duty cycle). The pulse wave output is supplied to the audio input of the VCF on Board C and to the ring modulator circuit on Board B.

2.2.4 Ring Modulator

The ring modulator utilizes two CMOS nand gates (Z1B and Z2B) and Q18 in an exclusive 'or' function. Square waves from VCO 1 and VCO 2 are supplied to pin 5 of Z1 and Z2 and the output is taken from the emitter of Q18.

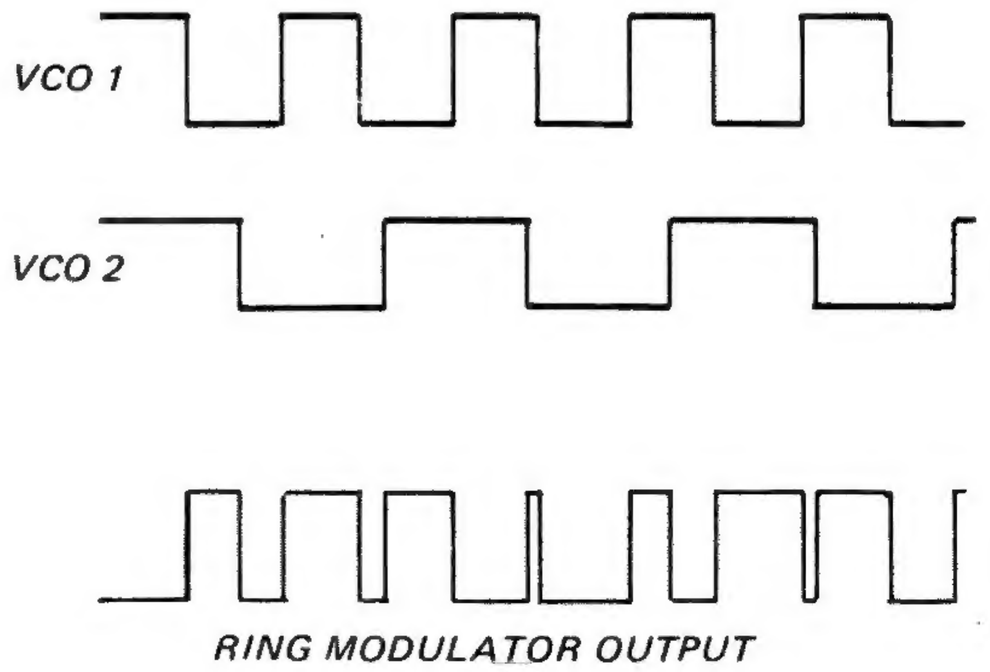
GATE TRUTH TABLES

NAND GATE

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

EXCLUSIVE OR

A	B	C
0	0	0
0	1	1
0	1	1
1	1	0



RING MODULATOR OUTPUT

2.3.1 Voltage Controlled Filter (VCF)

Audio signals from both VCOs, the ring modulator, and the noise generator are applied to the audio input of the voltage controlled filter (pin 1, 4023) through C1. Control voltage from the S/H, LFO, KYBD CV, and the envelope generators are summed and inverted by A1. The control input of the VCF accepts negative going control voltages; as the voltage on pin 3 of the 4023 module is decreased, the filter cutoff increases. Signals on the output of the VCF (pin 10) are fed back to the resonance input (pin 2) via the resonance slider, (P2).

2.3.2 Voltage Controlled Amplifier (VCA)

Audio signals from the VCF are processed through the high pass filter (C3, R13 and P3) and connected to the noninverting input of A3. A3 is an operational transconductance amplifier (OTA) whose gain is a function of the current supplied to pin 5. Control voltages from the two envelope generators and the VCA gain slider are connected to Q1 which supplies current to the OTA. T2, the control reject trimmer, balances the inputs of the OTA to minimize the effect of control voltages on the audio output of the VCA.

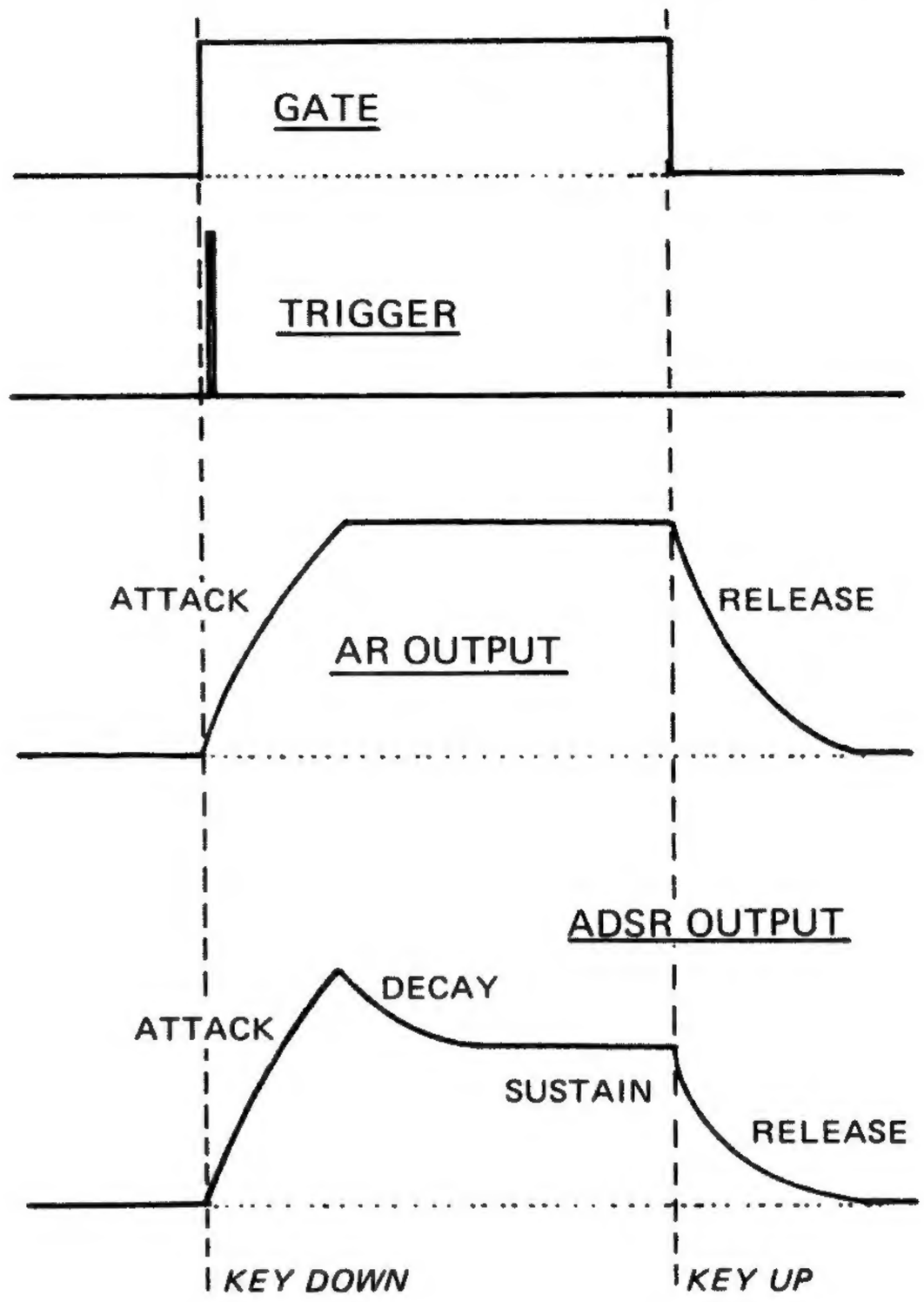
2.3.3 AR Envelope Generator

The Attack-Release envelope generator produces a control voltage with variable rise and fall times. It is used to control the VCF or the VCA. When a gate voltage is supplied by the keyboard or the LFO through S10, Q4 turns on which charges capacitor C7 through P5, R32 and CR5. The position of P5 (Attack Slider) determines the time C7 takes to charge up. When the gate voltage is removed, Q4 turns off which allows Q5 to turn on. The voltage on C7 then discharges through CR6, P6, R31, and Q5. P6 (Release slider) sets the release time. Q6 and Q7 buffer the voltage on C7 and supply it to the VCA and VCF.

2.3.4 ADSR Envelope Generator

The Attack-Decay-Sustain-Release envelope generator produces a control voltage with variable rise and fall times. It is used to control the VCF or the VCA and a gate and trigger signal must be supplied from the keyboard or LFO to start the ADSR voltage rising.

Attack: When a gate signal (+10 volts) is supplied through S8, Q8, Q9 and Q10 turn on which then allows Q16 to turn off. With Q16 off, a trigger applied through C9 and R55 will momentarily turn



NOTE: The ADSR is initiated with a gate and trigger voltage, and the AR envelope requires only the gate.

on Q18 and Q17. Q17 then supplies +15 volts through CR18, CR19, CR17 and R57 to hold Q18 on. Q18 and Q17 (the attack latch) now supplies +15 volts through the attack slider (P4), R43, and CR9 and charges up the integrating capacitor, C8.

Q12, Q13, and Q14 buffer the voltage on C8 and provides it to the VCA and VCF. Q15 is the peak detector which monitors the output of the ADSR. When the ADSR voltage reaches its maximum, (about +10 volts), Q15 will turn on and provide this voltage to the base of Q16 through CR15. Q16 then grounds out the voltage on the base of Q18 to unlatch Q18 and Q17 and end the attack portion of the ADSR cycle.

Decay & Sustain: When the attack portion of the ADSR cycle has completed, the voltage on C8 is allowed to discharge through CR11, R47, and the decay slider (P15) to the emitter of Q11. The sustain slider (P16) sets the voltage level on the base of Q11. When the voltage level on the emitter of Q11 falls below the level on the base, Q11 turns off and prevents the voltage on Q8 from discharging further.

Release: When the gate is removed, the remaining voltage on C8 is discharged to ground through CR10, R44 and the release slider (P17).

2.4.1 Keyboard Current Source

The keyboard current source supplies constant current through thirty-six 100 ohm resistors connected in series. These resistors are a voltage divider supplying specific voltages for each key on the keyboard. The top end of the resistor chain is connected to J2-5 and the low end to J2-6. The current source produces a 3 volt drop across the entire keyboard, or 1 volt per octave. The keyboard voltage is fed to the CV memory via the CV bus rod.

Pin 7 of Z2A (high end of the resistor chain) is 0 volts when either no keys or one key is depressed and pin 6 of Z2A (low end of the resistor chain) is +3 volts. When two keys are depressed, the contacts and bus rod short out a section of the resistors in the divider chain which reduces the gain of Z1A thereby raising the voltage on Z2A pin 7. This voltage increase represents the voltage difference between two held keys. When this difference voltage is subsequently added to the control voltage at the control input of VCO 2 (Bd. B), high note priority control over the pitch of VCO 2 is produced.

2.4.2 Control Voltage Memory

Control voltages supplied from the keyboard CV bus are buffered by a unity gain amplifier, Z4A. This voltage is then supplied to the memory capacitor C8 through the portamento slider (R30) and the gating FET (Q3). Q3 is turned on by the gate generator circuit only while a key is depressed. Q4 and Z4B are a FET follower with high input impedance to buffer the voltage on capacitor C8. J3-1 and J3-2 are connected to the portamento footswitch jack so that the portamento slider can be bypassed while the footswitch is plugged in.

2.4.3 Pitch Bend

Pitch Bend: The Pitch Bend control supplies an offset voltage to Z2B to be summed with the control voltage from Z4B (CV memory). CR3 and CR4 create a 'dead' zone when the control is centered and R27 calibrates the output to exactly plus and minus a volt.

2.4.4 PPC

The PPC circuit contains three resistive carbon strips, three conductive rubber strips and various summing resistors. Each end of the carbon strip is connected to a designated voltage source, while each end of the conductive rubber is making contact with the summing resistors. As the PPC button is depressed, the conductive rubber makes contact at various points on the carbon strip which, in turn, provides various degrees of control voltage to the summing resistors. The conductive rubber is tapered so that maximum sensitivity is achieved at the top of the button.

2.4.5 Transpose Switch

Transpose: The transpose switch also supplies an offset voltage to Z2B to be summed with the control voltage from Z4B. R23 calibrates the output to exactly plus and minus 2 volts.

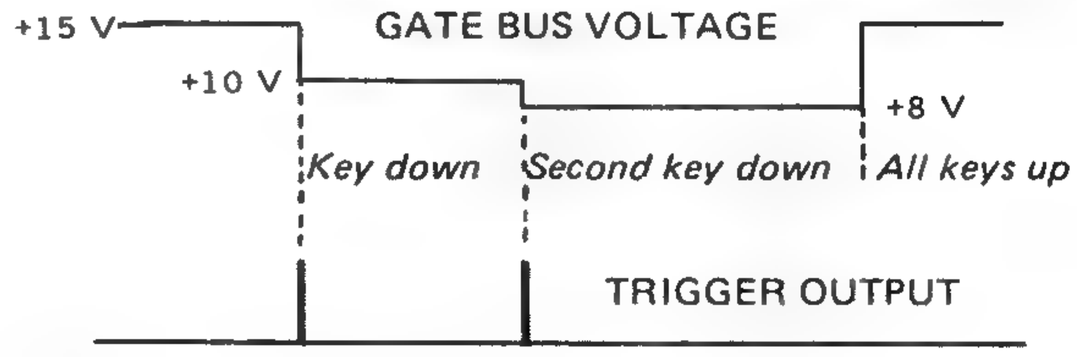
2.4.6 Summing Circuit

Summing: The output of Z4B is +3 volts when high 'C' is depressed and 0 volts when low 'C' is depressed. This control voltage is summed with the offset voltages from the transpose and pitch bend circuits on the input of Z2B. Z2B is a unity gain inverter whose output will be 0 volts with low 'C' depressed (pitch bend and transpose in the normal position) and +3 volts with high 'C' depressed. This voltage is supplied to the VCOs on Board B (pitch control) and the VCF on Board C (filter cutoff control).

2.4.7 Gate Generator

Each gate contact on the keyboard is connected to a 2.2K ohm resistor to ground. When a key is depressed the gate bus voltage drops from +15 volts to about +10 volts which turns on Q1. Q1 supplies two gate signals:

SIGNAL:	Key up:	Key down:	Location:
CV Memory	-15V	+15 V	Q1 coll.
Gate out	0 V	+10 V	J4-3



2.4.8 Trigger Generator

When a key is depressed, the gate bus voltage drops from +15 volts to about +10 volts. Additional key depressions will drop this voltage still further. These voltage transitions are coupled through capacitor C1 and R4 to Q2. Capacitor C2 is charged to +15 volts by Q2 when a key is depressed. Z1C and Z1D are CMOS nand gates (threshold is +7.5 volts). As C2

charges up, Z1D pin 11 will produce a 10 millisecond pulse (the pulse width is determined by C2) which is supplied to Q8. Q8 will conduct during the fall of the pulse from Z1D to provide a +10 volt trigger pulse (20 microsecond duration) to Board C and B. Trigger pulses from external sources are coupled through C20, Z1A and Z1B to Q8. Z1A and Z1B are connected in parallel to increase drive.

2.4.9 Noise Generator

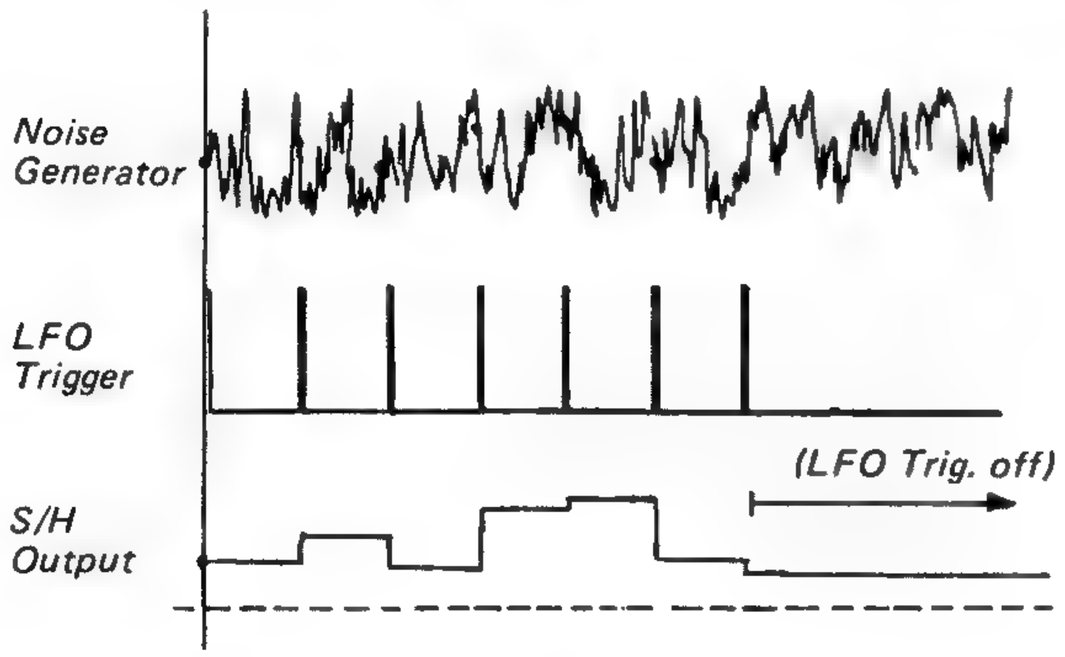
The noise generator circuit produces 10VPP white and pink noise signals which are supplied to the VCF audio input and the S/H mixer. The noise is obtained by amplifying a reversed biased transistor junction (Q5) in avalanche break down. Q5 is a transistor selected for optimum avalanche characteristics and therefore has good noise producing capability. Q6 is a buffer and Z5 amplifies and clips the noise signal. Z3 filters the noise to provide pink noise to the VCF and S/H.

NOTE: The more recent model Odysseys employ a zener diode instead of a noise transistor. See the revisions section 1.4.4 for the circuit change.

CIRCUIT DESCRIPTIONS (Board B-II)

2.5.1 Sample & Hold (S/H)

The sample and hold circuit provides a DC voltage output by sampling and storing the instantaneous voltage level of signals on its input each time a trigger pulse is provided. This stored voltage is held until the next trigger pulse occurs. Signals which are to be sampled are applied to pin 3 of Z1A. Z1A amplifies and buffers the signal and supplies it to Q1. When a trigger from either the LFO or the keyboard is received through C3, Q1 conducts just long enough for the memory capacitor (C1) to assume the new voltage level. Then Q1 turns off until another trigger is supplied. Q2 and Z2A are a FET op amp follower which buffers the voltage on C1 and provides it to the lag circuit (R15 and C2) and the output buffer (Z2B).



2.5.2 Low Frequency Oscillator (LFO)

The LFO produces a triangle and a square wave output in a frequency range from about .1 Hz to 25 Hz. Z5A and C7 are an integrator which charges from current passing through R33. Z5B is a hysteretic switch whose output switches from -15 volts to +15 volts when the output of Z5A reaches +5 volts. This change in output polarity then reverses the direction of current through R33 and the rate control (R34) and thus the direction of integration of the output of Z5A. When the output of Z5A reaches -5 volts, the output of Z5B switches back to -15 volts and the cycle repeats. An LFO reset pulse is supplied from Q4 every time a key is depressed. Q5 is turned on momentarily by the LFO reset pulse and discharges the integrating capacitor (C7) thus reinitializing the LFO output to zero.

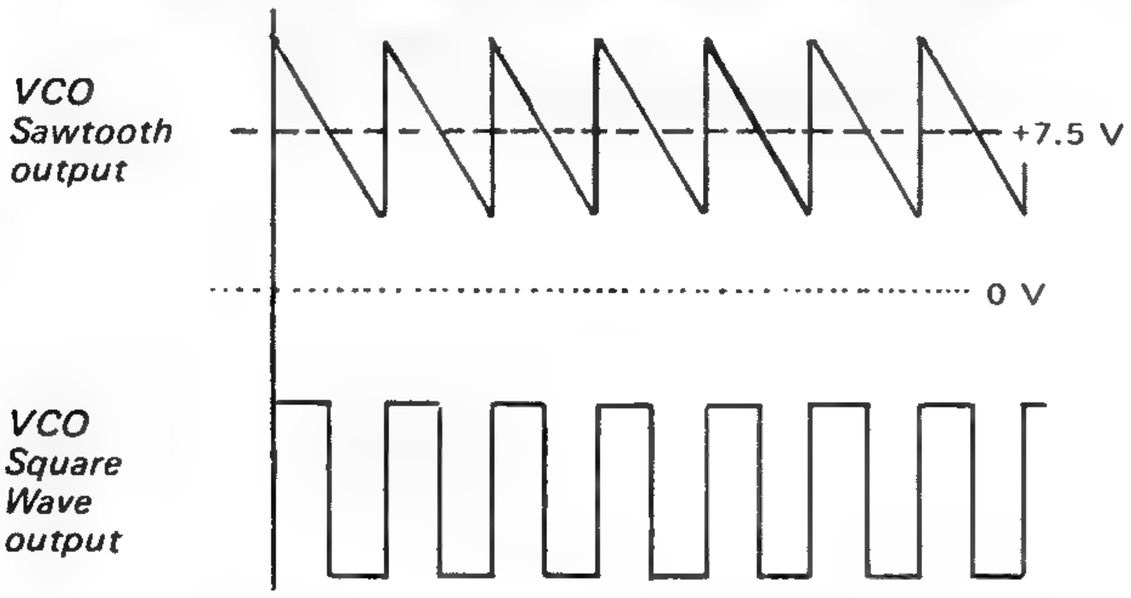
2.5.3 Voltage Controlled Oscillators (VCO)

Control voltages from the keyboard, initial frequency and fine tune sliders, the sample and hold circuit, LFO square wave and sine wave, and the ADSR are summed on the base of Q6. Q6 and Q7 are a linear voltage to exponential current generator; for every volt applied to the control input of the VCO from the keyboard, Q6 will conduct twice as much current. C11 is the integrating capacitor; it is initially charged to 15 volts and discharges through R61 and Q7 towards ground. Q7 determines the discharge current of the capacitor and therefore the period of oscillation. Q9 buffers the voltage on C11 and supplies it to a comparator, Z3B and Z3A. Pin 2 of Z3A is fixed at about +7.5 volts. When the voltage on pin 4 of Z3B decreases to below +7.5 volts, Z3A turns on Q11 which supplies +15 volts to the gate of Q8. Q8 then charges capacitor C11 back to +15 volts to start the cycle over again.

R63. C10 and R59 supply current to Q7 as the frequency of the oscillator is increased to prevent the oscillator from going flat due to the recovery time of the circuit. Q12 is a phase splitter which takes the sawtooth from pin 3 of Z3 and supplies it to the oscillator output and the pulse converter. The waveform on the emitter of Q12 is 7.5VPP negative going (+7.5 volts offset), and the collecter is about 5VPP positive going (zero referenced).

Sawtooth To Pulse Converter: Z3C and Z3D is a

comparator with R86 and R87 setting the switch point at +7.5 volts. The sawtooth wave from the oscillator is supplied to the comparator through R75 and C12. Z3E supplies an offset current to raise or lower the DC level of the sawtooth wave to change the point at which the comparator switches. When the pulse width sliders on the front panel are at minimum, the comparator will switch exactly in the middle of the sawtooth slope, producing a square wave (50% duty cycle). The output of the comparator (Z3, pin 8) is processed through Z4A which inverts the shapes of the pulse output.



2.5.4 Ring Modulator

The ring modulator utilizes two CMOS nand gates (Z4B and Z4C) and Q20 in an 'exclusive or' function. Square waves from VCO 1 and VCO 2 are supplied to pin 5 and pin 8 of Z4 and the output is taken from the emitter of Q20.

CIRCUIT DESCRIPTIONS (Board C-II)

2.6.1 Voltage Controlled Filter (VCF)

Audio signals from both VCOs, the ring modulator, and the noise generator are applied to the audio input of the voltage controlled filter (pin 1, M1) through C1 and C13. Control voltages from S/H, LFO, KYBD CV, and the envelope generators (ADSR and AR) are summed and inverted by Z1. The control input of the VCF accepts negative going control voltages; as the voltage on TP-1 is decreased, the filter cutoff increases. Signals on the output of the VCF (pin 10) are fed back to the resonance input (pin 2) via the resonance slider (R73).

2.6.2 Voltage Controlled Amplifier (VCA)

Audio signals from the VCF are processed by the high pass filter (C3, R13 and R74) and connected to the noninverting input of Z2. Z2 is an operational transconductance amplifier (OTA) whose gain is a function of the current supplied to pin 5. Control voltages from the two envelope generators and the VCA gain slider are connected to Q1 which supplies current to the OTA. R70, the control reject trimmer, balances the inputs of the OTA to minimize the effect of control voltages on the audio output of the VCA.

2.6.3 AR Envelope Generator

The Attack-Release envelope generator produces a control voltage with variable rise and fall times. It is used to control the VCF or the VCA. When a gate voltage is supplied by the keyboard or the LFO through S10, Q4 turns on. which charges capacitor C7 through R76, R32 and CR5. The position of R76 (attack slider) determines the time C7 takes to charge up. When the gate voltage is removed, Q4 turns off which allows Q5 to turn on. The voltage on C7 then discharges through CR6, R77, R31, and Q5. R77 (release slider) sets the release time. Q6 and Q7 buffer the voltage on C7 and supply it to the VCA and VCF.

2.6.4 ADSR Envelope Generator

The Attack-Decay-Sustain-Release envelope generator produces a control voltage with variable rise and fall times. It is used to control the VCF or the VCA. A gate and trigger signal must be supplied from the keyboard or LFO to start the ADSR voltage rising.

Attack: When a gate signal (+10 volts) is supplied through S8, Q8, Q9 and Q10 turns on which then allows Q16 to turn off. With Q16 off, a trigger applied through C9 and R55 will momentarily turn on Q18 and Q17. Q17 then supplies +15 volts through CR18, CR19, CR17 and R57 to hold Q18 on. Q18 and Q17 (the attack latch) now supplies +15 volts through the attack slider (R85), R43, and CR9 and charges up the integrating capacitor, C8.

Q12, Q13 and Q14 buffer the voltage on C8 and provides it to the VCA and VCF. Q15 is the peak detector which monitors the output of the ADSR. When the ADSR voltage reaches its maximum, (about +10 volts), Q15 will turn on and provide this voltage to the base of Q16 through CR15. Q16 then grounds out the voltage on the base of Q18 to unlatch Q18 and Q17 and end the attack portion of the ADSR cycle.

Decay & Sustain: When the attack portion of the ADSR cycle has completed, the voltage on C8 is allowed to discharge through CR11, R47 and the decay slider (R86) to the emitter of Q11. The sustain

slider (R87) sets the voltage level on the base of Q11. When the voltage level on the emitter of Q11 falls below the level on the base, Q11 turns off and prevents the voltage on Q8 from discharging further.

Release: When the gate is removed, the remaining voltage on C8 is discharged to ground through CR10, R44 and the release slider (R88).

CIRCUIT DESCRIPTIONS (Power Supply)

-15 Volt Supply: The -15 volt supply derives its regulation from the +15 volt supply through R8. When the output of the -15 volt supply is at the correct voltage, the junction of R8 and R12 is zero volts. The base of Q2 is referenced to zero volts through R9. Should the output of the minus supply increase, the voltage on the base of Q3 will also increase which begins to turn off Q3. Q2 conducts more current which requires Q4 to conduct more. Q4 drives the pass transistor (Q5) which then conducts more current thereby lowering the output to -15 volts.

+15 Volt Supply: Z1 contains a voltage reference which supplies +7.4 volts to pin 6 of Z1. This voltage is connected through pin 5 to the noninverting input of an op amp. The output of the op amp is connected to an emitter follower, also located in Z1, which controls the pass transistor (Q1). Should the output of the power supply change, the voltage at the junction of R3 and R6 will supply the inverting input of the op amp in Z1 with the voltage difference. The op amp will then supply a correction voltage to the emitter follower and pass transistor and bring the power supply's voltage to normal.

Short circuit protection: R2 and the transistor in Z1 connects to pins 2 and 3 limit the +15 supply's current to a maximum of 180 milliamps. Q6 and R16 limit the -15 supply's current to a maximum of 150 milliamps.

NOTE: Although the circuit description above is for the Power Supply - II Board, the information applies to the the Power Supply - I Board as well. The schematics and reference numbers for the two supplies are different, but the circuits are the same.

SECTION 3 TRIM PROCEDURES *NOTE: The following procedures must be performed in the order presented.*

3.1 Power Supply-I Trim Procedure *NOTE: Always execute Power Supply trims first.*

REF.	TRIMMER	TRIM PROCEDURE
T2	+15 VOLT SET	1. Monitor the power supply's +15 volt output with a digital voltmeter. 2. Adjust T2 for exactly +15.00 volts.
T1	-15 VOLT SET	1. Set T2 (+15 volts) first. 2. Put the digital voltmeter's ground lead on the power supply's -15 volt output and put the meter's plus lead on the power supply's ground output. 3. Adjust T1 for exactly +15.00 volts (reversed polarity).

3.2 Board A-I Trim Procedures

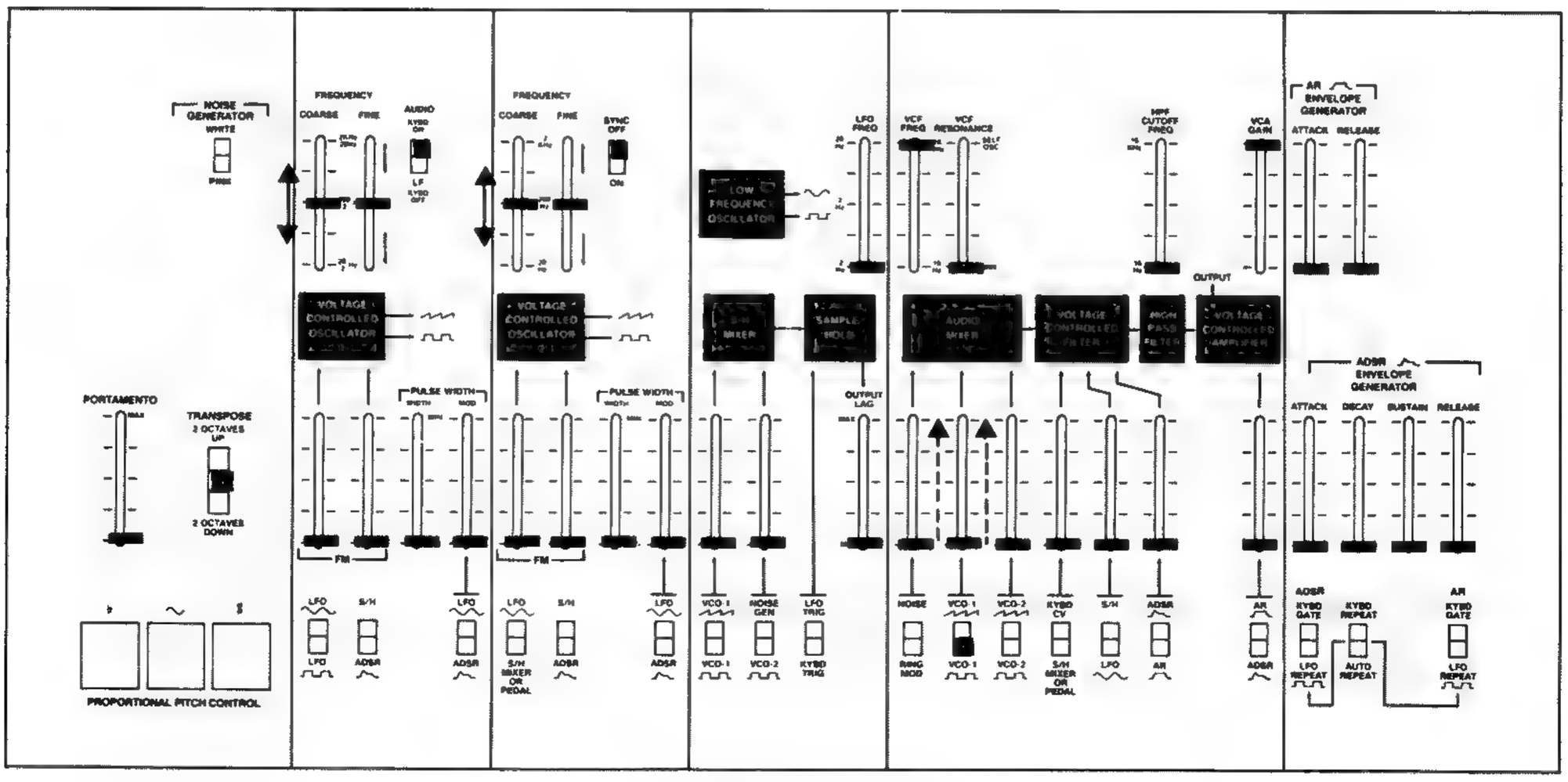
T1	V/OCT	1. Monitor pin 8 on Board A (CV-1 on the interconnecting board) with a digital volt meter. 2. Put the TRANSPOSE switch in the DOWN 2 OCTAVES position. 3. Pin low 'C' on the keyboard. 4. Measure the voltage on pin 8 (CV-1). 5. Pin high 'C' on the keyboard. 6. Adjust the V/OCT trimmer on Board A (T1) for exactly 3 volts higher than the voltage measured in step 4.
T3	NORM	7. Pin low 'C' on the keyboard. 8. Put the TRANSPOSE switch in the NORMAL position. 9. Adjust the NORM trimmer (T3) for exactly 2 volts higher than step 4.
T4	UP 2 OCT	10. Put the TRANSPOSE trimmer in the UP 2 OCTAVES position. 11. Adjust the UP 2 OCT trimmer on Board A (T4) for exactly 4 volts higher than step 4.
T2	2ND VOICE	12. Put the TRANSPOSE switch in the NORMAL position. 13. Monitor pin 6 on Board A (CV-2 on the interconnection board) and measure the exact voltage with a DVM (should be about 15 millivolts). 14. Put the TRANSPOSE switch in the UP 2 OCTAVES position. 15. Adjust the 2ND VOICE trimmer on Board A (T2) for exactly the same voltage as measured in step 13.

3.3 Board B-I (& B-II) Trim Procedures *NOTE: The reference numbers for the B-II boards are in parenthesis.*

T2 & T5 (R141, R80)	VCO 1 & 2 50% PULSE WIDTH	1. Put the TRANSPOSE switch in the normal position. 2. Depress a key in the middle of the keyboard. 3. Monitor TP-5 (square wave output) with an oscilloscope. 4. Adjust the VCO 1 (or VCO 2) COARSE FREQUENCY slider to display exactly one complete cycle. 5. Adjust the 50% PULSE WIDTH trimmer until the duty cycle of the waveform is exactly 50% (exactly square).
T3 & T6 (R118, R42)	VCO 1 & 2 CALIBRATE	1. Monitor TP-5 in VCO 1 (or VCO 2) with either an oscilloscope or a frequency counter. 2. Put the VCO 1 (or VCO 2) COARSE FREQUENCY slider DOWN fully. 3. Put the VCO 1 (or VCO 2) FINE TUNE slider exactly in the MIDDLE. 4. Pin low 'C' on the keyboard (transpose switch midposition). 5. Adjust the VCO CAL trimmer for a 50 msec. period, or 20 Hz.

Board B-I & B-II Trim Procedures (Continued)

REF.	TRIMMER	TRIM PROCEDURE
T1, T4 T7 (R104, R44, R56)	VCO V/OCT	1. Set the following sliders on the front panel at maximum: VCO 1 (square wave) to AUDIO MIXER, VCF FREQUENCY, VCA GAIN. 2. Put all other sliders on the front panel down. 3. Put the TRANSPOSE and PITCH BEND controls in the NORMAL position. 4. Put the VCO 1 range slide switch in the KYBD ON position. 5. Put the VCO 2 SYNC switch in the OFF position. 6. Monitor the HIGH OUTPUT of the Odyssey with a frequency counter or strobe tuner. 7. Pin low 'C' on the keyboard. 8. Adjust VCO 1 COARSE FREQUENCY slider for exactly 100 Hz (or 'C' on the strobe tuner). 9. Pin high 'C' on the keyboard. 10. Using the VCO 1 V/OCT trimmer on Board B, adjust the frequency of VCO 1 to exactly 800 Hz (or 'C' three octaves higher on a strobe tuner). 11. Repeat steps 7 through 10 until the frequency of VCO 1 is correct on low 'C' and high 'C'. 12. Pin low 'C' on the keyboard. 13. Raise the VCO 2 (square wave) slider to the AUDIO MIXER. 14. Adjust the VCO 2 COARSE and FINE TUNE sliders until VCO 2 is exactly in tune with VCO 1. 15. Pin high 'C' on the keyboard. 16. Using the VCO 2 V/OCT trimmer on Board B, adjust the frequency of VCO 2 until it is exactly the same as VCO 1. 17. Repeat steps 12 through 16 until the frequency of VCO 2 is the same as VCO 1 on low 'C' and high 'C'. 19. Pin high 'C' on the keyboard. 20. Depress and release low 'C' (while high 'C' is pinned). 21. Adjust the VCO 2ND VOICE V/OCT trimmer on Board B until the pitch of oscillator does not change in step 20. *THE FOLLOWING ADJUSTMENT IS FOR THE MODEL 2800 ONLY.* 22. Pin low 'C' on the keyboard. 23. Raise the VCO 1 (square wave) slider in the AUDIO MIXER. 24. Adjust VCO 1 & 2 FINE TUNE sliders so that VCO 1 & 2 are in unison. 25. Set the TRANSPOSE switch to the UP 2 OCTAVES position. 26. If the two oscillators are not exactly in tune with each other, adjust the 2nd VOICE TRIMMER on BOARD A until the two oscillators are zero beating.



TUNING SET-UP

3.4 Board C-I Trim Procedures

REF.	TRIMMER	TRIM PROCEDURE
T4	VCF BAL	1. Put the VCF RESONANCE slider at MAXIMUM. 2. Monitor pin 10 of the 4023 module with an oscilloscope. 3. Put all other sliders on the front panel DOWN. 4. Adjust the VCF FREQUENCY slider for a sine wave of about 1000 Hz. 5. Measure the peak to peak amplitude of the sine wave on pin 10. 6. Measure the peak to peak amplitude of the sine wave on pin 9 of the 4023 (should be about half the amplitude of pin 10). 7. Adjust the BAL trimmer on Board C until the sine wave on pin 9 is exactly half the amplitude of the sine wave on pin 20.
T3	VCF CUTOFF	1. Put the VCF RESONANCE slider at MAXIMUM. 2. Put all other sliders on the front panel DOWN. 3. Monitor pin 10 of the 4023 module with an oscilloscope or frequency counter. 4. Adjust the VCF CUTOFF trimmer for a 62.5 msec. period, or, 16 Hz.
T5	VCF V/OCT	1. Put the following sliders at MAXIMUM: VCF RESONANCE, VCA GAIN, and VCF KYBD CV. 2. Put all other sliders on the front panel DOWN. 3. Pin low 'C' on the keyboard. 4. Monitor the HIGH OUTPUT of the Odyssey with a frequency counter. 5. Adjust the VCF FREQUENCY slider for 100 Hz. 6. Pin high 'C' on the keyboard. 7. Adjust the VCF V/OCT trimmer on Board C for 800 Hz. 8. Repeat steps 3 through 7 until the frequency of the VCF is correct on low 'C' and high 'C'.
T1	VCA GAIN	1. Put the following sliders at MAXIMUM: VCO 2 'SQUARE WAVE' to the AUDIO MIXER, VCF FREQUENCY , and VCA GAIN. 2. Put all other sliders on the front panel DOWN. 3. Measure the peak to peak amplitude of the waveform on pin 10 of the 4023 module with an oscilloscope. 4. Monitor the HIGH OUTPUT of the Odyssey with an oscilloscope. 5. Adjust the VCA GAIN trimmer on Board C so that the amplitude of the waveform on the output of the Odyssey is that same as the amplitude measured in step 3.
T2	VCA CVR	1. Put the following sliders at MAXIMUM: VCA 'ADSR', and LFO FREQUENCY. 2. Put the ADSR 'DECAY' slider at ONE-FOURTH. 3. Put all other sliders on the front panel DOWN. 4. Put the three slide switches under the ADSR sliders DOWN. 5. Monitor the HIGH OUTPUT of the Odyssey with an oscilloscope (set to about .5 volts per division). 6. Adjust the VCA CVR trimmer on Board C for the minimum amplitude signal on the output of the Odyssey.

3.5 Power Supply-II Trim Procedures

REF.	TRIMMER	TRIM PROCEDURE
R5	+15 VOLT SET	1. Monitor the power supply's +15 volt output with a digital voltmeter. 2. Adjust R5 for exactly +15.00 volts.
R11	-15 VOLT SET	1. Set R5 (+15 volts) first. 2. Put the digital voltmeter's ground lead on the power supply's -15 volt output and put the meter's plus lead on the power supply's ground output. 3. Adjust R11 for exactly +15.00 volts (reversed polarity).

THE FOLLOWING PROCEDURE RECALIBRATES THE +15 VOLT SUPPLY SO THAT THE CV OUTPUT JACK WILL PROVIDE EXACTLY 1 V/OCT. THIS TRIM PROCEDURE MUST BE PERFORMED WHEN THE ODYSSEY IS TO BE USED AS A 'MASTER' SYNTHESIZER.

R5	+3V CV SET	1. Connect a digital voltmeter to the CV OUTPUT jack on the rear of the Odyssey. 2. Pin low 'C' on the keyboard (transpose and pitch bend normal). 3. Measure the exact voltage on the CV output (millivolt range). 4. Pin high 'C' on the keyboard. 5. Re-adjust the +15 volt trimmer (R5) for EXACTLY +3.00 volts higher than the voltage measured in step 3. 6. Perform the A-II trim procedure and the B-II (or B-I) trim procedure.

3.6 Board A-II Trim Procedures

R23	TRANSPOSE	1. Perform the PWR SUP-II trim procedure. 2. Perform the V/OCT section of the Board B-I (or B-II) trim procedure. 3. Put the following sliders at MAXIMUM: VCO 1 (square wave) to the AUDIO MIXER, VCF FREQUENCY, and VCA GAIN. 4. Put all other sliders on the front panel DOWN. 5. Put the TRANSPOSE switch in the NORMAL position. 6. Pin low 'C' on the keyboard. 7. Connect a frequency counter or strobe tuner to the HIGH OUTPUT of the Odyssey. 8. Adjust the VCO 1 COARSE FREQUENCY and FINE TUNE sliders to 100 Hz or ('C' on a strobe tuner). 9. Put the TRANSPOSE switch in the UP 2 OCT position. 10. Adjust the TRANSPOSE trimmer (R23) for exactly 400 Hz (or 'C' two octaves higher than step 8).

NOTE: Disregard the following adjustment for circuits containing PPC.

R26	PITCH BEND	1. Perform the PWR SUP-II trim procedure. 2. Perform the V/OCT section of the Board B-I (or B-II) trim procedure. 3. Put the following sliders at MAXIMUM: VCO 1 (square wave) to the AUDIO MIXER, VCF FREQUENCY, and VCA GAIN. 4. Put all other sliders on the front panel DOWN. 5. Put the PITCH BEND control in the CENTER. 6. Pin low 'C' on the keyboard. 7. Connect a frequency counter or strobe tuner to the HIGH OUTPUT of the Odyssey. 8. Adjust the VCO 1 COARSE FREQUENCY and FINE TUNE sliders to 100 Hz (or 'C' on a strobe tuner). 9. Put the PITCH BEND control fully CLOCKWISE. 10. Adjust the PITCH BEND trimmer (R26) for exactly 200 Hz (or 'C' one octave higher than step 8).

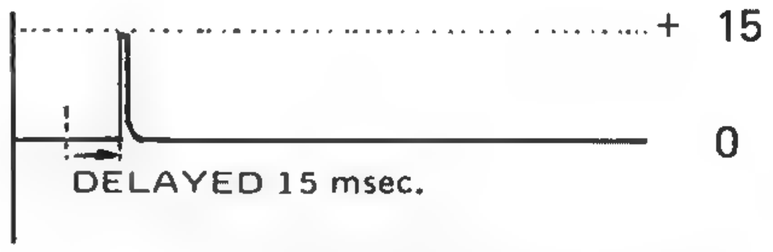
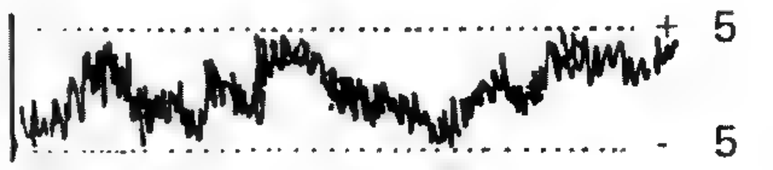
3.7 Board B-II Trim Procedures *(See Section 3.3 on page 14)*

3.8 Board C-II Trim Procedures

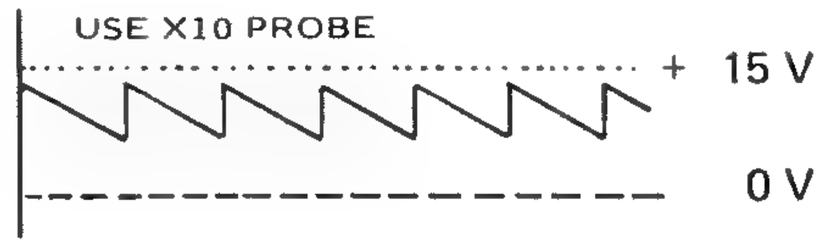
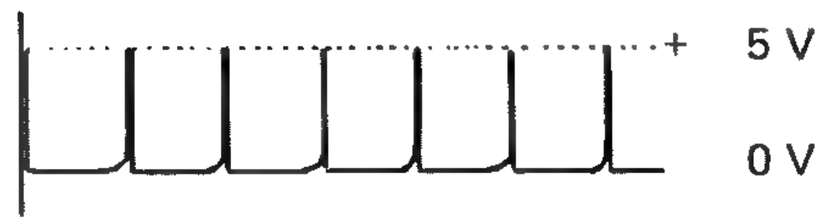
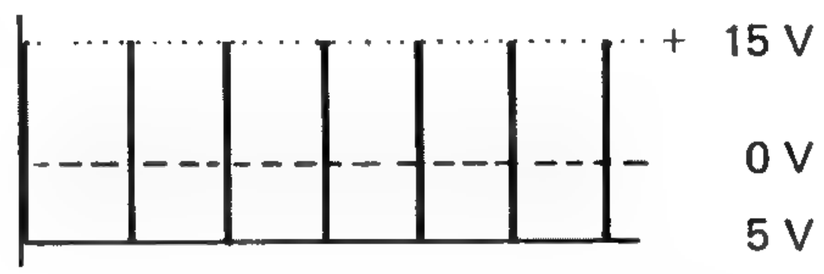
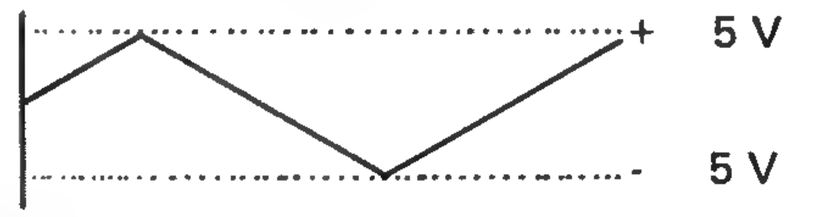
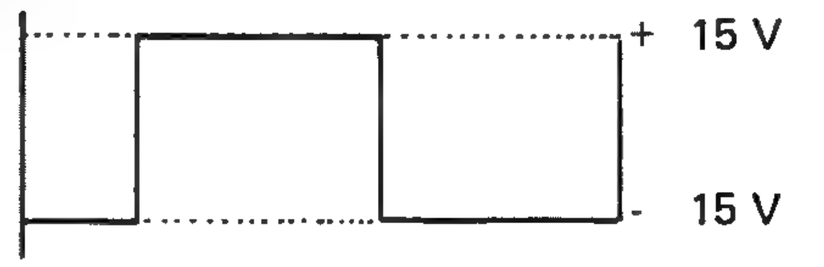
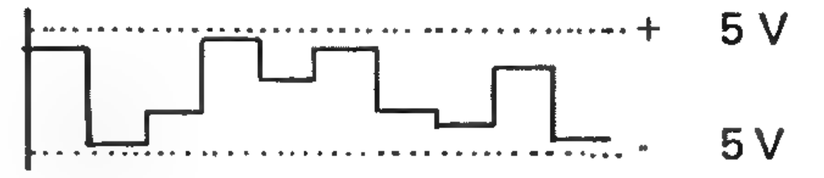
REF.	TRIMMER	TRIM PROCEDURE
R67	VCF BAL	1. Put the following sliders at MAXIMUM: VCA GAIN, and LFO FREQUENCY. 2. Put the ADSR 'DECAY' slider at ONE-FOURTH. 3. Put all other sliders on the front panel DOWN. 4. Put the three slide switches under the ADSR sliders DOWN. 5. Monitor the HIGH OUTPUT of the Odyssey with an oscilloscope (set to about .5 volts per division). 6. Adjust the VCF BAL trimmer on Board C for the minimum amplitude signal on the output of the Odyssey.
R71	VCF CUTOFF	1. Put the VCF RESONANCE slider at MAXIMUM. 2. Put all other sliders on the front panel DOWN. 3. Monitor pin 10 of M1 with an oscilloscope or frequency counter. 4. Adjust the VCF CUTOFF trimmer for a 62.5 msec. period, or, 16 Hz.
R68	VCF V/OCT	1. Put the following sliders at MAXIMUM: VCF RESONANCE, VCA GAIN, and VCF KYBD CV. 2. Put all other sliders on the front panel DOWN. 3. Pin low 'C' on the keyboard. 4. Monitor the HIGH OUTPUT of the Odyssey with a frequency counter. 5. Adjust the VCF FREQUENCY slider for 100 Hz. 6. Pin high 'C' on the keyboard. 7. Adjust the VCF V/OCT trimmer on Board C for 800 Hz. 8. Repeat steps 3 through 7 until the frequency of the VCF is correct on low 'C' and high 'C'.
R69	VCA GAIN	1. Put the following sliders at MAXIMUM: VCO 1 'SQUARE WAVE' to the AUDIO MIXER, VCF FREQUENCY, and VCA GAIN. 2. Put all other sliders on the front panel DOWN. 3. Monitor the HIGH OUTPUT of the Odyssey with an oscilloscope. 4. Adjust the VCA GAIN trimmer on Board C so that the amplitude of the waveform on the output of the Odyssey is 2VPP.
R70	VCA CVR	1. Put the following sliders at MAXIMUM: VCA 'ADSR', and LFO FREQUENCY. 2. Put the ADSR 'DECAY' slider at ONE-FOURTH. 3. Put all other sliders on the front panel DOWN. 4. Put the three slide switches under the ADSR DOWN. 5. Monitor the HIGH OUTPUT of the Odyssey with an oscilloscope (set to about .5 volts per division). 6. Adjust the VCA CVR trimmer on Board C for the minimum amplitude signal on the output of the Odyssey.

SECTION 4 BOARD TEST POINTS

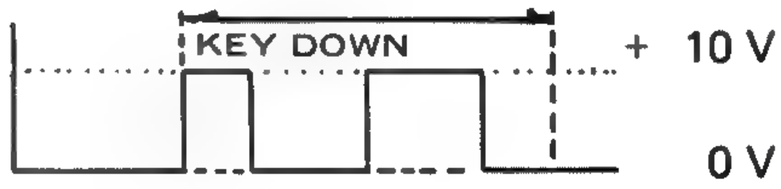
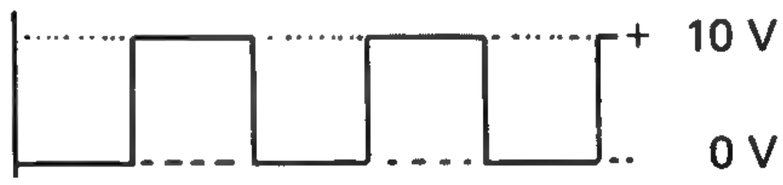
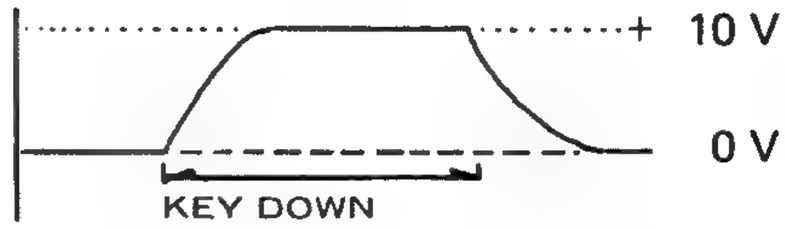
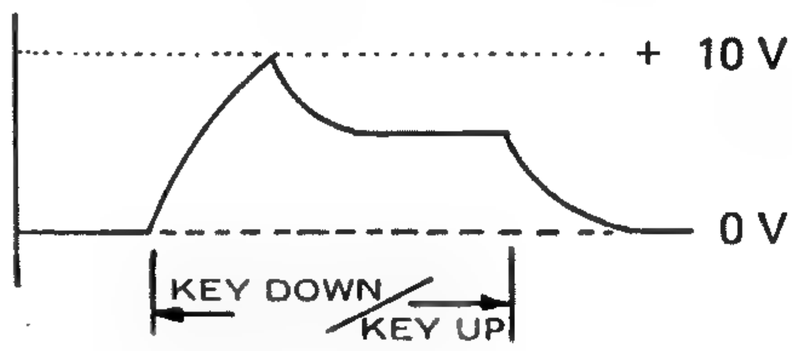
4.1 Board A-I Test Points

TEST POINT	FUNCTION	SET UP	SPECIFICATIONS
TP-1	2ND VOICE CV OUTPUT	1. No keys depressed	0V
		2. High 'C' and low 'C' both depressed.	+3V
TP-2	CURRENT SOURCE	1. Transpose switch: Down 2 octaves (no keys depressed).	+3V
		2. Transpose switch: Normal position.	+5V
		3. Transpose switch: Up 2 octaves.	+7V
TP-3	CV BUFFER	1. Depress and hold low 'C' (transpose switch in the normal position).	+2V
		2. Depress and hold high 'C'.	+5V
TP-4	CV OUTPUT	1. Depress and release low 'C' (transpose switch in the normal position).	+2V *(Should not change more than 20 millivolts in one minute.)*
		2. Depress and release high 'C'.	+5V *(Should not change more than 20 millivolts in one minute.)*
TP-5	GATE OUTPUT	1. No keys depressed.	0V
		2. Depress any key.	+12V
TP-6	GATE BUS	1. No keys depressed.	-13V
		2. Depress any key.	+13V
TP-7	TRIGGER BUS	1. Depress any key.	
TP-8	TRIGGER OUTPUT	1. Depress any key.	
TP-9	WHITE NOISE OUTPUT		
TP-10	PINK NOISE OUTPUT		

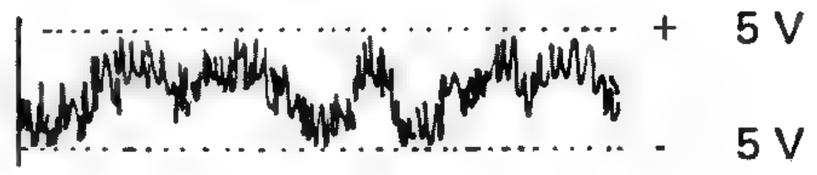
4.2 Board B-I Test Points

TEST POINT	FUNCTION	SET UP	SPECIFICATIONS
TP-1	SAWTOOTH (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-2	RESET PULSE (VCO 1 & 2)	1. Initial frequency sliders midposition 2. All other sliders down.	
TP-3	Q6, RESET PULSE (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-4	SAWTOOTH WAVE (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-5	SQUARE WAVE OUTPUT (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-6	SAWTOOTH OUTPUT (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-7	LFO TRIANGLE OUTPUT	1. LFO frequency slider up.	
TP-8	LFO SQUARE WAVE OUTPUT	1. LFO frequency slider up.	
TP-9	S/H OUTPUT	1. S/H mixer slider 'noise' up. 2. LFO trigger mode: LFO 3. LFO Frequency slider up.	

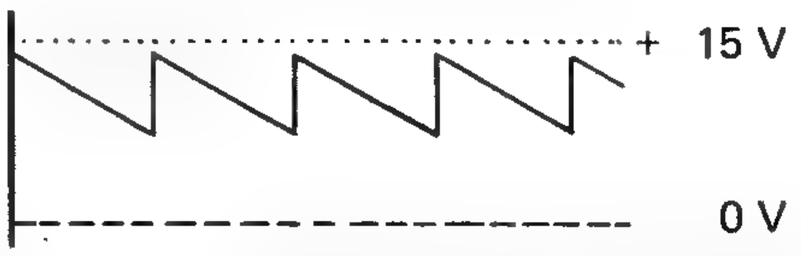
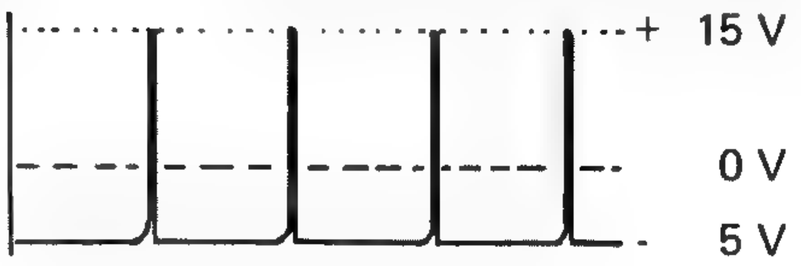
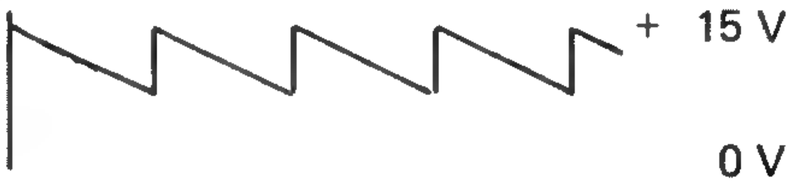
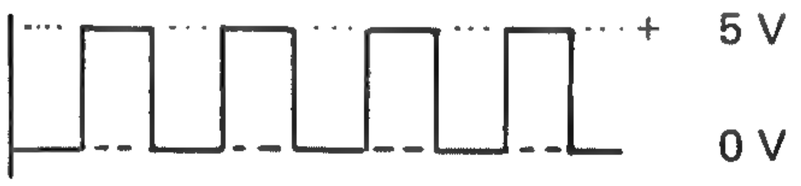
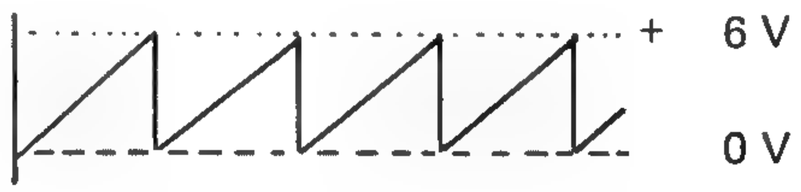
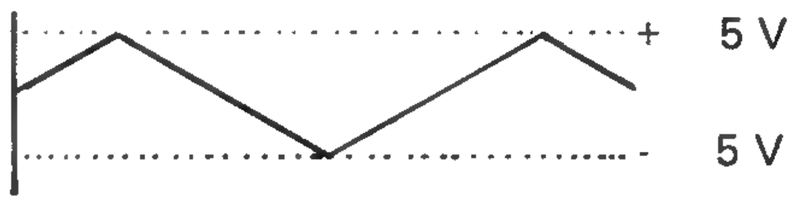
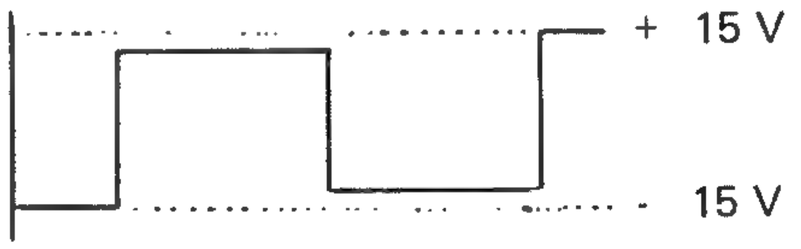
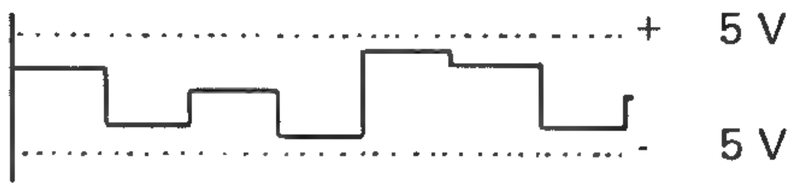
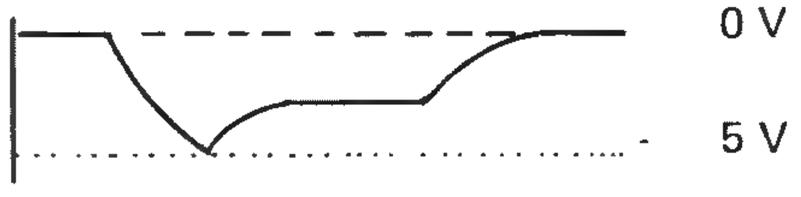
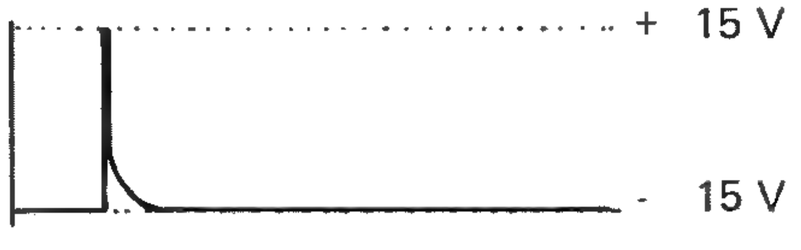
4.3 Board C-I Test Points

TEST POINT	FUNCTION	SET UP	SPECIFICATIONS
TP-1	CV INVERTER	1. VCF 'CV' slider up. 2. All other sliders down. 3. Pin low 'C' on the keyboard. (Transpose switch in the normal position.)	-2V
		4. Pin high 'C' on the keyboard.	-5V
TP-2	VCF OUTPUT	1. Raise the VCF 'VCO 1 Sawtooth' slider. 2. Raise the initial filter frequency slider. 3. Put all other sliders down.	
TP-3	VCA OUTPUT	1. Raise the VCF 'VCO 1 Sawtooth' slider. 2. Raise the initial filter frequency slider. 3. Raise the VCA gain slider. 4. Put all other sliders down.	
TP-4	GATE BUFFER	1. All repeat slide switches under the ADSR UP. 2. Depress and release a key.	
		3. Repeat switch: AUTO position (down).	
TP-5	AR OUTPUT	1. AR attack slider: ½ 2. AR release slider:½ 3. Depress and release a key (all repeat switches up).	
TP-6	ADSR OUTPUT	1. ADSR attack slider: ½ 2. ADSR decay slider: ½ 3. ADSR sustain slider: ½ 4. ADSR release slider:½ 5. Depress and release a key (all repeat switches up).	

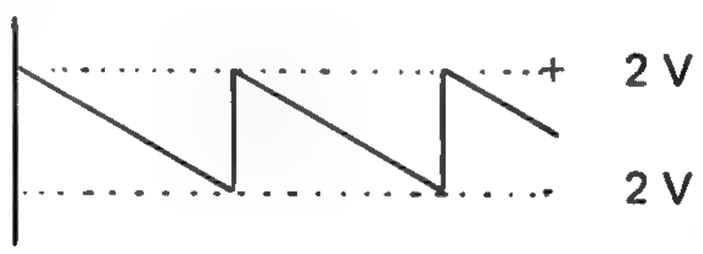
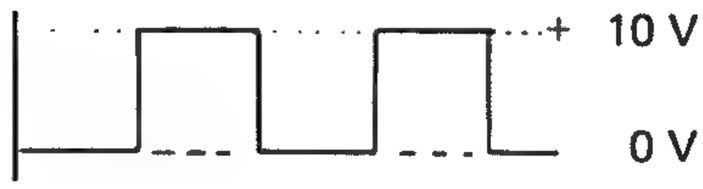
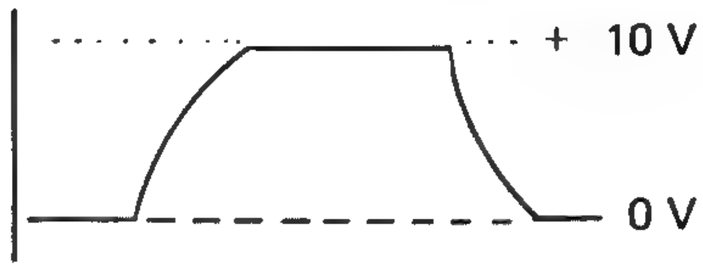
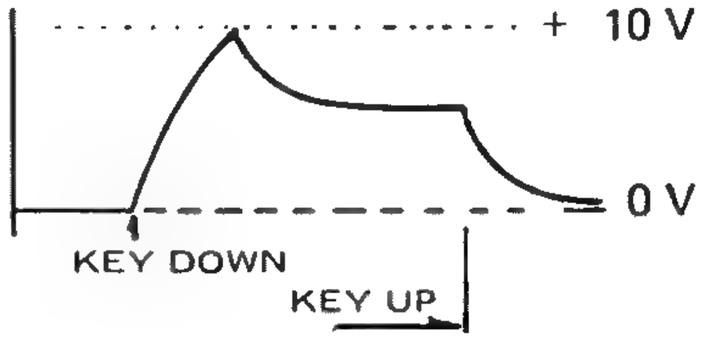
4.4 Board A-II Test Points

TEST POINT	FUNCTION	SET UP	SPECIFICATIONS
TP-1	CURRENT SOURCE & 2ND VOICE CV GENERATOR	1. No keys depressed.	0V
		2. Both low 'C' and high 'C' held.	+3V
TP-2	CV BUFFER	1. Depress and hold low 'C'.	+3V
		2. Depress and hold high 'C'.	0V
TP-3	CV MEMORY	1. Depress and release low 'C'.	+3V *(Should not change more than 20 millivolts in one minute.)*
		2. Depress and release high 'C'.	0V *(should not change more than 20 millivolts in one minute.)*
TP-4	CV OUTPUT	1. Transpose and Pitch Bend: Normal 2. Depress and release low 'C'.	0V
		3. Depress and release high 'C'.	+3V
TP-5	GATE BUS	1. All keys up.	+15V
		2. Depress any key.	+10V
TP-6	MEMORY GATE	1. All keys up.	-13V
		2. Depress any key.	+15V
TP-7	GATE OUT	1. All keys up.	0V
		2. Depress any key.	+12V
TP-8	TRIGGER OUT	1. Depress any key.	
TP-9	WHITE NOISE	1. Put NOISE switch in the WHITE position.	
TP-10	PINK NOISE	1. Put NOISE switch in PINK position.	

4.5 Board B-II Test Points

TEST POINT	FUNCTION	SET UP	SPECIFICATION
TP-1	SAWTOOTH (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-2	SAWTOOTH (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-3	RESET PULSE (VCO 1 & 2)	1. Initial frequency sliders midposition.	
TP-4	SAWTOOTH TO PULSE (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-5	SQUARE WAVE OUTPUT (VCO 1 & 2)	1. Initial frequency sliders midposition.	
TP-6	SAWTOOTH OUTPUT (VCO 1 & 2)	1. Initial frequency sliders midposition. 2. All other sliders down.	
TP-7	LFO TRIANGLE OUTPUT	1. LFO frequency slider up.	
TP-8	LFO SQUARE WAVE OUTPUT	1. LFO frequency slider up.	
TP-9	S/H OUTPUT	1. S/H 'noise' slider up. 2. LFO/KYBD slider switch up (LFO) 3. LFO frequency slider up.	
TP-10	ADSR INVERTER	1. Put all ADSR sliders at ½. 2. Depress any key (repeat switches all up).	
TP-11	TRIGGER PROCESSOR	1. Depress any key.	

4.6 Board C-II Test Points

TEST POINT	FUNCTION	SET UP	SPECIFICATIONS
TP-1	CV INVERTER	1. VCF 'CV' slider up. 2. All other sliders down. 3. Pin low 'C' on the keyboard (transpose switch in the normal position).	0V
		4. Pin high 'C' on the keyboard	-3V
TP-2	VCF OUTPUT	1. Raise the VCF 'VCO 1 Sawtooth' slider. 2. Raise the initial filter frequency slider. 3. Put all other sliders down.	
TP-3	VCA OUTPUT	1. Raise the VCF 'VCO 1 Sawtooth' slider. 2. Raise the initial filter frequency slider. 3. Raise the VCA gain slider. 4. Put all other sliders down.	
TP-4	GATE BUFFER	1. All repeat slide switches under the ADSR UP. 2. Depress and release a key.	
		3. Repeat switch: AUTO position (down).	
TP-5	AR OUTPUT	1. AR attack slider: ½ 2. AR release slider: ½ 3. Depress and release a key (all repeat switches up).	
TP-6	ADSR OUTPUT	1. ADSR attack slider: ½ 2. ADSR decay slider: ½ 3. ADSR sustain slider:½ 4. ADSR release slider: ½ 5. Depress and release a key (all repeat switches up).	

J1-3 +15V
C4 1μF
J1-2 COM
C5 1μF
J1-1 -15V

J2-1 Trigger Bus
R1 10K
Q1 2N 6076
R2 27K
C1 100 PF
R4 1K
R7 10K
R11 2.7K
R3 4.7K
R5 5.6K
R6 56K
C2 .47
Q2 2N 5172
R8 100K
R9 10K
C3 .01
Q3 2N 5172
R10 10K
Q4 2N 6076
R12 1K
4 Trigger Out

P1 10K LIN CW
R13 3.3K
R14 1.2K
CR4
CR5
R15 1K
9 Pitch Bend

J3-1
J3-2 } Portamento
J3-3

R16 5.36K 1%
T1 1K CW
CR1
R17 6.98K 1%
R18 6.98K 1%
Q5 2N 6076

J2-5 Keyboard High
Keyboard Bus PAD NEAR Q6
P2 Portamento 1M AUD
Q7 LS4392
R22 1M
CR3
Q6 IMF 3958
A1a ½LM1458
C6 .047
R19 100K
R20 100K
R21 1K
C7 .05
R23 100K
CR2
Q8 IMF 3958
A1b ½LM1458
R24 100K
R25 100K
R26 1K
8 Keyboard C.V.
C8 0.47

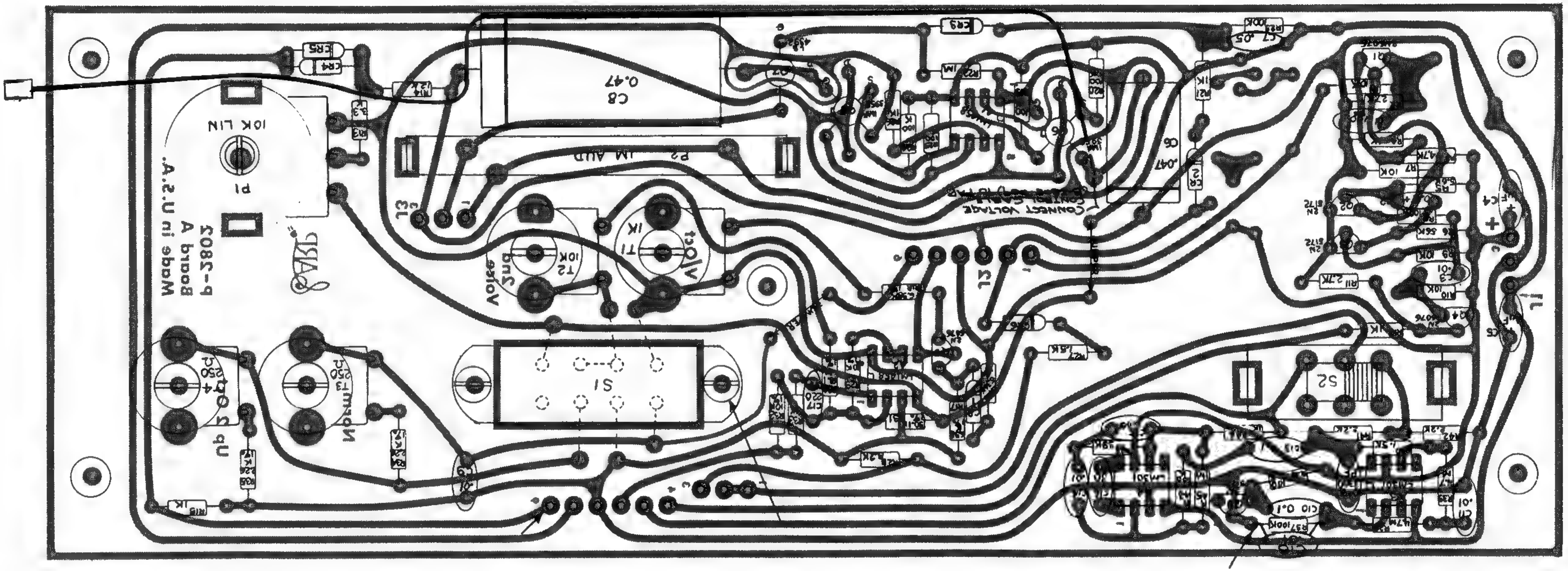
J2-2 Gate Bus
CR6
R27 1.5K
R28 8.2K
3 Gate Out

R32 10K 1%
C17 220 PF
A2a ½LM1458
R29 10K 1%
R30 68.1K 1%
R31 30.1K 1%
A2b ½LM1458
R33 1K
6 Aux Out (2nd Voice)

R36 100K
C10 0.1
R38 4.7M
R39 4.7M
C11 .01
Q9 2N 5172
R37 100K
A3 LM301
R40 1.5K
C12 .0033
R41 2.2K
R42 2.2K
C13 0.1
R43 100K
C15 .001
R44 39K
C14 .01
R45 1M
C16 30 PF
A4 LM301
R46 1K
5 Noise B
1-2 Noise A
S2

TRANSPOSE SWITCH S1
UP 2 OCT
NORM
DOWN 2 OCT
T3 250Ω
R34 2.26K 1%
T4 250Ω
R35 2.21K 1%
J2-6 Keyboard Low
C9 .01

ARP ODYSSEY Model 2800
SCHEMATIC Board A-1



ARP ODYSSEY Model 2800
ASSEMBLY Board A-1

TRANSPOSE CIRCUIT
TRANSPOSE SWITCH
UP 2 OCTAVES
NORMAL
DOWN 2 OCTAVES
S1
TRANSPOSE TRIM
R23 10K LIN
R22 68.1K 1%
J2-3 GND
J2-4
P.P.C. CIRCUIT
P.P.C. BOARD 72.17501
TO BOARD 81
R16 10K 1%
R14 49.9K 1%
R15 3.3K
SUMMING CIRCUIT
J4-3 CV OUT
J4-2 CV IN
KEYBOARD CONTROL VOLTAGE
9 PITCH BEND (FORMER)
7 GND
PITCH BEND CIRCUIT
J5-1 LED GROUND
J5-3 LED POWER
R51 680Ω ½W 10%
J4-5 GATE IN
CR8
J4-4 GATE OUT
5 GATE OUT
KEYBOARD CONTROL VOLTAGE MEMORY
J3-2 PORTAMENTO
J3-1
J2-2 KEYBOARD CONTROL VOLTAGE BUSS
J3-3 GND
R18 1K
C7 0.05 20%
CR5
PORTAMENTO R30 1M
Q3 2N4392
C8 0.47 10%
R24 10K 1%
Q4 IMF395B
R31 100K
R32 100K
R36 1M
CR6
R38 100K
J1-3 +15V
J1-2 GND
J1-1 -15V
C11 1MF 35V
C12 1MF 35V
J2-1 KEYBOARD GATE
R1 1K
R2 10K
Q1 2N6076
CR2
R9 2.2K
R10 10K
GATE GENERATOR
TRIGGER GENERATOR
R3 2.2K
Q2 2N6076
R4 10K
R5 39K
C2 .01 20%
R6 1M
R7 1M
C1 0.1 +80% -20%
CR7
C3 0.001 20%
R8 1M
C20 20% 0.001
R46 100K
R48 100K
Q8 2N6076
R47 39K
R49 1K
R50 100K
4 TRIGGER OUT
J4-1 TRIGGER OUT
R20 100K
C21 0.001 20%
R21 100K
6 AUX OUT 2ND VOICE
J4-6 TRIGGER IN
J2-5 KEYBOARD HIGH
J2-6 KEYBOARD LOW
C5 0.01 20%
R11 15K 1%
R12 390K
R17 28K 1%
R13 6.98K 1%
KEYBOARD CURRENT SOURCE & 2ND VOICE GENERATOR
NOISE GENERATOR
Q5 (SELECTED 2N5172) 56001
C14 0.01 20%
C15 22 16V
R39 100K
C16 1MF 35V
Q6 2N6076
C17 1MF 35V
R40 100K
R41 100K
R43 10K
R42 1M
C18 3.3P 10%
R44 1.5K
R45 2.2K
R37 2.2K
C10 0.01 20%
C9 0.001 20%
R33 39K
R34 1M
C6 30P 20%
R35 100K
C13 0.1 +80% -20%
C19 0.0033 20%
PINK WHITE S2 UP
5 NOISE B
1
NOISE A
2

ARP ODYSSEY-2
Model 2810 - 2823
SCHEMATIC Board A-II

ARP ODYSSEY-2 Model 2810 - 2823
ASSEMBLY Board A-II
(without PPC)

ARP ODYSSEY-2 Model 2810 - 2823
ASSEMBLY Board A-II
(with PPC)

A1, A2: LM1458
A3: CA3080
T1, T2: CD4011AE
All diodes 1N4149 EXCEPT CR4 IN34
Resistors are ¼W ±5%
Except as noted
Capacitors are in mfd
Except as noted

VCO-1

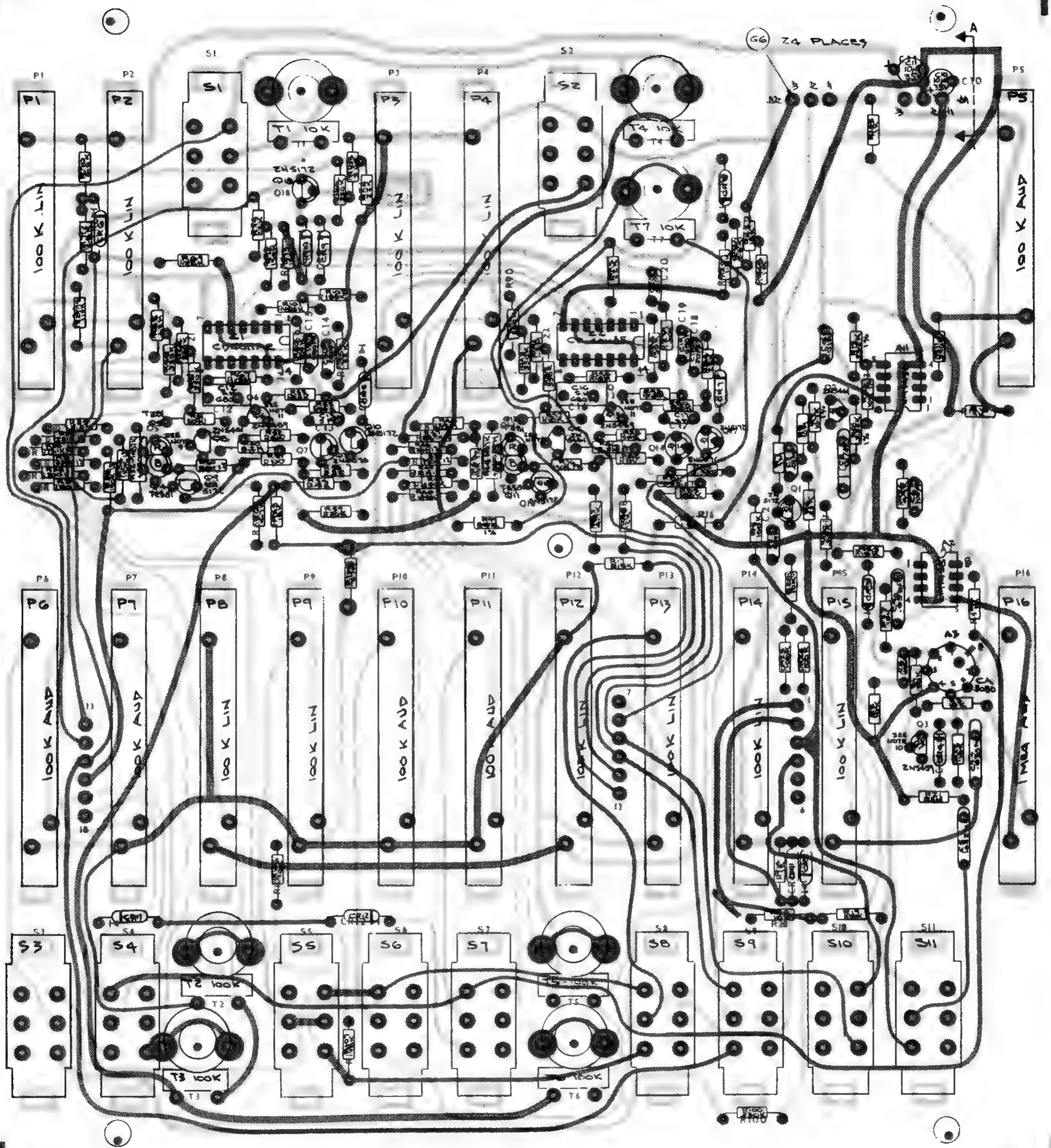
VCO-2

LFO

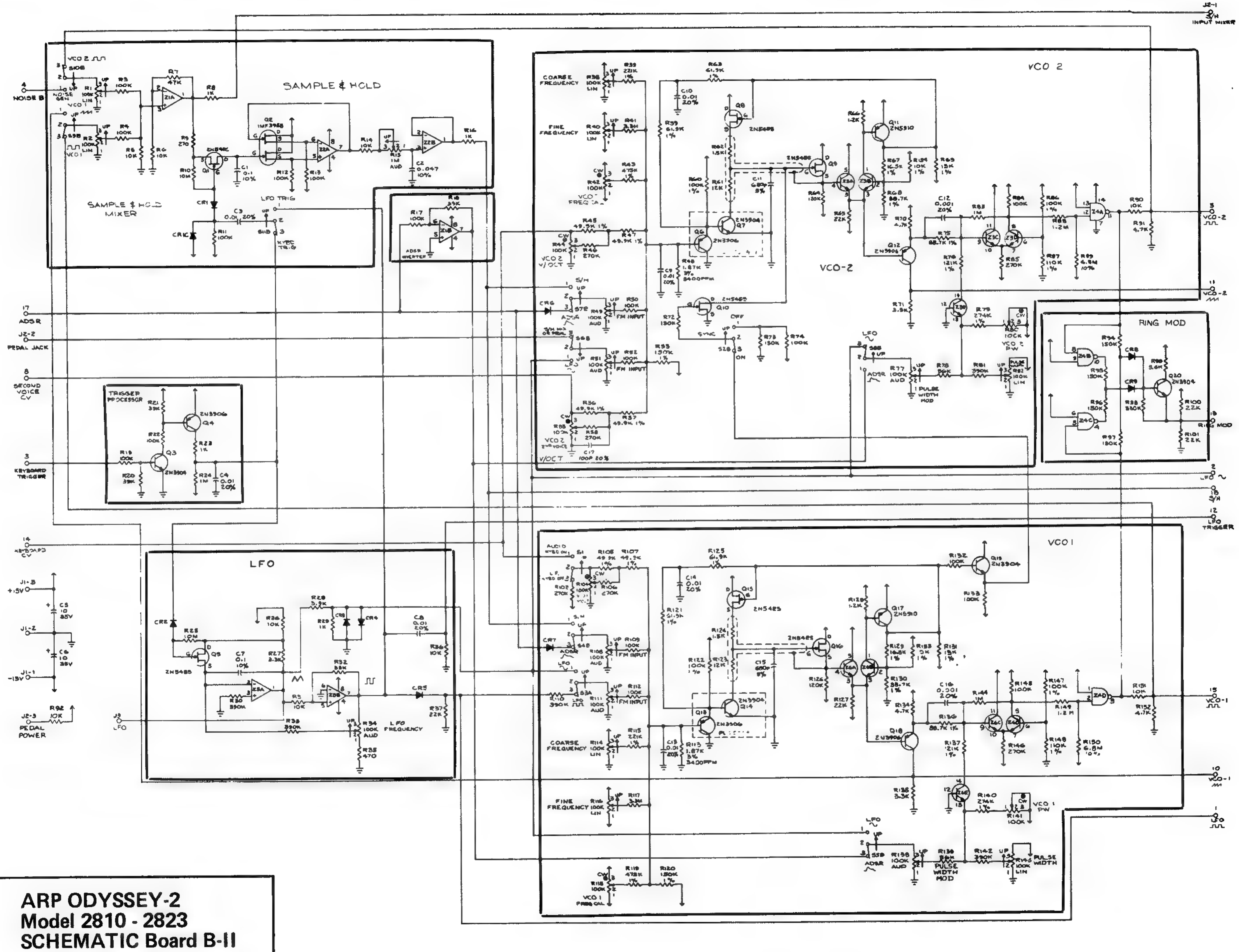
RING MOD

SAMPLE & HOLD

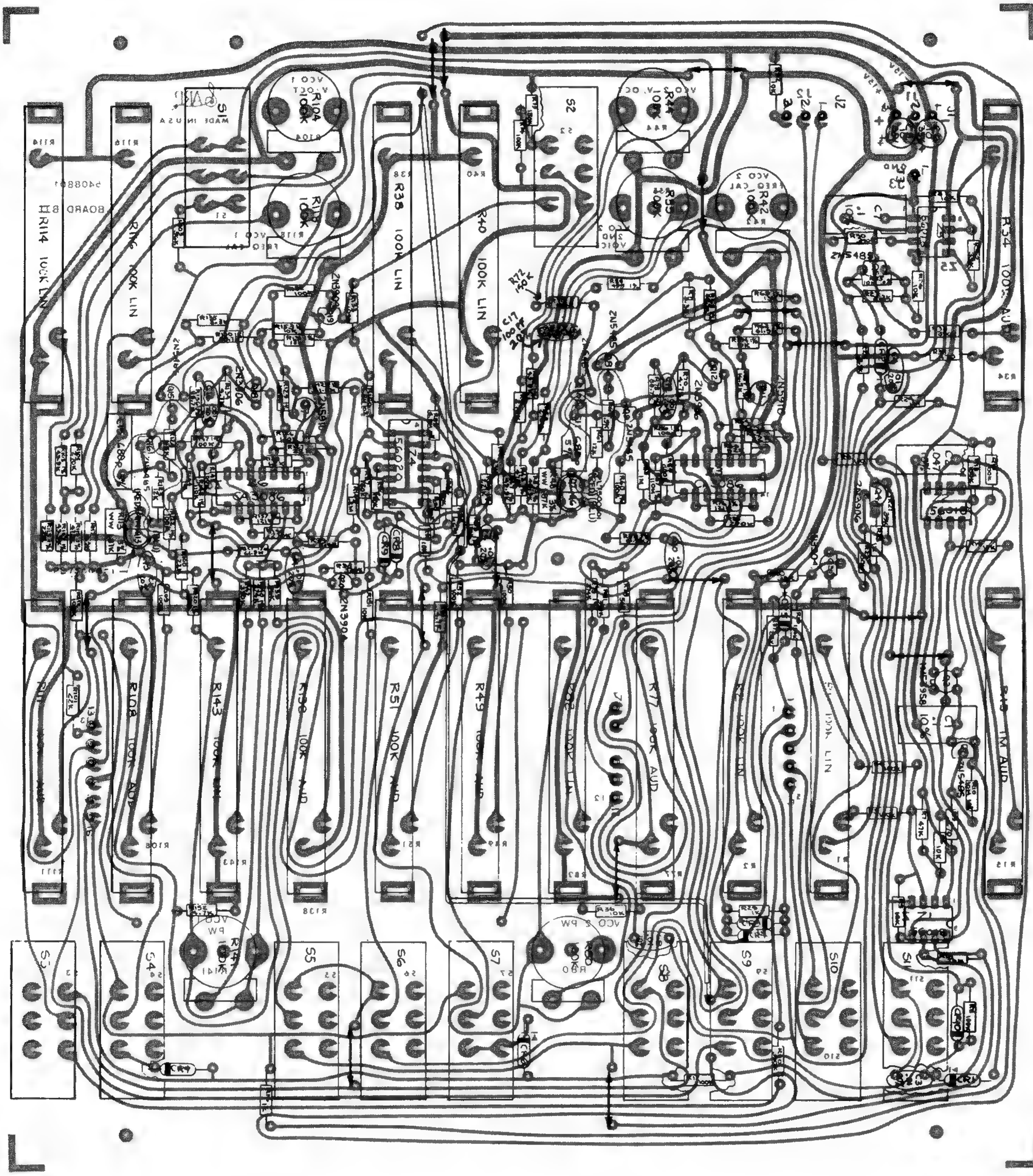
ARP ODYSSEY Model 2800
SCHEMATIC Board B-1



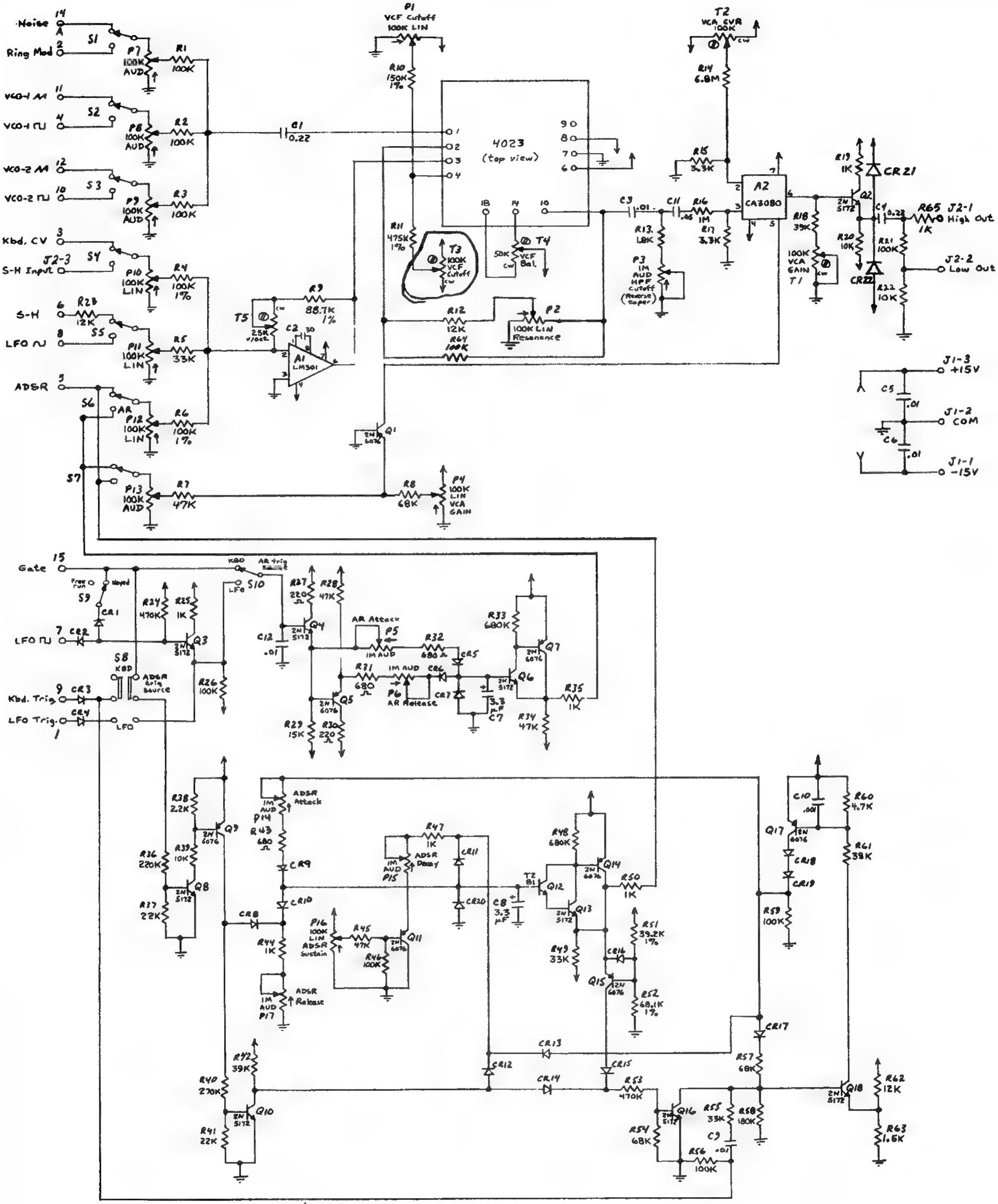
ARP ODYSSEY Model 2800
ASSEMBLY Board B-I



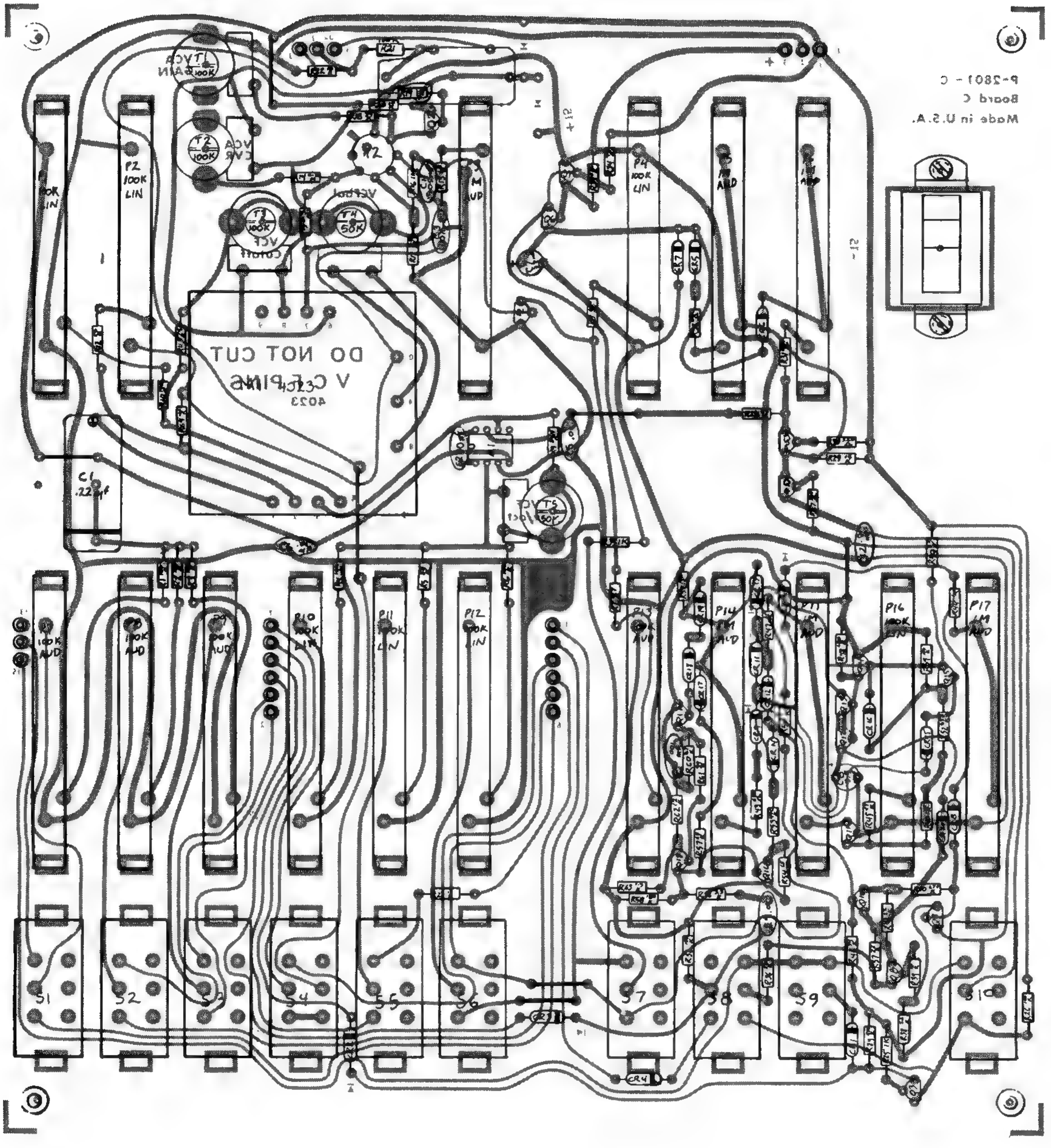
ARP ODYSSEY-2
Model 2810 - 2823
SCHEMATIC Board B-II



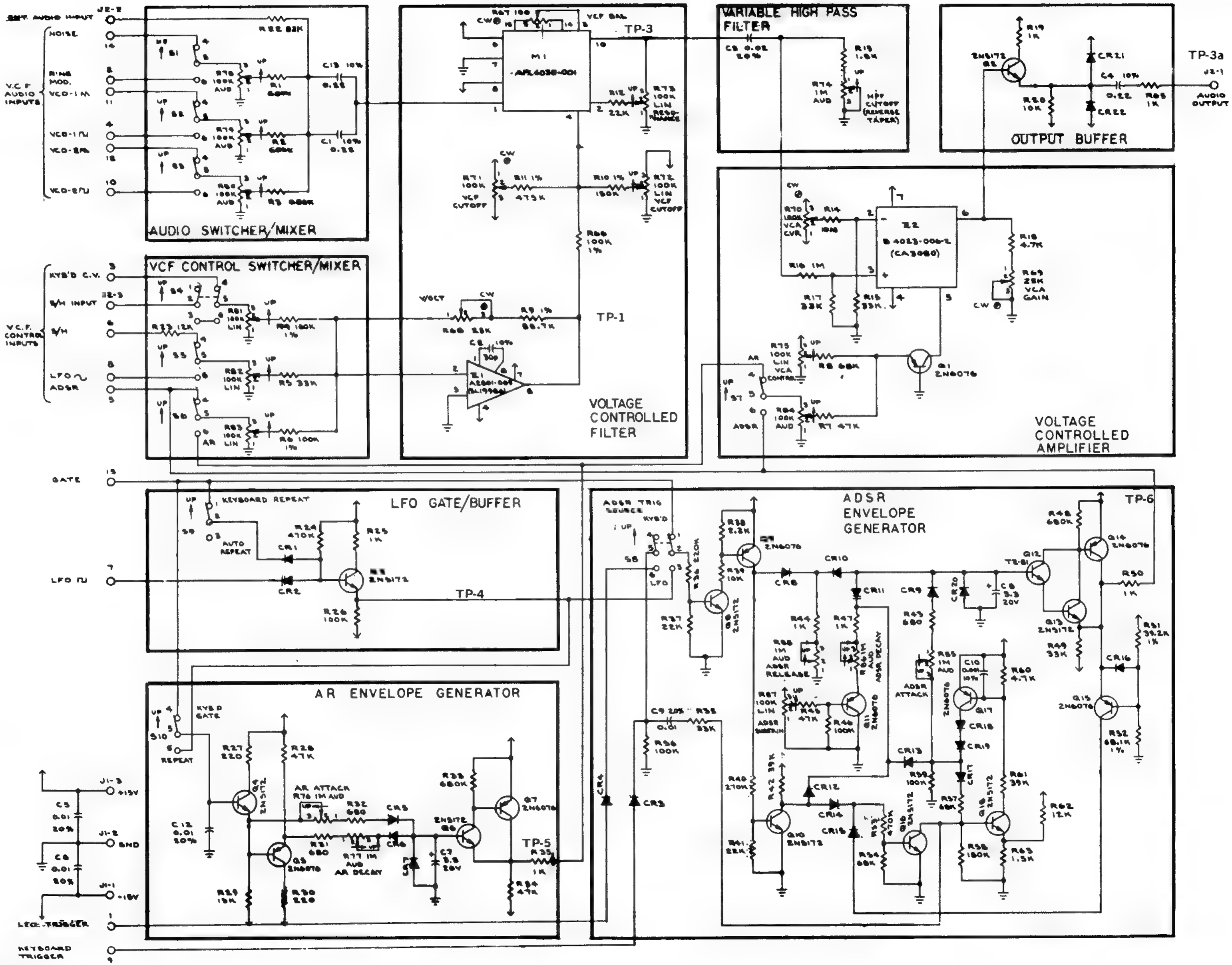
ARP ODYSSEY-2
Model 2810 - 2823
ASSEMBLY Board B-II



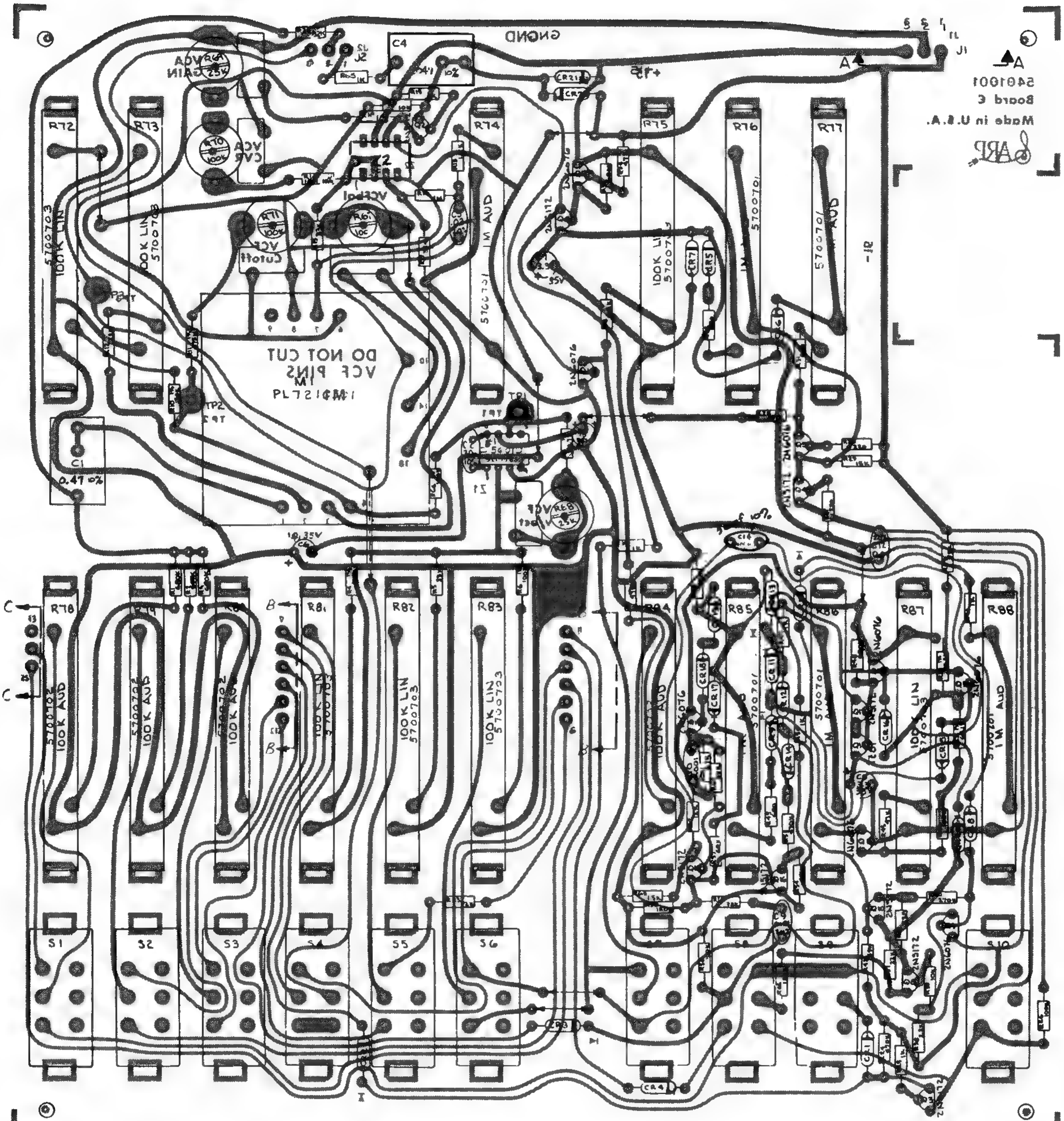
ARP ODYSSEY Model 2800
SCHEMATIC Board C-1



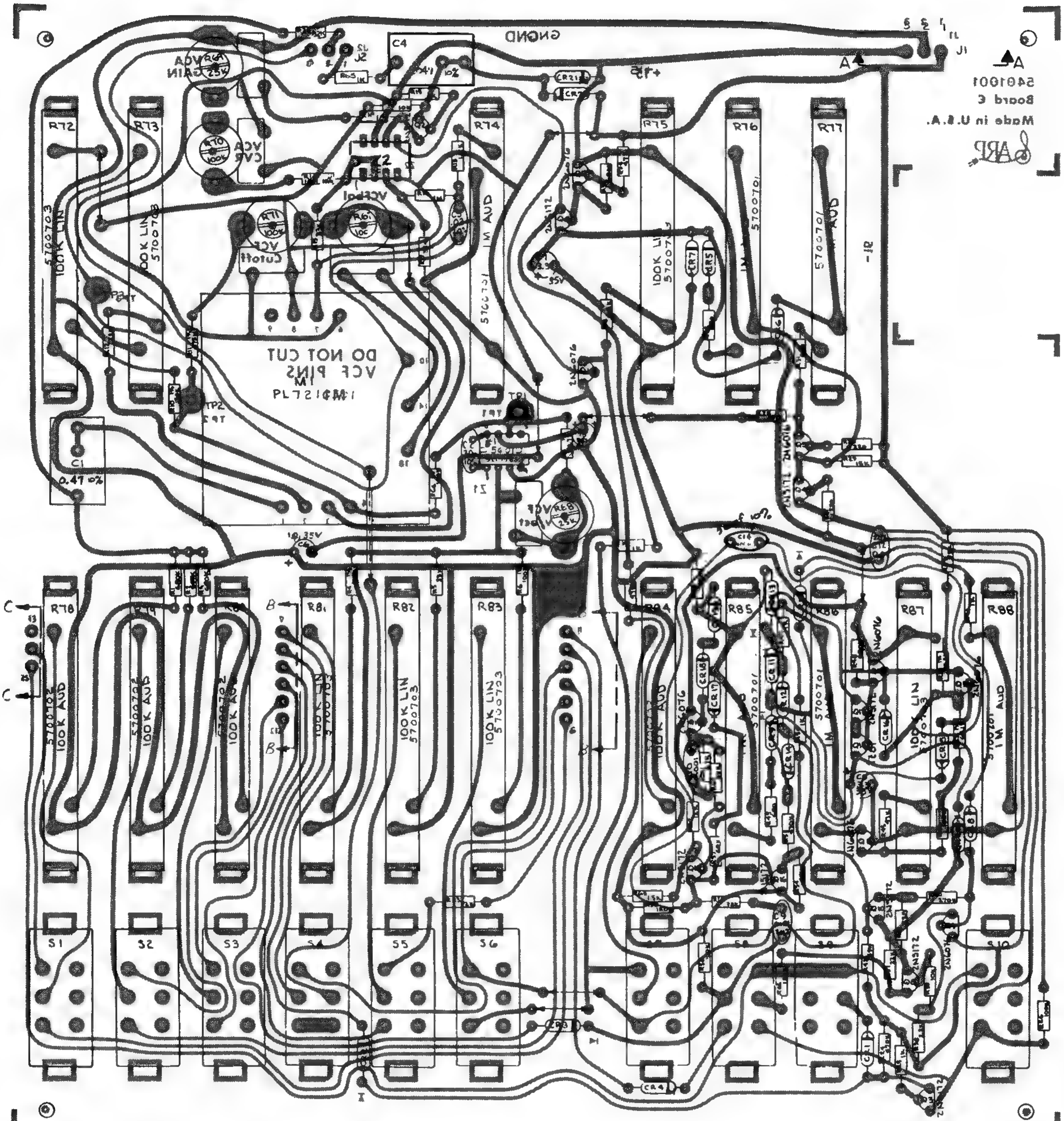
ARP ODYSSEY Model 2800
ASSEMBLY Board C-I



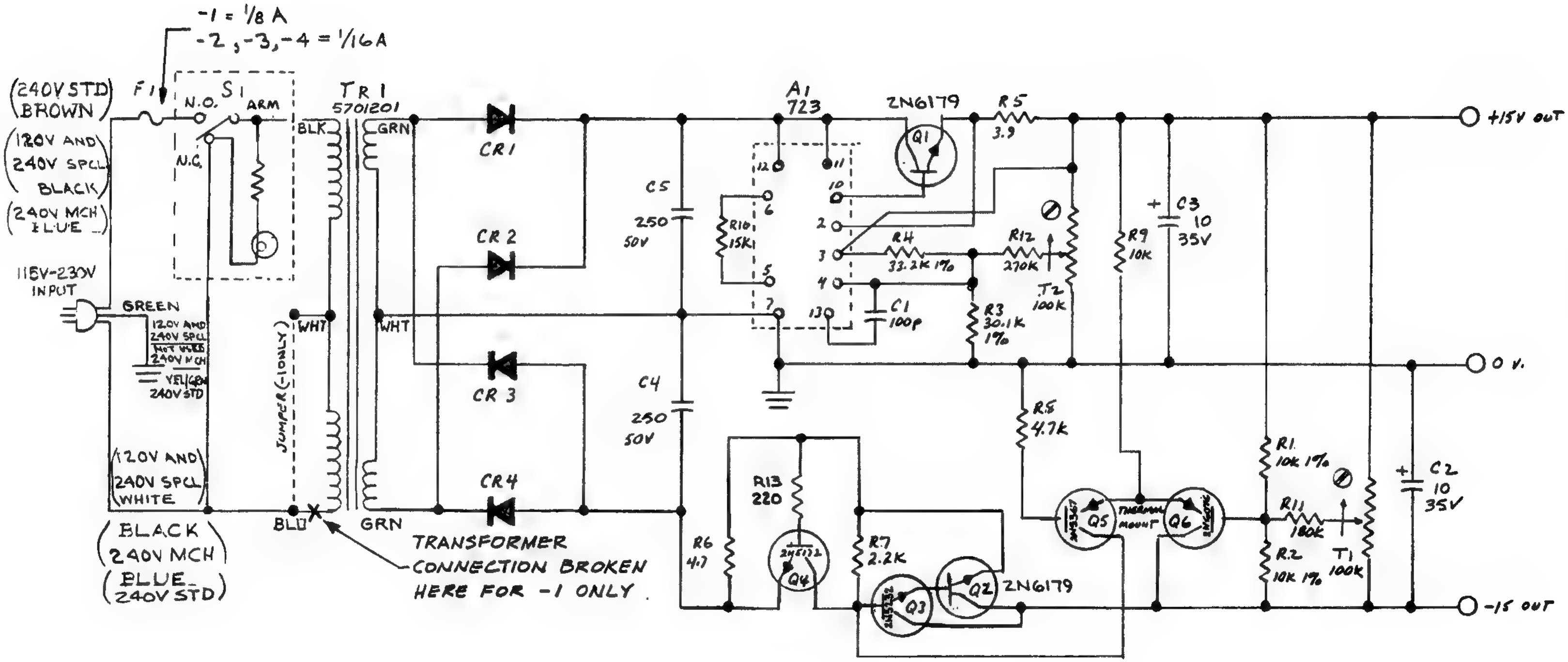
ARP ODYSSEY-2
Model 2810 - 2823
SCHEMATIC Board C-II



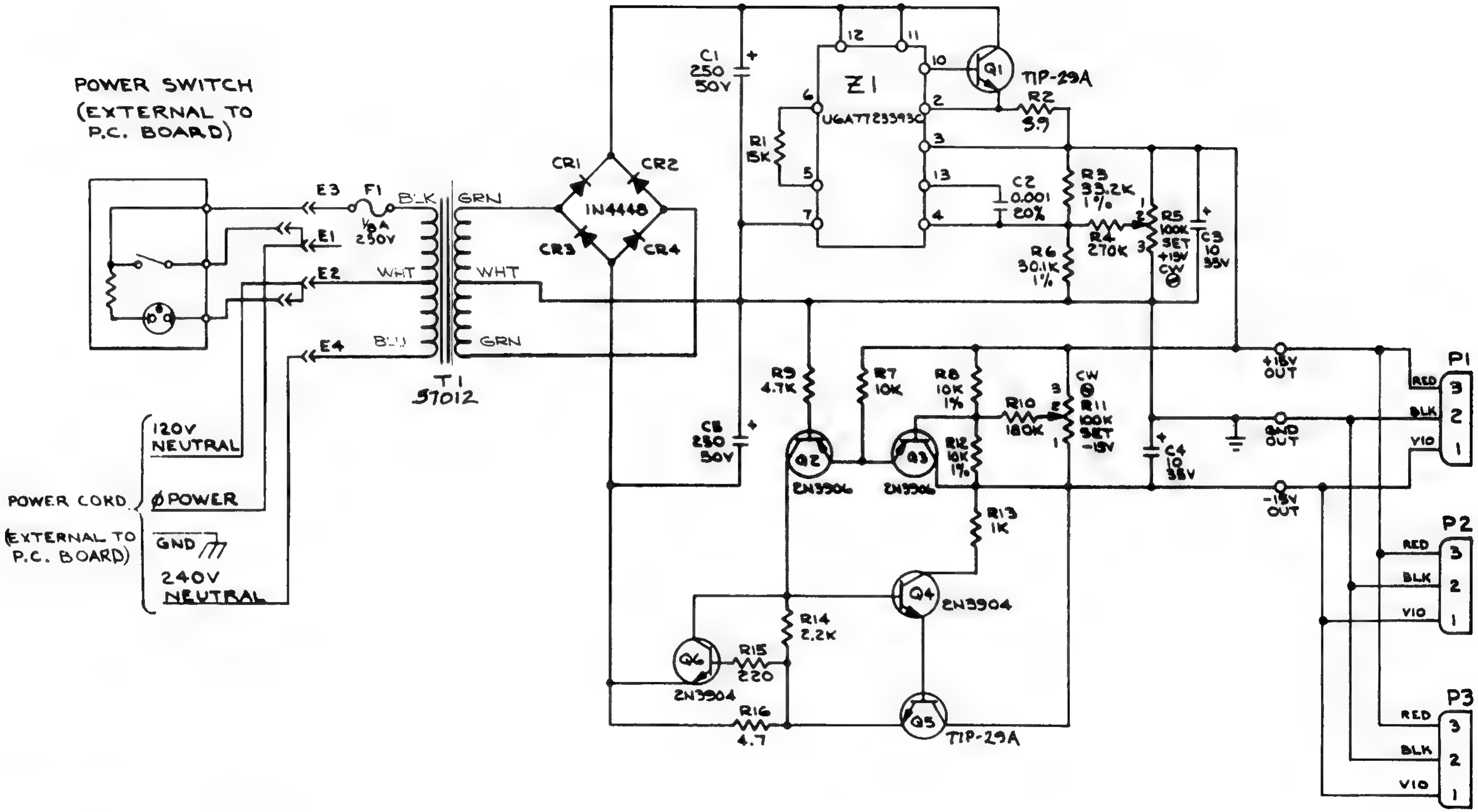
ARP ODYSSEY-2
Model 2810 - 2823
ASSEMBLY Board C-II



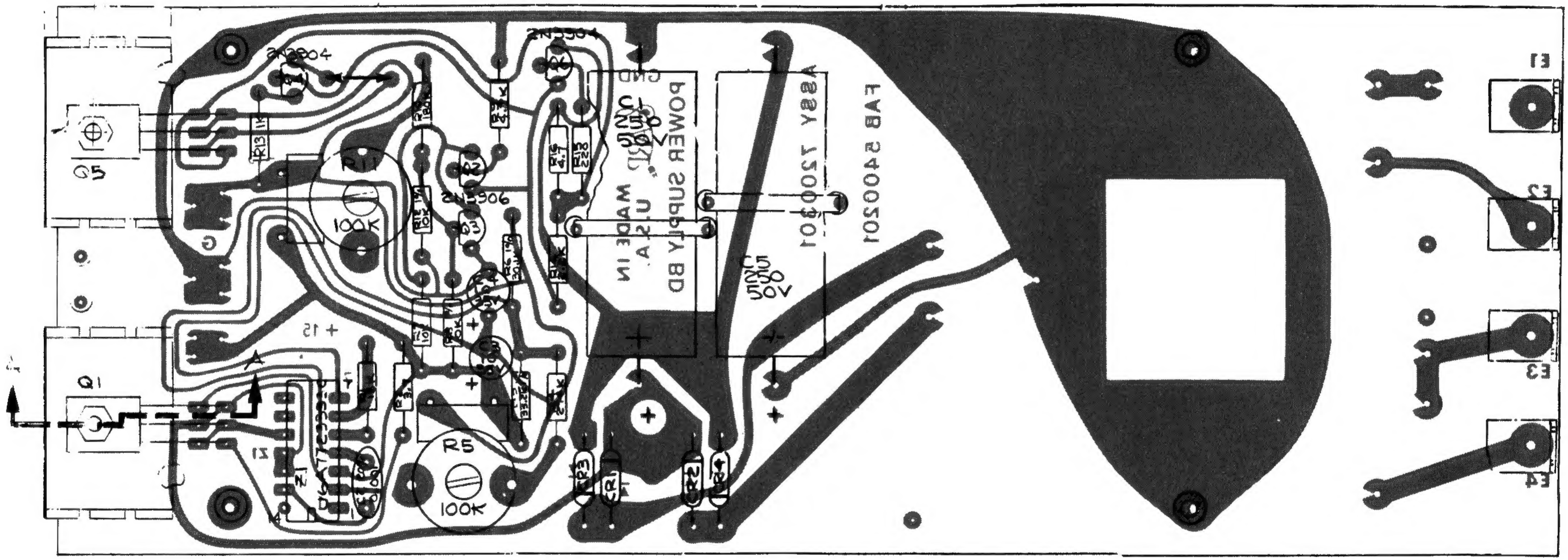
ARP ODYSSEY-2
Model 2810 - 2823
ASSEMBLY Board C-II



ARP ODYSSEY Model 2800
SCHEMATIC Power Supply- I



ARP ODYSSEY-2
Model 2810 - 2823
SCHEMATIC Power Supply-II



ARP ODYSSEY-2
Model 2810 - 2823
ASSEMBLY Power Supply-II

SECTION 7 PARTS LIST

7.1 BOARD A-I

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
A1, 2	5601801	A-2801-008A/SL 19988	DUAL OP AMP (SEL LM1458)
A3, 4	5601901	A-2801-009/SL19986	OP AMP (SEL LM301AN)
Q6,8	1303901	IMF3958	DUAL N-CHANNEL FET
Q2,3	1301701	2N5172	TRANSISTOR, NPN
Q9	5600401	A2802-014-1	TRANSISTOR, NOISE (SEL 2N5172)
Q1,4,5	1302801	2N6076	TRANSISTOR, PNP
CR1-6	1200301	IN4148	DIODE, SIGNAL
P2	1001203	B2801-006-1B	SLIDE POT, 1M LOG
P1	5701801	B-2801-010-1A	ROTARY POT, 10K LIN
T3,T4	1000903	U201R251B	TRIM POT,250
T1	1000904	R201R102B	TRIM POT,1K
T2	1000913	U201R103B	TRIM POT,10K
C8	1100901	WCR1P47	CAP.POLYCARB .47uf 10% 100V
C2	1100702	150D406X9010B	CAP.TANT .47uf 10% 35V
C4,5	1100608	G-0-001-G-10-0	CAP.TANT,1.0uf 10% 35V
S1	1900801	02-481-0001	SWITCH
S2	1902401	02-481-0006	SWITCH, SLIDE DPDT

7.2 BOARD B-I

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
A1,2,	5601801	A2801-008A	DUAL OP AMP (SEL LM1458)
A3	5601501	A4024-006-2B	OPERATIONAL TRANS AMP
Z1,2	5602001	A2803-002A	QUAD 2 INPUT NAND GATE
Q1,9,10,16,17,18	1301701	2N5172	TRANSISTOR,NPN
Q7,14	1302801	2N6076	TRANSISTOR,PNP
Q4/5,Q11/12	7502600	APL4027-008	TRANSISTOR,ASSY.NPN/PNP
Q2,8,15	1302501	2N5461	FET P-CHANNEL
Q3	5600201	A2803-003-1B	FET N-CHANNEL (MOT 2N5459)
Q6,13	5600202	A2803-003-2B	FET N-CHANNEL (MOT 2N5459)
CR1-3,5-12	1200301	1N4148	DIODE,SIGNAL
CR4	1200102	1N34	DIODE
C12,16	1101201	DM-15-681K	CAP MICA 680pf 10% 100V
C10,11	1100612	Tag-00-10/35-50/20	CAP. D TANT 10uf +50%-20%,35V
R32,44	1000105	SA-21	RES. 1.87K 3%+3500 PPM TC
P16	5700701	B2801-006-1D	SLIDE POT 1M. LOG.
P5,6,7,10,11,	5700702	B2801-006-2B	SLIDE POT 100K LOG.
P1,2,3,4,8,9,12, 13,14,15	5700703	B2801-006-3B	SLIDE POT 100K LINEAR
T1,4,7	1000909	U201R103B	TRIM POT 10K
T2,3,5,6	1000915	U201R104B	TRIM POT 100K
S1-11	1902401	01-481-0006	SLIDE SWITCH DPDT

7.3 BOARD C-I

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
M1	4023		4023 VCF MODULE
A1	5601901	A-2801-009-1	OP AMP (LM301AN)
A2	5601501	B4023-006-2B	OP TRANSCONDUCTANCE AMP
Q12	1304601	TZ81	TRANSISTOR,NPN
Q2,3,4,6.8, 10,13,16,18	1301701	2N5172	TRANSISTOR,NPN
Q2,5,7,9,11, 14,15,17	1302801	2N6076	TRANSISTOR,PNP
CR1-22	1200301	1N4148	DIODE,SIGNAL
C7,8	1100602	TAG-00-3.3/20-10/10	CAP.,TANT.3.3uf 10% 20V
P3,5,6,14,15,17	1001203	B2801-006-1D	SLIDE POT IM LOG

P7,8,9,13	1001202	B2801-006-2D	SLIDE POT 100K LOG
P1,2,4,10,11,12,16	1001201	B2801-006-3D	SLIDE POT 100K LINEAR
S11	1902602	12-000-0054	SWITCH 115 VAC
S11	1902601	02-481-0008	SWITCH 230 VAC
T4	1000913	U201R503B	TRIM POT 50K,¼W,20%
T5	1000911	U201R253B	TRIM POT 25K,¼W,20%
T1,2,3	1000915	U201R104B	TRIM POT 100K,¼W,20%
S1-10	1902401	01-481-0006	SLIDE SWITCH DPDT

7.4 POWER SUPPLY-I

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
A1	1401301	U6E7723393C	VOLTAGE REGULATOR
Q1,2	1303401	2N6179	TRANSISTOR,NPN,POWER
Q3	1301801	2N5232	TRANSISTOR,NPN
Q4	1301701	2N5172	TRANSISTOR,NPN
Q5	1302201	2N5367	TRANSISTOR,PNP
Q6	1302801	2N6076	TRANSISTOR,PNP
CR1-4	1200401	IN4448	DIODE,RECTIFIER
C2,3	1100612	TAG-00-10/35-50/20	CAP.,TANT,10uf,+50-20%,35V
C4,5	1201702	B-41010- 250/50	CAP.,ELECT.,250mf,+50-10%,50V
T1,2	1000915	U201R104B	TRIM POT.,100K,+20%,¼W
F1	1700401	MCV-1/16	FUSE,PIGTAIL,1/16A,250V
TR1	5701101	C2804-008	TRANSFORMER

7.5 BOARD A-II

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
CR1-7	1200301	1N4148	DIODE, SILICON, SIGNAL
Q1,2,6,8	1302801	2N6076	TRANSISTOR,PNP
Q4	1303901	1MF3958	TRANSISTOR,SILICON,J-FET
Q3	1301301	LS4392	TRANSISTOR,N-CHANNEL FET
Q7	1301701	2N5172	TRANSISTOR,NPN
Q5	5600101	A8000-012	TRANSISTOR,NOISE,SEL(2N5172)
Z2,4	5601801	A2801-008/SL19988	AMPLIFIER,OPL,TESTED LM1458
Z3,5	5601901	A2801-009/SL19986	AMPLIFIER,OPL,TESTED LM30IAN
Z1	5602001	A2803-002	IC,QUAD 2 INPUT NAND GATE
R23,R27	1000909	U201R103B	POT.,ROTARY,LIN,¼W,20%,10K
R29	5701802	B2801-010-2	POT.,ROTARY,LIN,30%,100K
R30	5700701	B2801-006-1	POT.,SLIDE,AUD,1/3W,30%,1M
C11,12	1100609	TAG-00-1/35-20/20	CAP.,TANT,35V,20%,1uf
C15	1100601	TAG-00-22/16-20/20	CAP.,TANT,16V,20%,22uf
C8	1100901	WCR1P47	CAP.,P CARB,100V,10%,0.47uf
S1	1900801	02-481-0001	SWITCH,ROCKER,DPTT
S2	1902401	01-481-0006	SWITCH,SLIDE,DPDT

7.6 BOARD A-II (with PPC)

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
CR2, 3, 4, 5, 6, 7 8, 9, 10	1200301	1N4148	DIODE SIGNAL
Q1, 2, 6, 8	1302801	2N6076	TSTR PNP GENERAL PURPOSE
Q4	1303901	IMF3958	TSTR N CHANNEL
Q3	1301301	2N4392	TSTR N CHANNEL
Q5	5600101	8000-012	TSTR NPN SELECT
Z2, 4	1401101	LM1458	IC OP AMP DUAL
Z3, 5	1400801	LM301AN	IC OP AMP
Z1	1400601	CD4011AE	IC GATE 4 X 2I NAND
R23	1000909	U201R103B	TRIM POT 10K ¼W 30%
R30	5700701	----------	SLIDE POT AUD 1M, 1/3W 30%
C11, 12, 16, 17	1100609	G-0-001-G-20-0	CAP TANT 1UF 35V 20%
C15	1100601	G-0-022-D-20-0	CAP TANT 22UF 16V 20%
C8	1100901	WCR1P47	CAP PLASTIC .47UF 100V 10%

7.7 BOARD B-II

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
CR1-10	1200301	1N4148	DIODE,SILICON,SIGNAL
Q3,19,20	1302901	2N3904	TRANSISTOR,SILICON,NPN
Q4,12,18	1303001	2N3906	TRANSISTOR,SILICON,PNP
Q11,17	1302701	2N5910	TRANSISTOR,SILICON,PNP
Q6,7,13,14	7500801	2300-029	TRANSISTOR PAIR,NPN/PNP
Q8,9,15,16,10	5600201	A2803-003-1	TRANSISTOR,FET,SEL,(2N5459,ORN)
Q1,5,10	5600202	A2803-003-2	TRANSISTOR,FET,SEL,(2N5459,YEL)
Q2	1303901	1MF3958	TRANSISTOR,DUAL J-FET
Z3,6	1400501	CA3086	TRANSISTOR ARRAY,NPN
Z1,2,5	5601801	A2801-008/SL19988	OP-AMP,TESTED LM1458
Z4	5602001	A2803-002	QUAD 2-INPUT NAND GATE
R48,113	1000105	SA21	RES,WIRE WOUND 3% 1.87K
R42,44,55,80,104, 118,141	1000915	U201R104B	POT,ROTARY,LIN,,1/4W,20%,100K
R1,2,38,40,82,114, 116,143	5700703	B2801-006-3	POT,SLIDE,LIN,1/3W,30%,100K
R34,49,51,77,108, 111,138	5700702	B2801-006-2	POT,SLIDE,AUD,1/3W,30%,100K
R15	5700701	B2801-006-1	POT,SLIDE,AUD,1/3W,30%,1M
C5,6	1100612	G-0-010-G-20-0	CAP,TANT,35V,20%,10uf
C11,15	1101205	ADM-19-681J	CAP,S.MICA.500V,5%,680pf

7.8 BOARD C-II

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
M1	7210500	APL4075-005	PC BD ASSY,VCF 4075 MODULE
CR1-22	1200301	IN4148	DIODE,SILICON,SIGNAL
Q2,3,4,6,8,10,13 16,18	1301701	2N5172	TRANSISTOR,NPN
Q1,5,7,9,11	1302801	2N6076	TRANSISTOR,PNP
Q12	1304601	TZ-81	TRANSISTOR,NPN
Z1	5601901	A2801-009/SL19986	AMPLIFIER,OPL,TESTED LM301AN
R67	1000901	U201R101B	POT.,ROTARY,LIN,¼W,20%,100
R68,69	1000911	U201R253B	POT.,ROTARY,LIN,¼W,20%,25K
R70,71	1000915	U201R104B	POT.,ROTARY,LIN,¼W,20%100K
R74,76,77,85,86,88	5700701	B2801-006-1	POT.,SLIDE,AUD,1/3W,30%,1M
R78,79,80,84	5700702	B2801-006-2	POT.,SLIDE,AUD,1/3W,30%100K
R72,73,75,81,82, 83,87	5700703	B2801-006-3	POT.,SLIDE,LIN,1/3W,30%,100K
C7,8	1100602	TAG-00-3.3/20-10/10	CAP.,TANT,20V,10%,3.3uf

7.9 POWER SUPPLY-III

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
CR1-4	1200401	1N4448	RECTIFIER,SILICON,75V,200 MA
Q1,5	1303401	2N6179	TRANSISTOR,NPN,PWR
Q4,6	1302901	2N3904	TRANSISTOR,SILICON,NPN
Q2,3	1303001	2N3906	TRANSISTOR,SILICON,PNP
Z1	1401301	U6A7723393C	IC,VOLTAGE REGULATOR
R5,11	1000915	U201R104B	POT.,ROTARY,LIN,¼W,10%,100K
C3,4	1100612	TAG-00-10/35-50/20	CAP TANT,35V,+50%-20%,10uf
C1,5	1101701	B41010-250/50	CAP ELECT,50V,+50%-10%,250uf
T1	5701101	C2804-008	TRANSFORMER,POWER
F1	1700402	MDV-1/8	FUSE,PIGTAIL,1/8A,250V