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Analysis and design of class-E power amplifier considering MOSFET nonlinear capacitance

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ABSTRACT

Class-E power amplifiers are integrated into many applications because their simple design and high performance. The efficiency of the power amplifier is significantly impacted by the nonlinear characteristic of the switching device, which is not analyzed clearly in theory. The nonlinear drain-to-source parasitic capacitance of the power transistor and the linear external capacitance are both contributed to the optimum conditions for obtaining the exact shunt capacitance. In this paper, a high-efficiency class-E power amplifier with shunt capacitance is designed with the consideration of both linear and nonlinear capacitance. Furthermore, a mathematical analysis is derived to calculate the component values in order to design the class-E power amplifier. Consequently, high power-added efficiency of 94.6% is obtained using MRF9030 MOSFET transistor with parameter of 4W output power and 13.56 MHz operating frequency. Finally, the measurement result of a linear class-E power amplifier circuit is obtained to compare and realize the efficiency of the proposed work.

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1. INTRODUCTION

The main purpose of power amplifier system is reducing significantly the power consumption to optimize the efficiency of system operation. One of the most important factors that impact on such efficiency, is power added efficiency (PAE) [1]–[7]. There are several switch-mode amplifier structures such as class-E, D, F, and inverse class-F power amplifier have been introduced to archive high efficiencies. Each switch-mode class has some advantages and disadvantages depending on the specific application [8]–[12]. For instance, the class-D power amplifier is suitable for audio and RF frequencies application. Therefore, this amplifier archives low efficiency at high frequencies because a remarkable energy loss is caused of parasitic reactance of the device [13]. Meanwhile, the class-F and the inverse class-F power amplifier are proposed to control harmonic components in case of operating in a saturation region of the device in order to mitigate overlapping between waveform of current and voltage. Unfortunately, a certain large number of harmonics has to put under control to improve the efficiency [14], [15]. Therefore, the harmonic controlling circuit becomes extremely complex and voluminous.

The integration of class-E power amplifier and a shunt capacitor was manufactured with the PAE theoretically reaching nearly 100% [16]–[18]. However, the actual operation of a linear shunt capacitance factor in class E power amplifier is not similar to its theoretical analysis. The overall value of shunt capacitance is significantly increased by nonlinear of switch component, specifically, its parasitic drain-to-

source capacitance. Therefore, regarding to the operation of the class-E power amplifier, the nonlinear capacitance must be considered. In [19], [20], the author presented an analysis and design method of the class E amplifier for both nonlinear and linear shunt capacitance. In this work, in order to figure out results of a numerical analysis of the design equations for extracting the component values in the class E amplifier, the supported figures and tables is examed. However, the analysis neglected the dependence of the junction capacitance on the characteristic capacitance of the transistor leading to an inaccurate capacitance extraction. Therefore, to design a class-E power amplifier integrated both a nonlinear and linear capacitance, the equations should be solved for a specific MOSFET transistor without the inheritance of the design process in previous literature.

In this paper, the class-E power amplifier with nonlinear and linear capacitance are a deeply analyzed to explain the dependence of the shunt capacitance with the specific MOSFET transistor to calculate the accurate nonlinear capacitance. A mathematical analysis is derived to archieve electronic component values of the circuit. In addition, the equations of a specific MOSFET transistor depend on its own parameters. A design process of the class-E power amplifier is presented to obtain the maximized PAE for an arbitrary MOSFET transistor. The zero-voltage switching (ZVS) and zero-voltage-derivative switching (ZVDS) conditions are used to obtain the exact components for the power amplifier, which ensure minimizing switching loss, low noise, and enhances component tolerances [21]–[25]. In addition, the PAE of the proposed work is compared with the linear capacitance class-E amplifier to evaluate efficiency improvement. Finally, the proposed power amplifier is fabricated and measured to verify the high performance with the exactly calculated nonlinear capacitance.

This paper is organized as follows. The circuit analysis and extracted parameters for the components of the class-E power amplifier are presented in section 2. The mathematical equations are founded to evaluate the dependence of the nonlinear capacitance on the operating frequency. The fabrication and measurement of the proposed class-E power amplifier are demonstrated in section 3. Finally, a comparison between the proposed method and a linear class-E power amplifier is shown to present the efficiency improvement.

2. CIRCUIT ANALYSIS AND PARAMETERS

The integrated circuit between class-E amplifier and shunt capacitance is illustrated in Figure 1. The MOSFET transistor plays as a switch device and the series resonant circuit is RLC. C_0 and C_e are MOSFET drain-to-source capacitance and the external linear capacitance of the shunt capacitance respectively. The equation of total shunt C_{shunt} is given:

$$C_{shunt} = C_0 + C_e = \frac{C_{j0}}{\sqrt{1+\frac{v_s}{V_{bi}}}} + C_e \quad (1)$$

where v_s and V_{bi} are the drain-to-source voltage and the built-in potential of the MOSFET body diode respectively, and C_{j0} is defined as the shunt capacitance at v_s=0V.

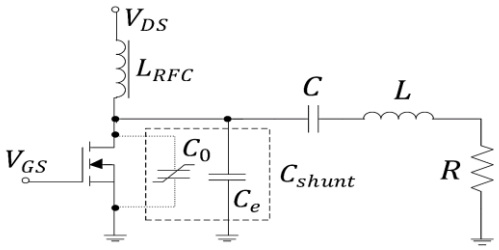

Figure 1. The circuit of class-E power amplifier

During the operating time, the switch voltage has to adapt the ZVS condition. Because the measured value of the dc component of the voltage drop across the choke inductor L_{RC} is zero, the dc supply voltage V_{DS} *is equal* the average value of the switch voltage and depends on the drain-to-source voltage v_s in case the status of switch is off, i.e for $0 < \theta = \omega t \leq 2\pi$:

$$V_{DS} = \frac{1}{2\pi}\int_0^{2\pi} v_s(\theta)d\theta \quad (2)$$

The drain-to-source voltage v_s can be extracted by the integration of the drain current in (3):

$$\omega \int_0^{v_s} \left(\frac{C_{j0}}{\sqrt{1+\frac{v_s}{V_{bi}}}} + C_e\right) dv_s = \int_0^{\theta} i_C d\theta \quad (3)$$

Substituting the v_s into in (2) and then expanding, we obtain the equation as followed:

$$\frac{V_{DS}}{V_{bi}} = \frac{\delta}{\pi}\left[\pi(\delta + \beta \sin\emptyset \cos\emptyset + 1) + \beta\left(\frac{\pi^2}{2} + 2\right)\sin^2\emptyset\right] - \frac{\delta}{\pi}\int_0^{\pi}[\delta^2 + 2\delta + 1 + 2\delta\beta \sin\emptyset\cos\emptyset\ 2\delta\beta\theta \sin^2\emptyset - 2\delta\beta \sin\emptyset \cos(\beta + \emptyset)]^{\frac{1}{2}} d\theta \quad (4)$$

Where:

$$\beta = \frac{V_{DS}}{2\pi f R C_{j0} V_{bi}} \text{ and } \delta = \frac{C_{j0}}{C_e} \quad (5)$$

and $\emptyset$ is the phase difference between input and output signals.

A nonlinear function of optimization was applied to the in (4) with the aim of obtaining an analysis solution through using the toolbox of MATLAB software because this equation could not be integrated. The solution is shown in Figure 2 that describe the dependence of δ and the operating frequency f with the given values of V_{DS} and P_0. From this figure, it is obvious to determine the ratio δ of the junction capacitance C_{j0} and the external capacitance C_e at a specification frequency. Therefore, the external capacitance C_e can be obtained by deducing from the C_{j0}:

$$C_{j0} = (C_{oss} - C_{rss})\sqrt{1 + \frac{25}{V_{bi}}} \quad (6)$$

where C_{oss} and C_{rss} which are given in datasheet of MOSFETs, are in turn the output capacitance and reverse transfer capacitance of the transistor. Moreover, in (4), the junction capacitance C_{j0} is still exising in β, which infers from the parasitic parameters of the transistor. Consequently, the result of the in (4) is obtained for only the transistor that has the extracted C_{j0}.

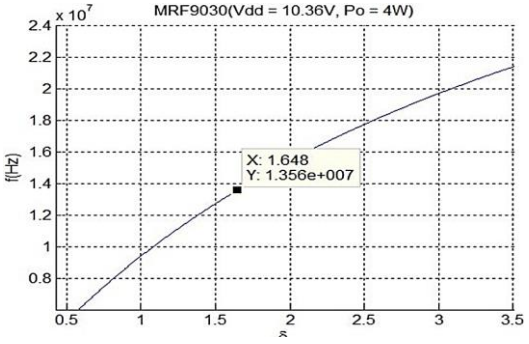

Figure 2. The relationship between frequency f and dependence of δ

The remained component values of circuit in Figure 1 can be calculated by:

$$R = \frac{8V_{DS}^2}{(\pi^2+4)P_0} \quad (7)$$

$$X = R\,tan(\emptyset + 0.567) \quad (8)$$

$$L = \frac{RQ}{\omega}\ and\ C = \frac{1}{\omega(RQ-X)} \quad (9)$$

Where Q is the quality factor. Then, the choke inductor L_{RFC} is calculated as:

$$L_{RFC} = 2\left(\frac{\pi^2}{4} + 1\right)\frac{R}{f} \quad (10)$$

Since the above analyzed results, the designed schematic design of class-E power amplifier circuit is depicted in Figure 3. Regarding to this schematic, to minimize the power loss, the output load matching

network is constructed by $L_{o-match}$ and $C_{o-match}$ to shape the output voltage and current. Meanwhile, $L_{i-match}$ and $C_{i-match}$ are two factors which constitute the input combining network. However, these factors do not have many effects on the total circuit performance. Figure 4 depicts the simulated voltage and current waveform under the optimum operation. There is a slight overlap with each other that leads to the minimized power attenuation on the MOSFET. The voltage across the switching device is proved to satisfy the ZVS and ZVDS conditions. Therefore, the class-E amplifier with the nonlinear capacitance consideration presents an approximately perfect operation of an idea class-E power amplifier.

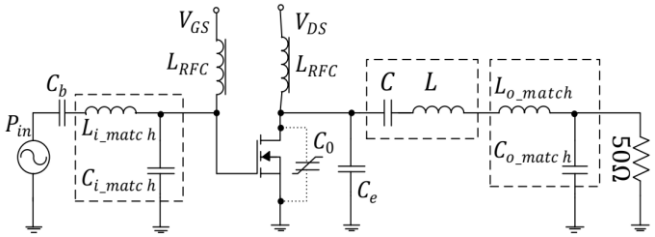

Figure 3. The designed circuit of class-E power amplifier

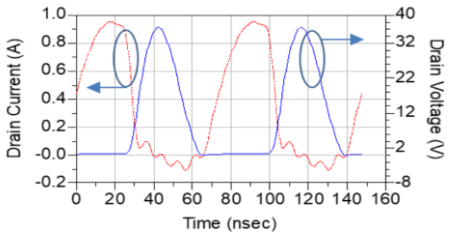

Figure 4. The simulation waveforms of drain current and voltage

3. CIRCUIT DESIGN AND PERFORMANCE EVALUATION

The proposed circuit of class-E power amplifier was fabricated to evaluate the performance using an MRF9030 MOSFET. From the above analysis, the component values were calculated, simulated, and implemented as demonstrated in Table 1. The values in the simulation and measurement are optimized for accumulating the highest efficiency cause a slight difference. Figure 5 shows the experimental results of the proposed circuit. The output power is measured using an Agilent 85665EC spectrum analyzer. Because the spectrum analyzer is limitated at maximum measurement output of 30 dBm, and an attenuator of -37.67 dB is added at the end of the circuit. Finally, the output power is achieved at 36 dBm or 3.98 W, which is the sum of the attenuator and the measurement value in the monitor of the analyzer network. The PAE value of 94.6% is extracted by:

$$PAE = \frac{P_{out}-P_{in}}{P_{dc}} = \frac{P_{out}-P_{in}}{V_{GS}I_{GS}+V_{DS}I_{DS}} = \frac{P_{out}-P_{in}}{V_{DS}I_{DS}}\% \quad (11)$$

Table 1. The comparision of parameter class-E in different methods

Components	Calculation	Simulation	Measurement
C_e	111 pF	111 pF	110 pF
C	86 pF	82 pF	82 pF
L	1.8 uH	1.8 uH	1.8 uH
L_{RFC}	7.9 uH	8.2 uH	10 uH
$L_{o-match}$		270 uH	270 uH
$C_{o-match}$		360 pF	360 pF
$L_{i-match}$		270 uH	270 uH
$C_{i-match}$		91 pF	91 pF

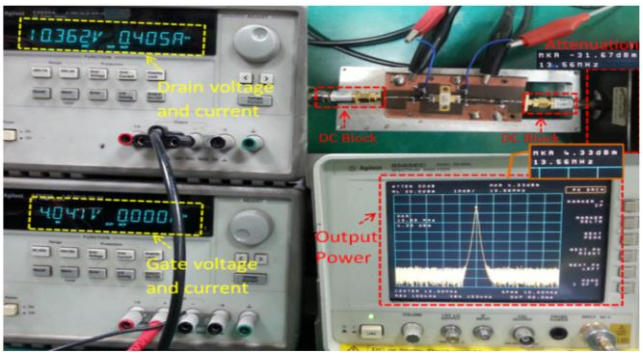

Figure 5. Measurement of class-E power amplifier circuit

The gate-to-source current I_{GS} can be ignored or appropriately zero. The drain-to-source voltage V_{DS} and gate-to-source voltage V_{GS} are supplied by 10.36 V and 4 V, respectively. The external capacitor C_e is chosen by the calculation based on the dependence of the δ value on the frequency for a specific condition. A comparison between the simulation and experiment results of the gain and PAE has a remarkable outcome, as shown in Figure 6. The highest PAE of the proposed amplifier can be obtained at 10 dBm input power and power gain of 25 dB. The system can maintain the PAE higher than 80 % with the lowest input power of approximately 3 dBm, which presents a good performance of the proposed class-E power amplifier. To evaluate the efficiency of the proposed nonlinear capacitance class-E power amplifier, the design of the linear shunt capacitance class-E PAE circuit was experimented to compare the performance. The design method of the linear shunt capacitance class-E amplifier is referred to as the set of equations, which is presented by Sokal [11]. A contrast between two amplifiers with parameter values and efficiency is shown in Table 2. The total shunt capacitance in two cases has a tolerance of 60 pF. In the linear shunt capacitance class-E circuit, the drain current is higher than the one in the proposed circuit; whereas, the output power is lower. Therefore, the dissipated power in the switch device is increased significantly in the linear class-E amplifier, which has about 8% of PAE less than the proposed circuit. In consequence, to compare with the conventional linear of class-E power amplifier, the PAE of the class-E power amplifier with a consideration of nonlinear capacitance for a specific condition can be improved significantly.

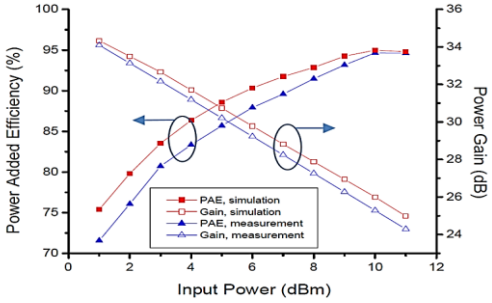

Figure 6. The result of gain and PAE in both simulation and measurement

Table 2. Comparison between the linear and composed of linear and nonlinear shunt capacitance class-E amplifier circuits

Parameters	Linear circuit	Proposed circuit
V_{DS}	10.36V	10.36V
V_{GS}	4V	4V
I_{DS}	0.412A	0.405A
I_{GS}	0A	0A
C_e	170pF	110pF
P_{in}	10dBm	10dBm
P_{out}	35.67dBm/ 3.69W	36dBm/3.98W
PAE	86.2%	94.6%

4. CONCLUSION

This work analyzed a practical class-E power amplifier circuit, which was designed using the composition of the nonlinear drain-to-source capacitance of the switching device and the external linear capacitance. A mathematical analysis is derived to obtain the exact value of the external capacitance. The PAE value of the proposed technique is improved significantly in comparison to the linear class-E circuit. The measured results indicated that a high result of PAE of 94.6% is achieved at 4W output power level and 13.56 MHz operating frequency.

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