DDX Multichannel Digital Audio Processor

FEATURES

- SOURCE-TO-SPEAKER INTEGRATED DIGITAL AUDIO SOLUTION WITH DDX-2060 POWER ICs
- DIGITAL PREAMP FUNCTIONS:
  - Digital Volume Control
  - Bass and Treble
  - Parametric EQ on each Channel
  - Bass Management for LFE Channel
  - Soft Mute
  - Automatic Mute for Zero Inputs
- 4+1 CHANNELS DDX PROCESSING
- STEREO S/PDIF INPUT INTERFACE
- 4 CHANNEL PROGRAMMABLE SERIAL INPUT INTERFACE
- 6 CHANNEL PROGRAMMABLE SERIAL OUTPUT INTERFACE
- Intel AC'97 LINK (rev.2.1) INPUT INTERFACE for AUDIO AND CONTROL
- AUTOMATIC INPUT SAMPLING FREQUENCY DETECTION AND SAMPLE RATE CONVERTER
- I^2C CONTROL BUS
- LOW POWER 3.3V CMOS TECHNOLOGY
- EXTERNAL INPUT CLOCK OR BUILT-IN XTAL OSCILLATOR
- DIGITAL GAIN CONTROL; UP TO +24dB @ 0.75 dB/STEP

1. GENERAL DESCRIPTION

The DDX-4100A Digital Audio Processor is a single chip device for implementing complete digital solutions for audio amplification. In conjunction with multiple DDX-2060 or DDX-2100 Power IC's, the solution provides a full digital, multi-channel, high quality, power processing chain without the need of Digital-to-Analog converters between the DSP and power amplifier.

The device supports two input configurations, AC'97 input mode or I²S / S/PDIF input mode, with the selection made via a dedicated pin (*AC97_MODE pin*).

The AC'97 input mode can be configured to work in either a 'Fully Compliant' mode or a 'Proprietary' mode. The selection of this compliance mode is made in a Vendor Reserved register. The 'Fully Compliant' mode conforms to rev. 2.1 of the AC'97 specification. The 'Proprietary' mode enables additional features not found in the 'Fully Compliant' mode. The link supports up to 6 input channels with discrete sampling frequencies of 44.1, 48, 88.2, or 96 kHz.

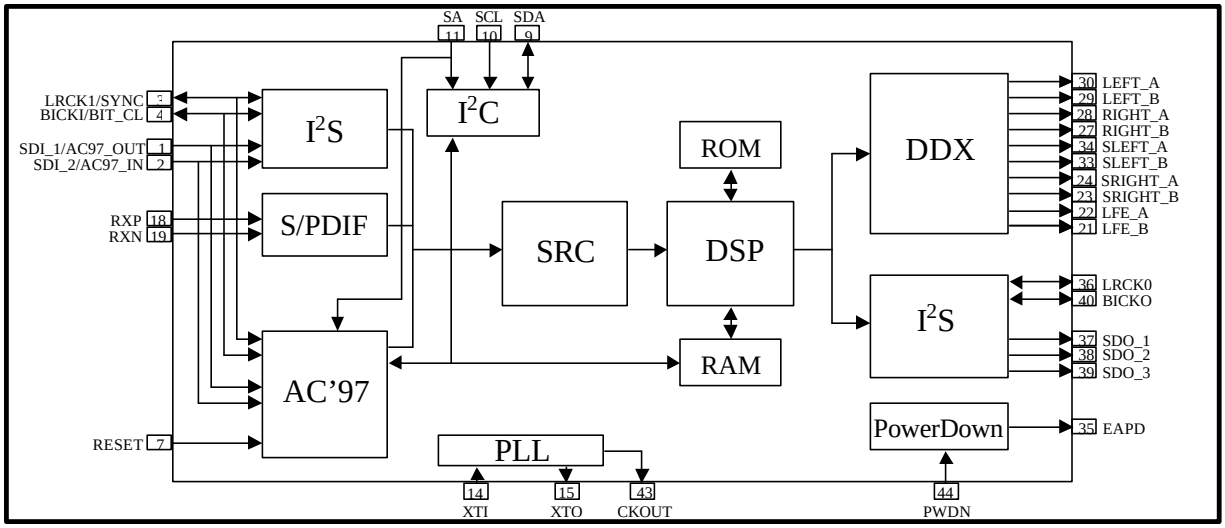


Figure 1. Block Diagram.

GENERAL DESCRIPTION (Continued)

In the I²S / S/PDIF mode, a stereo S/PDIF and a 4 channel three-wire programmable serial input interface support any sampling frequency in the continuous range from 32 to 96 KHz. The programmable serial interface supports up to four channels including the standard I²S protocol. Operation of the S/PDIF or the I²S inputs is mutually exclusive.

An embedded high quality sample rate converter (SRC) re-samples input data at the internal fixed sampling frequency of 48 kHz for DSP operations. The DSP is a 20 x 20 bit core audio processor performing several user controlled parametric algorithms, among them are static equalization, Bass, Treble, Volume control and more. The DSP operates at 49.152MHz (1024 x FS). This frequency is generated by an internal PLL with programmable multiplication factor (x2 or x8) in conjunction with the built-in oscillator or an external clock input.

The device includes 5 channels of Direct Digital Amplification (DDX™), providing PWM output signals used to directly drive external high efficiency class-D power bridge stages (DDX-2060 or DDX-2100). Additionally, a programmable 6-channel digital output interface (supporting I²S standard protocol) is embedded for applications with standard audio D/A converters. The output sampling frequency is fixed at 48 kHz when the interface operates as a master. An over-sampling clock (256 x FS or 512 x FS) is provided for external D/A converters.

An I²C interface allows programming of internal algorithms and control registers via an external controller. Arbitration logic handles access conflicts to embedded control registers (which may occur as a consequence of simultaneous access to control registers by Aclink, I²C and DSP blocks).

1.1. PIN CONNECTION (Top View)

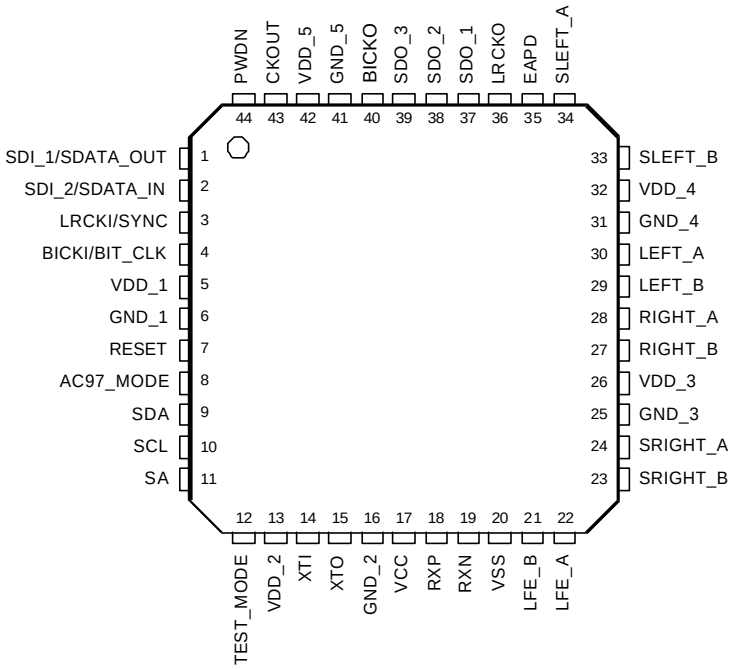


Figure 2. Pin Connection Diagram.

1.2. PIN FUNCTION

PIN	NAME	TYPE	DESCRIPTION	FAN - IN / OUT
1	SDI_1/SDATA_OUT	I	Input I^2S Serial Data 1/AC97 Output Data (I^2S mode maps to L,R DDX)	
2	SDI_2/SDATA_IN	I/O	Input I^2S Serial Data 2/AC97 Input Data (I^2S mode maps to LS,RS DDX)	2mA
3	LRCKI/SYNC	I/O	Input I^2S Left/Right Clock/AC97 Synch. Clock	2mA
4	BICKI/BIT_CLK	I/O	Input I^2S Serial Clock/AC97 Bit Clock	4mA
5	VDD_1		Digital Supply Voltage	
6	GND_1		Digital Ground	
7	RESET	I	Global Reset (Active Low) This pin is sensed only after 2 clock cycles	CMOS Schmitt In Pull-Up
8	AC97_MODE	I	AC97 Enable/Disable (1=AC97; 0=I^2S/SPDIF)	CMOS Schmitt In Pull-Down
9	SDA	I/O	I^2C Serial Data	2mA
10	SCL	I	I^2C Serial Clock	
11	SA	I	Select Address (I^2C/AC97)	
12	TEST_MODE		Connect pin to ground	CMOS In Pull-Down
13	VDD_2		Digital Supply Voltage	
14	XTI	I	Crystal Oscillator Input (Clock Input)	Analog IN
15	XTO	O	Crystal Oscillator Output Do Not Load	
16	GND_2		Digital Ground	
17	VCC		Analog Supply Voltage	
18	RXP	I	S/PDIF receiver positive (L,R DDX)	Analog In
19	RXN	I	S/PDIF receiver negative (L,R DDX)	Analog In
20	VSS		Analog Ground	
21	LFE_B	O	PWM LFE (subwoofer) channel output (B)	3mA
22	LFE_A	O	PWM LFE (subwoofer) channel output (A)	3mA
23	SRIGHT_B	O	PWM Surround right channel output (B)	3mA
24	SRIGHT_A	O	PWM Surround right channel output (A)	3mA
25	GND_3		Digital Ground	
26	VDD_3		Digital Supply Voltage	
27	RIGHT_B	O	PWM Right channel output (B)	3mA
28	RIGHT_A	O	PWM Right channel output (A)	3mA
29	LEFT_B	O	PWM Left channel output (B)	3mA
30	LEFT_A	O	PWM Left channel output (A)	3mA
31	GND_4		Digital Ground	
32	VDD_4		Digital Supply Voltage	
33	SLEFT_B	O	PWM Surround Left channel output (B)	3mA
34	SLEFT_A	O	PWM Surround Left channel output (A)	3mA
35	EAPD	O	External Amplifier Power down (Active Low)	3mA
36	LRCKO	I/O	I^2S Left/Right Clock	2mA
37	SDO_1	O	I^2S Serial Data 1 Output (L, R)	2mA
38	SDO_2	O	I^2S Serial Data 2 Output (LS, RS)	2mA
39	SDO_3	O	I^2S Serial Data 3 Output (C, SUB)	2mA
40	BICKO	I/O	I^2S Serial Clock	4mA
41	GND_5		Digital Ground	
42	VDD_5		Digital Supply Voltage	
43	CKOUT	O	Clock Output (256 x FS or 512 x FS)	8mA
44	PWDN	I	Device Power down (Active Low)	CMOS In Pull-Up

Table 1

1.3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply	-0.3 to 4	V
V_i	Voltage on input pins	-0.3 to VDD+0.3	V
V_o	Voltage on output pins	-0.3 to VDD+0.3	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_a	Ambient operating temperature	-20 to +85	°C

1.4. THERMAL DATA

Symbol	Parameter	Value	Unit
$R?_{j\text{-}a}$	Thermal resistance Junction to Ambient	85	°C/W

1.5. RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Value
V_{DD}	Power Supply Voltage	3.0 to 3.6V
T_j	Operation Junction Temperature	-20 to 125 °C

1.6. ELECTRICAL CHARACTERISTICS (VDD= 3.3±0.3V; T_a=0 to 70°C; unless otherwise specified)

1.6.1. GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{il}	Low Level Input Current Without pull-up/dn device	Vi – 0V	-10		10	µA	1
I_{ih}	High Level Input Current Without pull-up/dn device	Vi – V_{DD} = 3.6V	-10		10	µA	1
V_{esd}	Electrostatic Protection	Leakage < 1µA	2000			V	2

1.6.2. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
V_{il}	Low Level Input Voltage				0.2*V_{DD}	V	
V_{ih}	High Level Input Voltage		0.8*V_{DD}			V	
V_{ol}	Low Level Output Voltage	Iol = X mA			0.4*V_{DD}	V	3
V_{oh}	High Level Output Voltage		0.85*V_{DD}			V	3
I_{pu}	Pull-up current	V_i = 0V; V_{DD} = 3.3V	-26	-66	-125	µA	4
R_{pu}	Equivalent Pull-up resistance			50		kohm	
Tr	Reset Active Time			2*Tck		ns	
Tck	Master Clock Period			20.345		ns	

Note 1: See Table 1 for input pins with pull-up/down

Note 2: Human Body Model

Note 3: X is the source/sink current under worst-case conditions and is reflected in the name of the I/O cell according to the drive capability, see Table 1for values.

Note 4: Min condition: V_{DD} = 2.7V; Max condition: V_{DD} = 3.6 V

1.6.3. DIGITAL CHARACTERISTICS – S/PDIF RECEIVER (RXP, RXN pins only)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
Vth	Differential input voltage		200			mV	
Vhyst	Input Hysteresis			50		mV	

1.7. DESIGN CONSIDERATIONS

These specifics must be considered for design of DDX-4100A systems:

- *Using the SRC, Serial Data input signals, in I²S or S/PDIF format, must be valid before commanding the speakers to unmute. Failure to use a valid input signal will apply a DC level to the speakers and could cause damage. See sections 6.2 and 6.3 for more information.*
- *Only a 24.576MHz crystal or clock input may be used with the DDX-4100A.*
- *When using the DDX-4100A in dual processor configuration, there is an operational error when using the combination of I^2C address = 0011 111x (SA {pin 11} connected to Vdd) and serial I^2S input SDI1 (pin 1). See section 11.4 for more information.*

2. AC'97 REGISTER BANK OVERVIEW

The AC'97 interface is compliant with 'Audio Codec '97 – Revision 2.1' specification in terms of the protocol used. All of the registers described in this specification, including Standard, Vendor Reserved and Extended Audio (AC'97 2.0) registers, are available in the device, however, only relevant registers (Register Summary in section 12) are implemented.

2.1. Reading AC'97 Registers

The AC'97 register bank is implemented as a contiguous RAM space, from a DSP point of view, as the result of a read operation the content of the RAM itself will be returned. This should be followed as the general rule, but in some cases, an alternate approach is required. The following is a list of the registers and bits where an alternate approach is required;

- *CodecID_0, CodecID_1:*

These two bits are bits D14 and D15 of registers 28h (Extended Audio ID) and 3Ch (Extended Modem ID). When a read operation of these registers is performed, the returned value is dependent on the status of the SA pin: CodecID_0 reports the status of the SA pin. CodecID_1 always reports 0. Other bits of these registers return the related RAM register contents. Also, note that the status of the SA pin is not readable by the DSP.

- *PR4:*

Bit D12 of register 26h (Power down, ctrl/start) is used to set the AC'97 D_CLK and SDATA_IN signal to a low state. In response to a warm reset the status of this bit is set back to its default 0 value. In response to a read request the actual value of this signal is returned, not the RAM content. Due to this, the RAM register content can be inconsistent.

- *Regs. 2Ch, 2Eh and 30h (Audio Sample Rate Control):*

These three registers are used to setup the sample rate when the Variable Rate Mode is enabled. In response to a read request on one of these registers, the actual value returned can be either BB80h or AC44h, depending on the status of an internal hardware signal. The status of this signal is updated every time a write operation into one of these registers is performed.

Using the *AC97_FC_MODE* configuration bit the interface can be configured in Fully Compliant mode (default). In this mode the value returned as a response to a read operation will be properly masked in order to set 'reserved' bits to 0, per the specification. This operation is performed on all registers including the Standard or Extended Audio address space. If the Full-Compliant mode is not selected the full 16 bits of data from the corresponding RAM register will be returned with no further manipulation.

If an odd-addressed register reading operation is performed, the following scheme is adopted:

- *Slot 0: report valid bit set to 1 for both slot 1 and slot 2*
- *Slot 1 (address): report the odd address*
- *Slot 2 (data): report all 0s*

2.2. Writing AC'97 Registers

When a write operation into one of the available AC'97 registers is performed the entire 16 bit data word is written into the addressed RAM register (also *reserved* bits are passed through). Some bits of some registers may have corresponding *hardware registers (Flip-Flops),* used to control the internal status of the device. In this case, the value of the FF is also updated every time a write to the related RAM register is performed. The status of the FFs are reset to their default values after either a hardware or software reset (writing to reg. 00h) request has been issued; in which case the DSP will also have to reload the RAM register contents.

Some registers have a different behavior from the one depicted above and are summarized below.

- *Regs. 7Ch and 7Eh:*

These are the Vendor ID1 and VendorID2 registers. Any write request to one of these will be ignored.

- *Regs. 28h:*

The 'Extended Audio ID Register' is read only. Therefore, any write request will be ignored.

- *Regs. 26h:*

When a write request is issued the actual data written into the RAM register is "xxxxxxxxxxxx1110', where 'x' represents the incoming data.

- *Regs. 2Ah:*

When a write request is issued the actual data written into the RAM register is 'xxxxxx0111xxxxxx', where 'x' represents the incoming data.

- *Regs. 32h and 34h:*

Any write request into one of these sample rate registers will result in the value BB80h written into the corresponding RAM register.

3. I^2S INPUT INTERFACE CONFIGURATION

To configure the I^2S input interface the *Configuration Register B (CRB)* is used. Using the three I²S1_Align_x bits, one of the seven configuration modes can be selected. Table 2 describes each of them.

Table 2

Mode	# of Slots	W. Length	Alignment	Delay Slot	Notes
0	32	24	Left	No	
1	32	24	Left	Yes	
2	32	16	Right	No	MSB first only
3	32	24	Right	No	
4	24	24	Left	No	Slave only
5	Not Valid	Not Valid	Not Valid	Not Valid	Reserved, do not use
6	24	16	Right	No	MSB first only. Slave only
7	24	24	Right	No	Slave only

Note: By default the standard I²S input interface slave is provided (mode 1 in bits D0, D1, and D2 of register CRB, I2SS_BICK_POL = 1 and I2SI_LRCK_Pol = 0)

3.1. I²S Input switching characteristics (10pF load, Fsm = 32 to 96kHz) (Refer to Figure 3)

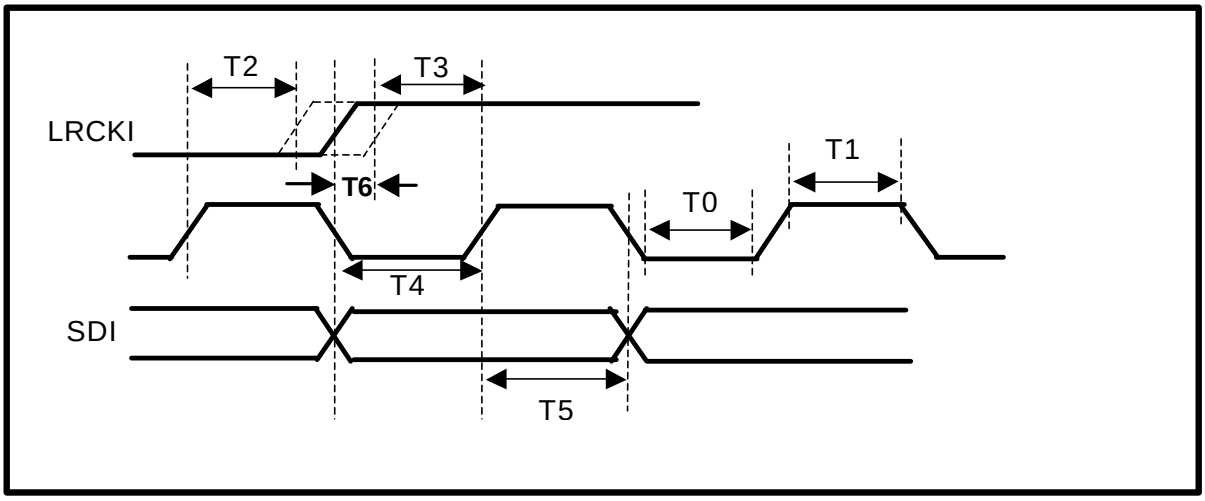


Figure 3. Input Switching Characteristics.

BICKI FREQUENCY (master mode)	3.072MHz
BICKI FREQUENCY (slave mode)	6.4MHz max.
BICKI pulse width low (T0) (slave mode)	40ns min.
BICKI pulse width high (T0) (slave mode)	40ns min.
BICKI active to LRCKI edge delay (T2)	20ns min.
BICKI active to LRCKI edge delay (T3)	20ns min.
SDI valid to BICKI active setup (T4)	20ns min.
BICKI active to SDI hold time (T5)	20ns min.
BICKI falling to LRCKI edge (T6) (master mode)	3ns min.
BICKI falling to LRCKI edge (T6) (master mode)	9ns max.

4. I²S OUTPUT INTERFACE CONFIGURATION

To configure the I²S output interface the *Configuration Register B (CRB)* is used. Using the three I2SO_Align_x bits one of the seven configuration modes can be selected. Table 3 describes each of them.

Table 3

Mode	# of Slots	W. Length	Alignment	Delay Slot	Notes
0	32	24	Left	No	
1	32	24	Left	Yes	
2	32	16	Right	No	MSb first only
3	32	24	Right	No	
4	24	24	Left	No	Slave only
5	Not Valid	Not Valid	Not Valid	Not Valid	Reserved, do not use
6	24	16	Right	No	MSb first only. Slave only
7	24	24	Right	No	Slave only
By default the standard I²S output interface master is provided (mode 1 in bits D8, D9 and D10 of register CRB, I2SO_BICK_Pol = 1 and I2SO_LRCK_Pol = 0 in the same register).					

4.1. I^2S Output switching characteristics (10pF load, Fsm = 48kHz) (Refer to Figure 4.)

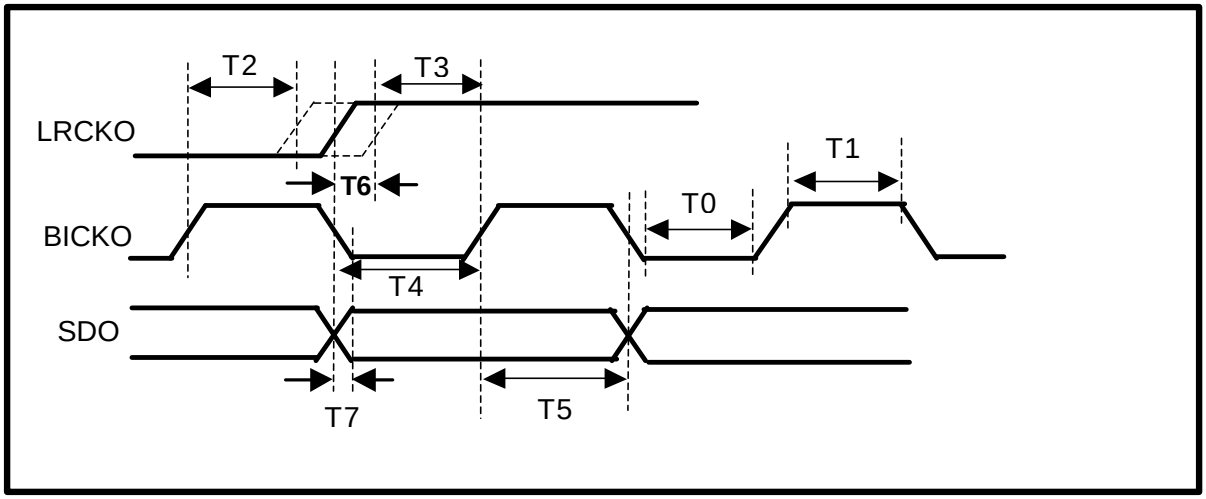


Figure 4. I^2S Output Switching Characteristics.

BICKO Frequency (master mode)	64*Fsm
BICKO Frequency (slave mode)	64*Fsm
BICKO pulse width low (T0) (slave mode)	40ns min.
BICKO pulse width high (T0) (slave mode)	40ns min.
BICKO active to LRCKO edge delay (T2)	20ns min.
BICKO active to LRCKO edge delay (T3)	20ns min.
SDO valid to BICKO active setup (T4)	20ns min.
BICKO active to SDO hold time (T5)	20ns min.
BICKO falling to LRCKO edge (T6) (master mode)	2ns min.
BICKO falling to LRCKO edge (T6) (master mode)	8ns max.
BICKO falling to SDO edge (T7) (master mode)	2ns min.
BICKO falling to SDO edge (T7) (master mode)	8ns max.
BICKO falling to SDO edge (T7) (slave mode)	6ns min.
BICKO falling to SDO edge (T7) (slave mode)	17ns max.

5. SAMPLE RATE CONVERTER (SRC)

The sample rate converter re-samples the selected input data source in order to send to the DSP an audio stream with a fixed frequency of 48 KHz. Figure 5 shows the basic architecture. The threshold selector block makes the selection between a X2 FIR interpolation and direct anti-aliasing filter on the input data automatically. If the input sampling frequency, (measured by DRLL), is higher than the SRC threshold (see Table 12 in section 12.9), the direct initializing filter is selected, otherwise if the input frequency is lower than the SRC threshold, the X2 FIR filter is added to the data path. A 1kHz hysteresis is fixed around the SRC threshold nominal values of Table 12, section 12.9, to prevent unstable settings.

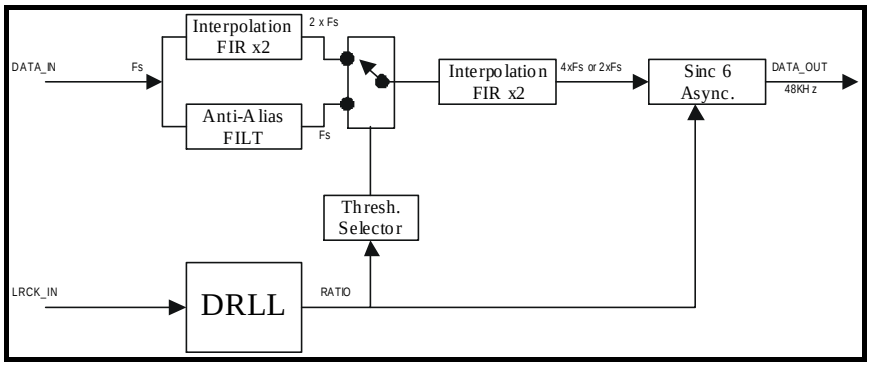


Figure 5. Sample Rate Converter.

6. DIGITAL AUDIO PROCESSOR (DAP) INPUT STAGE

The device provides three mutually exclusive input interfaces: I²S, S/PDIF and AC'97. Their configuration is shown in Figure 6.

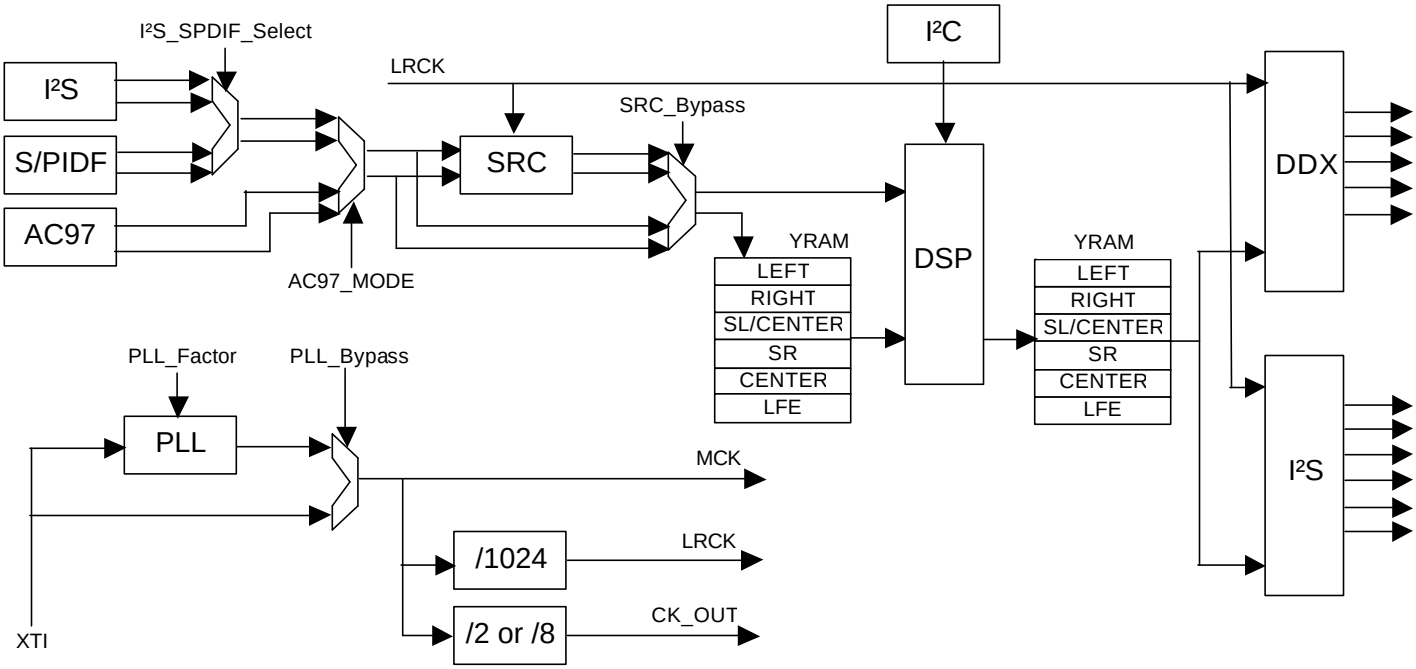


Figure 6. DAP Input Stage.

6.1. INPUT FROM I²S

Using this input interface a maximum of 4 channels can be sent to the DSP. This I/F can be configured as either master or slave. When the master the sampling frequency is fixed to 48 kHz, the SRC can be by passed using the *SRC_Bypass* configuration bit. If slave operation is selected, the full range between 32kHz and 96kHz is supported but the SRC must always be in the processing path (no bypass). In order to select this interface the AC97_MODE pin must be tied to GND and the I2S_SPDIF_Sel must be 0.

The DDX-4100A includes a double-buffering feature to adapt the phase of the incoming serial data to the internal data frame. Double-buffering is enabled by setting Bit D1 in Configuration Register A, address 0x5B. Enabling this function requires that the incoming data rate is exactly equal to the internal data rate, e.g. for a synchronous application using an ADC. If the nominal data input frequency and the internal data frequency are not exactly the same, this function will not properly work and samples will be lost causing performance degradation. It is not recommended to use this feature when the SRC is enabled.

Input Rate : |L0|R0|L1|R1|L2|R2| ...
Output Rate : | | |L0 |R0 |L1 |R1 |L2 |R2 | ...

When using the sample rate converter (SRC), **it is mandatory to apply a valid input signal to the DDX-4100 prior to un-muting.** Failure to do so will result in large DC offsets applied to speaker outputs which may damage loudspeakers. To ensure proper operation using the serial I²S inputs or AC97, valid clock signals must be applied to DDX-4100 pins 3,4 (LRCKI/SYNC, BICKI/BIT_CLK) prior to unmuting. The “SRC Status” bit (register 0x77, bit 0 which determines SRC lock), does not provide a correct indication prior to receiving a valid input signal. The “SRC Status” bit 0 will indicate SRC lock , logic ‘0’, whether or not valid input signals are applied. Subsequent to receiving a valid input signal, the “SRC Status” bit operates as intended, i.e. removing the input signal will cause an out-of-lock indication.

6.2. INPUT FROM S/PDIF

This interface is compliant with the AES/EBU IEC 958, S/PDIF and EIA CP-340/1201 professional and consumer standards. The full range from 32 kHz up to 96 kHz is supported but the SRC bypass option must be switched off. Using the *SPDIF_Mode* bit this interface can be configured as a digital or an analog input. If the analog mode is selected the line receiver can decode differential as well as single ended inputs. The receiver consists of a differential input Schmitt Trigger comparator with 50mV of hysteresis to prevent noise from corrupting the recovered data. The minimum input signal is 200 mV. If the digital mode is selected only single ended operation is supported; the input signal must comply with the input voltage specifications in DC ELECTRICAL CHARACTERISTICS. In order to select this interface the AC97_MODE pin must be tied to GND and the I2S_SPDIF_Sel must be 1.

When using the sample rate converter (SRC), **it is mandatory to apply a valid input signal to the DDX-4100 prior to unmuting.** Failure to do so will result in large DC offsets applied to speaker outputs which may damage loudspeakers. To ensure proper operation using the S/PDIF input, be sure to poll the “S/PDIF Status” bit (register 0x77, bit 1 which determines S/PDIF lock) indicating a valid input signal prior to unmuting. Bit 1 will report logic ‘0’ for a valid S/PDIF input signal or logic ‘1’ for an invalid signal. Delay unmuting until after a valid signal is detected.

6.3. INPUT FROM AC'97

To select this interface the AC97_MODE pin must be tied to VDD (I2S_SPDIF_Sel is don't care). The AC'97 interface can be configured either as the primary or secondary device using the external configuration pin SA. This interface supports four discrete sampling frequencies, according to the Variable and Double Rate Audio Codec '97 specification. Table 4 summarizes the slot usage for each one of these frequencies and Table 5 summarizes the different input configurations

Table 4. Slot Usage

Freq.	Slot 3	Slot4	Slot 6	Slot 7	Slot 8	Slot 9	Slot 10	Slot 11	Slot 12
48	Left	Right	Center	Surr.L	Surr.R	LFE			
44.1	Left	Right		Surr.L	Surr.R				
88.2*	Left	Right	Center				Left (n+1)	Right (n +1)	Center (n+1)
96	Left	Right	Center				Left (n+1)	Right (n+1)	Center (n+1)

**Slots 3, 4 and 6 are always requested. Slots 10, 11, and 12 are requested only when needed*

Table 5. Input Configurations

Input from	Channels	Available Freq. (KHz)	Bypass	Notes
I²S (Master)	4	48	Yes	Bypass is user selectable
I²S (Slave)	4	32..96	No	
S/PDIF	2	32..96	No	
AC'97	6	48	Yes*	Left, Right, SL, SR, Center, LFE
AC'97	3	96	No	Left, Right, Center
AC'97	4	44.1 (VRA)	No	Left, Right, SL, SR
AC'97	3	88.2 (VRA)	No	Left, Right, Center

**In this configuration the BYPASS is always active, regardless of the state (status) of SRC_Bypass bit in reg. 5Ah*

7. PHASE LOCKED LOOP (PLL)

To generate the required internal 49.152 MHz clock a low-jitter PLL has been included in the device. It must be configured to work with a multiplication factor of X2, in order to fit an external frequency reference of 24.576 MHz. Using *PLL_Bypass* bit the PLL section can be bypassed, allowing direct connection of the internal clock to the XTI pin. When this option is selected, the PLL is automatically powered-down and an external frequency of 49.152 MHz needs to be provided to the device.

8. POWER DOWN MANAGEMENT

The power down capability and its logic behavior is shown in Figure 7. There are three power-down requests that are external to the device that will cause a power down condition:

- *External PWDN pin –*

This signal will turn-off the device, which will enter the power down mode (all the device clocks are stopped). The device will exit this state as soon as the PWDN pin is de-asserted.

- *PR5 bit (reg. 26h, bit D13) –*

Setting this bit will cause a partial power down of the device, with all the clocks suspended except those that are required to keep the AC97 and I²C cells alive. In this way, using either of these input interfaces makes it possible to resume from this state simply by resetting the PR5 bit.

- *EAPD bit (reg. 26h, bit D15) –*

The External Amplifier Power Down bit controls the state of the related pin (EAPD), which in turn, is used to switch off the external power device.

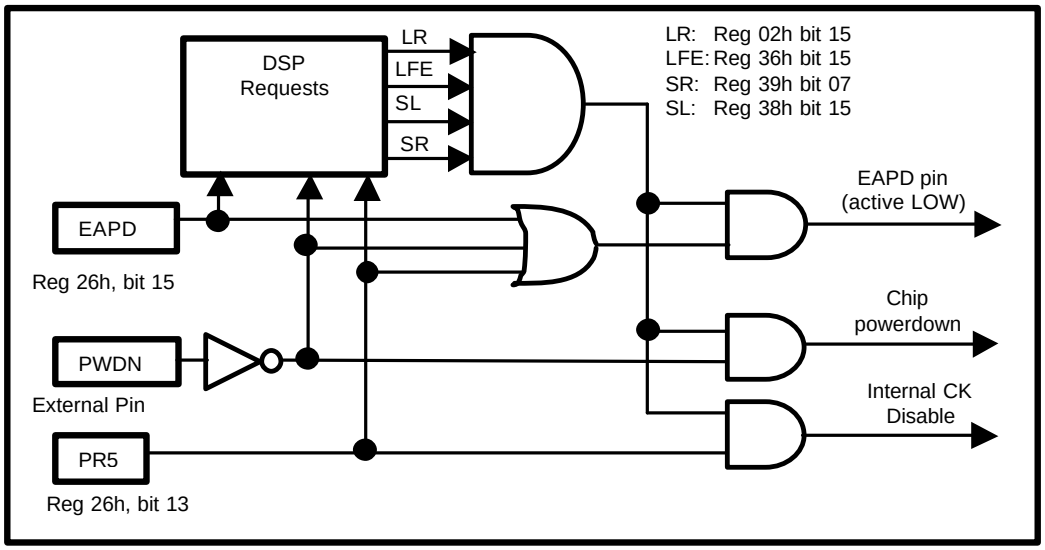


Figure 7. Power Down Management.

To avoid any extraneous noise while switching between the various power-down modes, a masking technique has been adopted to drive the actual controlling signals. As shown in Figure 7, a power-down request will instruct the DSP to perform a volume fade-out and MUTE of all channels (soft-mute). The external power device will also be turned off (via the EAPD pin) not only as a consequence of an EAPD request, but also as a consequence of a PR5 or PWDN request, preventing any possible noise.

9. BASS MANAGEMENT AND EQ

The DDX-4100A has the ability to redirect sound to the SBW,(subwoofer), channel and to pass each channel through a 4 stage cascaded 2nd order IIR filter. With the combination of the DDX gain/compressor (CRA register bits 2-3) a dynamic EQ can be implemented. Additionally, a special Side-Firing sound can be achieved by enabling this feature available with the ready-made filter topology on the surround channels.

9.1. Bass Redirection

There is an option to redirect each input channel to the SBW output channel. The scaling factor of each channel can be set with values between 0 (no redirection) to – 1 (full redirection). See Section 10 for more information about setting the scaling factor registers. This redirection takes place when bit D0 of the Bass Management Register (add. 72h) is set (see section 12.12).

Together with the static EQ option, described in the following section, and by setting the appropriate filters, a full bass management solution is available. Note that C and LFE channels are available only with six channel AC97 input. Four channel I²S INPUT has only L, R, LS and RS. Two channel S/PDIF input has only L and R.

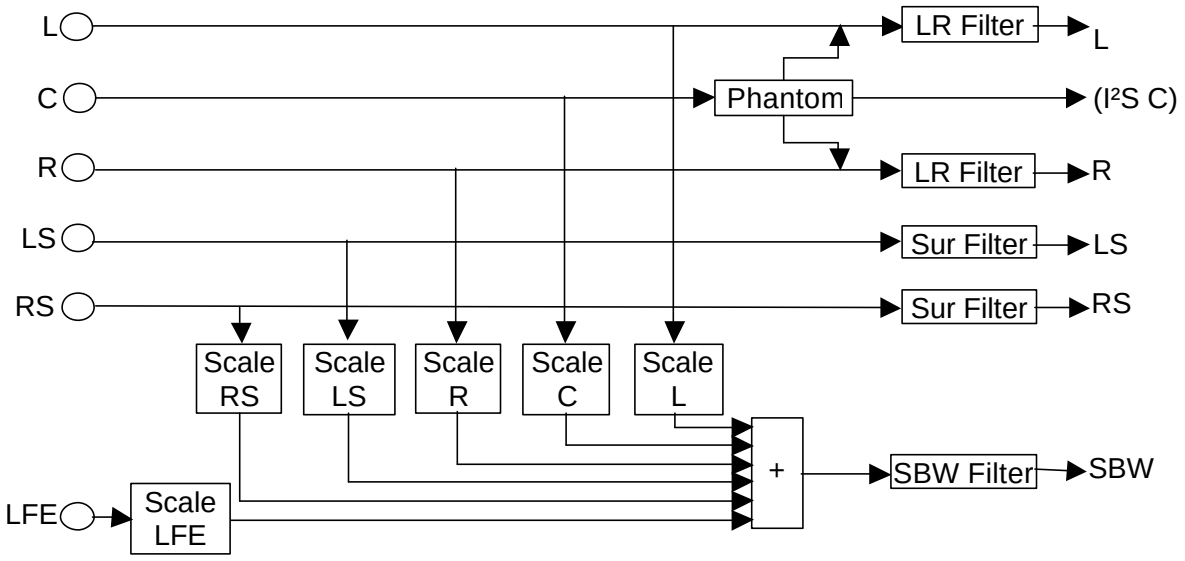


Figure 8. Bass Redirection

9.2. Static EQ

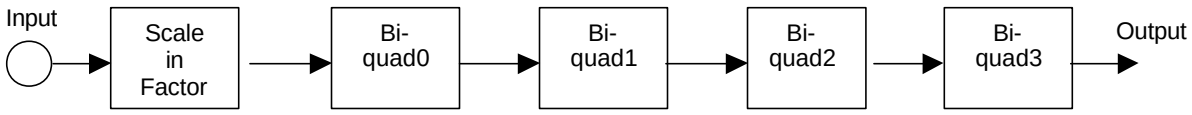


Figure 9. Static EQ Biquads

Each channel has a 4-stage cascaded filter of 2nd order bi-quad sections. Each filter's coefficients are user definable (see Section 10). The coefficients for the Left and Right channels are common, as are the coefficients for the surrounds. There is also an input-scaling factor for each channel, which can be set with values from 0 to –1. The scaling factor must be set to an appropriate value to prevent the filters from saturating.

The Static EQ filters are activated by the Static EQ and Side Firing registers (address 70h, see Section 12.11).

9.3. Surround Side Firing

Instead of the normal filters described in the previous section above, a special topology is available for the surround channels:

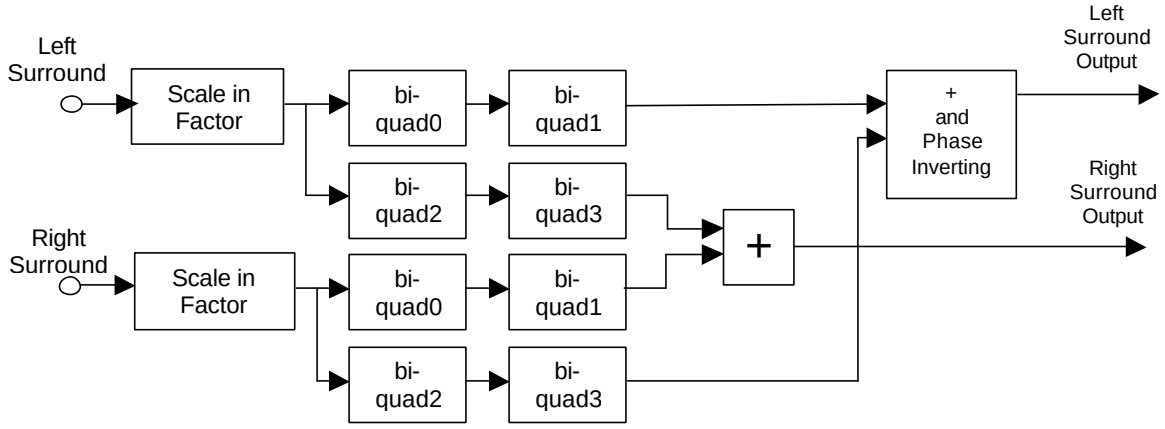


Figure 10. Side Firing connections for Surround channels.

By designing appropriate filters, special surround sound can be achieved where surround speakers are located next to the front speakers and rotated to the sides. By setting Static EQ and Side Firing (address 70h, Section 12.11), this Side Firing topology is enabled.

10. EQ AND BASS MANAGEMENT COEFFICIENT HANDLING

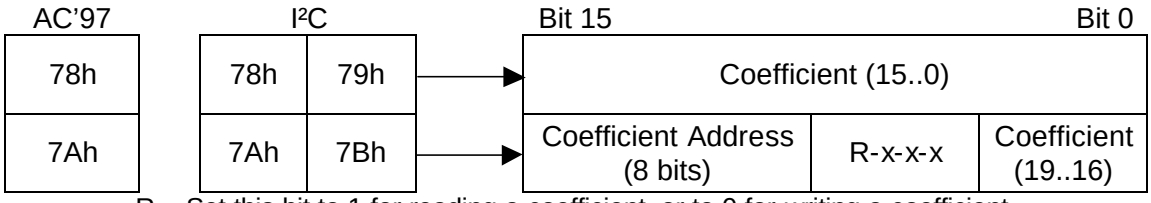
In order to implement the Static EQ filters and the Bass management, a RAM space for user coefficients has been included in this device. Beginning with address 240h (YRAM), there are 69 x 20 bit registers available for this purpose.

IMPORTANT: All outputs MUST be Soft-Muted (see section 8) before changing any of these coefficients.

To read or write into these registers the application software must follow an indirect addressing approach. As shown in there are two AC'97 dedicated registers, (4 x 8 bit registers for I²C addressing), to access the coefficient table. In register 78h (78h + 79h in I²C addressing) the 16 low bits of the coefficient are stored either by the user for a write operation, or by the internal logic for a read operation. The upper 4 bits are stored in the lowest nibble of register 7Ah (7Bh in I²C addressing). The address of the coefficient on which the R/W operation must be performed is stored in the high byte of register 7Ah. The address is derived by adding the coefficient index to the base location 40h.

To select between Read or Write operation the 'R' bit in register 7Ah (7Bh in I²C addressing) must be properly setup. The actual read/write operation will start after register 7Ah (7Bh in I²C addressing) has been written. The following explains this in more detail:

Table 6. Coefficient registers usage.



R = Set this bit to 1 for reading a coefficient, or to 0 for writing a coefficient.

10.1. Reading a Coefficient Value

Depending on the bus used to read the coefficient, the following steps must be executed:

- *Reading from AC'97*
  - *Write 8 bit INDEX 40h and R/W bit at AC'97 address 7Ah*
  - *Read 16 lower data bits at AC'97 address 78h*
  - *Read 4 upper data bits at AC'97 address 7Ah*
- *Reading From I²C*
  - *Write 8 bit address at I²C address 7Ah coefficient INDEX + 40h*
  - *Write R/W bit at I²C address 7Bh*
  - *Read 8 middle data bits at I²C address 78h*
  - *Read 8 lower data bits at I²C address 79h*
  - *Read 4 upper data bits at I²C address 7Bh*

10.2. Writing a Coefficient Value

Depending on the bus used to write the coefficient, the following steps must be followed:

- *Writing from AC'97*
  - *Write 16 lower bit data at AC'97 address 78h*
  - *Write 8 bit INDEX 40h and R/W bit and 4 upper data bits at AC'97 address 7Ah*
- *Writing from I²C*
  - *Write 8 middle data bits at I²C address 78h*
  - *Write 8 lower data bits at I²C address 79h*
  - *Write 8 bit address at I²C address 7Ah coeff INDEX +40h*
  - *Write 4 upper data bits and R/W bit at I²C address 7Bh*

10.3. Coefficient Map

Table 7

Index (decimal)	Index (hex)		Coefficient	Default Value
0	0h	20 LR Filter Coef	LR00(b2)	00000h
1	1h		LR01(b0-1)	00000h
***	***		****	***
4	4h		LR04 (b1/2)	00000h
5	5h		LR10(b2)	00000h
***	***		***	***
19	13h		LR34(b1/2)	00000h
20	14h	20 Surrounds filter coef	SUR00	00000h
***	***		***	***
39	27h		SUR34	00000h
40	28h	20 SBW filter coef	SBW00(b2)	00032h
41	29h		SBW01(b0-1)	80032h
42	2Ah		SBW02(a2)	7C7Eah
43	2bh		SBW03(a1/2)	81C6Fh
44	2Ch		SBW04(b1/2)	00032h
45	2dh		SBW10	00000h
***	***		***	***
59	3bh		SBW34	00000h

10.3 Coefficient Map (*Table 7 Continued*)

60	3Ch	3 scale in factors	-scale_in LR	80000h
61	3dh		-scale in SUR	80000h
62	3Eh		-scale in SBW	80000h
63	3Fh	6 SBW redirection factors	-scale_L – SBW	C0000h
64	40h		-scale_R – SBW	C0000h
65	41h		-scale_LS – SBW	C0000h
66	42h		-scale_RS – SBW	C0000h
67	43h		-scale_C – SBW	C0000h
68	44h		-scale_LFE – SBW	80000h

Filter coefficients:
CHx0 = b2
CHx1 = (b0)-1
CHx2 = a2
CHx3 = (a1)/2
CHx4 = (b1)/2

Where the CH stands for LR, SUR or SBW and x stands for the filter number (0 thru 3).

The filter equation is:

$$Y_n = X_n+((b0)-1)* X_n + 2 *((b1)/2) *X_{n-1} + b2 *X_{n-2} – 2 * ((a1)/2) *Y_{n-1} – a2 *Y_{n-2}$$

which becomes:

$$Y_n = b0 *X_n + b1 *X_{n-1} + b2 *X_{n-2} – a1 *Y_{n-1} – a2 *Y_{n-2}$$ *Equation 1*

The coefficient registers are 20 bits wide and should be in the range (-1 to 1) (80000h to 7fffffh).

Scaling factor registers:

- *For the filters Xn = - (-scale_in) *CHn, where CHn is the value before scaling and Xn is the input to the filter.*
- *For the SBW redirection SBWn = S (-scale_CH) *CHn*
- *The scaling factor registers are 20 bits wide and should be in the range (-1 to 0) (80000h to 000000h).*
- *SBW redirection: - 1 for maximum redirection and 0 for no redirection.*
- *Filter scaling: -1 for maximum input and 0 for no input to filter.*

11. I²C BUS SPECIFICATION

The DDX-4100A supports the I²C protocol. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The DDX-4100A is always a slave device in all of its communications.

16-bit registers are addressed as two 8-bit registers. The high byte has an even address, while the low byte has an odd address. For example, reading from register 02 (16-bit) means read register 02 (High Byte) and 03 (Low Byte) for I²C.

11.1. COMMUNICATION PROTOCOL

11.1.1. Data Transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

11.1.2. Start Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

11.1.3. Stop Condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between DDX-4100A and the bus master.

11.1.4. Data Input

During the data input the DDX-4100A samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

11.2. DEVICE ADDRESSING

To start communication between the master and the DDX-4100A, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I2C bus definition. In the DDX-4100A the I2C interface has two device addresses depending on the SA pin configuration, 0011110 when SA = 0, and 0011111 when SA = 1.

The 8th bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the DDX-4100A identifies on the bus the device address and if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

11.3. WRITE OPERATION (see Figure 11)

Following the START condition the master sends a device select code with the RW bit set to 0. The DDX-4100A acknowledges this and the writes for the byte of internal address. After receiving the internal byte address the DDX-4100A again responds with an acknowledgement.

11.3.1. Byte Write

In the byte write mode the master sends one data byte, this is acknowledged by the DDX-4100A. The master then terminates the transfer by generating a STOP condition.

11.3.2. Multi-byte Write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

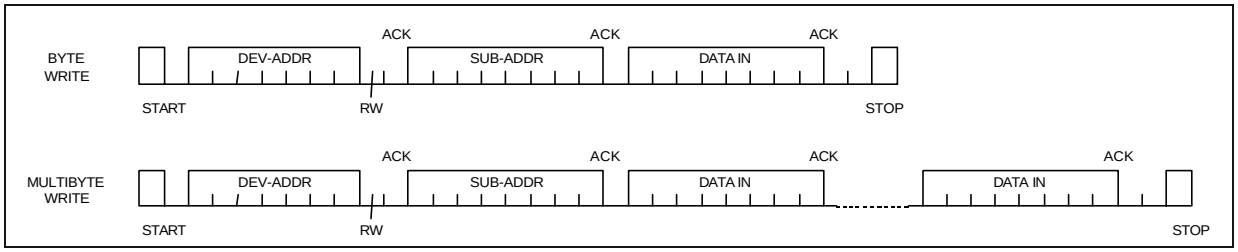


Figure 11. Write Mode Sequence.

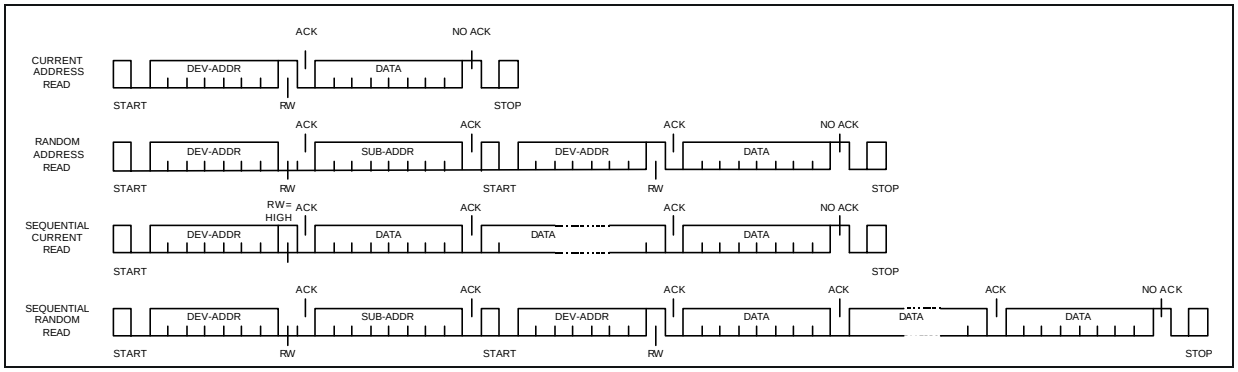


Figure 12. Read Mode Sequence.

11.4. ADDRESSING MULTIPLE DDX-4100A DEVICES

When using the DDX-4100A in dual processor configuration, **there is an operational error when using the combination of I2C address = 0011 111x (SA {pin 11} connected to Vdd) and serial I2S input SDI1 (pin 1).** The serial data input SDI1 will not operate properly in this configuration. Using I2C address = 0011 110x (SA {pin 11} connected to ground, both SDI1,2 inputs operate properly. Single processor configurations are not affected by this error, provided the SA pin is connected to ground. There are two choices for a corrective action.

The first choice is to ground SA (pin 11) on both ICs, causing both ICs to have the same I²C address = 0011 110x, and use two separate I²C Clock pins (SCL pin 10) from the system microcontroller, one for each IC, to address the two processors independently. When communicating with the first processor, the SCL signal connected to the second must remain static and vice versa. The advantage is that full functionality is achieved and no other changes are required. The disadvantage is that there is an additional signal required from the system microcontroller.

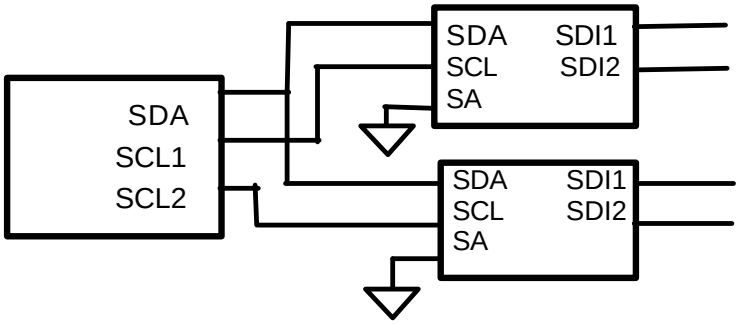


Figure 13. First Choice: Ground SA on both controllers

The second choice is to ground the SDI1 pin (pin 1) on the DDX-4100 when the SA pin (pin 11) is connected to V_{DD}. This means that you cannot use this input disabling L and R outputs on this device and so only the LS and RS surround outputs will be available.

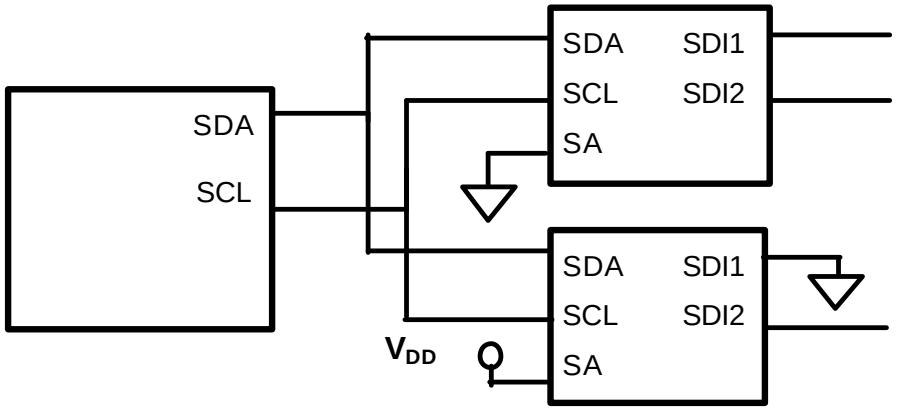


Figure 14. Second Choice: Ground SA on one controller.

12. REGISTER SUMMARY

12.1. Reset Register (address 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns 00E4h as it is the ID code of the part and it's 3D Stereo Enhancement type (see AC'97 revision 2.1 specification, Section 6.3.1).

12.2. LR Volume Register (address 02h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	ML6	ML5	ML4	ML3	ML2	ML1	ML0	X	MR6	MR5	MR4	MR4	MR2	MR1	MR0

This register manages the stereo (both right and left channels) output signal volume. The MSB of the register is the mute bit. ML6 through ML0 set the left channel level, MR6 though MR0 set the right channel. There are two options: 'Full Compliance' operating mode (bit D0 in the CRA register, address 5Ah, is set to '0') only 6 bits are active (Mx0 to Mx5) and each step corresponds to 1.5dB. In 'Proprietary" mode (bit D1 in the CRA register is set to '1'), Mx0 to Mx6 can have the values between 0h to 68h (110 1000) and each step corresponds to 1dB. Greater values are undefined.

The default value is 8000h (1000 0000 0000 0000), which corresponds to 0dB attenuation.

Mute	Mx6 – Mx0	Function
0	X00 0000	0 dB Attenuation
0	X01 1111	46.5dB Attenuation
0	X11 1111	94.5dB Attenuation
1	xxx xxxx	∞dB Attenuation

Table 8. Full Compliance Mode

Mute	Mx6 – Mx0	Function
0	000 0000	0 dB Attenuation
0	001 1111	31 dB Attenuation
0	011 1111	63 dB Attenuation
	***	***
0	110 0001	97 dB Attenuation
0	110 0010	99 dB Attenuation
0	110 0011	100 dB Attenuation
0	110 0100	102 dB Attenuation
0	110 0101	104 dB Attenuation
0	110 0110	107 dB Attenuation
0	110 0111	111 dB Attenuation
0	110 1000	∞ dB Attenuation
1	xxx xxxx	∞ db Attenuation

Table 9. Proprietary Mode.

12.3. Tone Control Register (address 08h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	BA3	BA2	BA1	BA0	X	X	X	X	TR3	TR2	TR1	TR0

This register supports tone controls (bass and treble). Writing a 0000h corresponds to +12dB of gain. The frequencies (from which gains are measured) are 160Hz for Bass and 5,000Hz for Treble. The default value is 0F0Fh, which corresponds to bass and treble bypass. The tone feature is implemented only on the L and R front channel. Tone Control contour curves are shown in Figure 15.

TR3… TR0 or BA3… BA0	Function
0000	+12dB of gain
0001	+10dB of gain
0010	+8dB of gain
0011	+6 dB of gain
0100	+4dB of gain
0101	+2 dB of gain
0110	+1dB of gain
0111	0dB of gain
1000	-1dB of gain
1001	-2dB of gain
1010	-4dB of gain
1011	-6dB of gain
1100	-8dB of gain
1101	-10dB of gain
1110	-12dB of gain
1111	Bypass

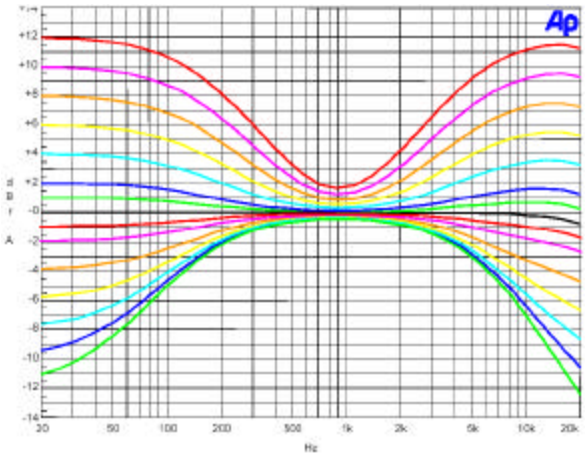


Figure 15. Tone Control Contour Curves.

The tone control in the DDX-4100A is implemented in such a manner that boosting can create clipping of the audio regardless of the volume setting. This is because the Bass/Treble boost occurs before the volume control. Meaning, for example, if the bass boost is set at +8dB then any low-frequency program material recorded above –8 dB FS will clip within the bass boost processing. Implementing attenuation prior to the DDX-4100A can solve this problem. Many audio decoding ICs provide a volume control that can accomplish this. An attenuation of –12 dB should be implemented in the decoding IC. Therefore no clipping will take place in either the bass or treble boost regardless of the setting. Volume is controlled normally using the DDX-4100A, except when maximum DDX-4100A volume(0 dB) is reached. The attenuation in the decoder IC will then have to be decreased from –12 dB to 0 dB in the appropriate volume step size to obtain maximum gain through the system. This implementation will only create signal clipping once maximum output has been reached. Therefore it will clip like any other amplifier regardless of the bass/treble settings.

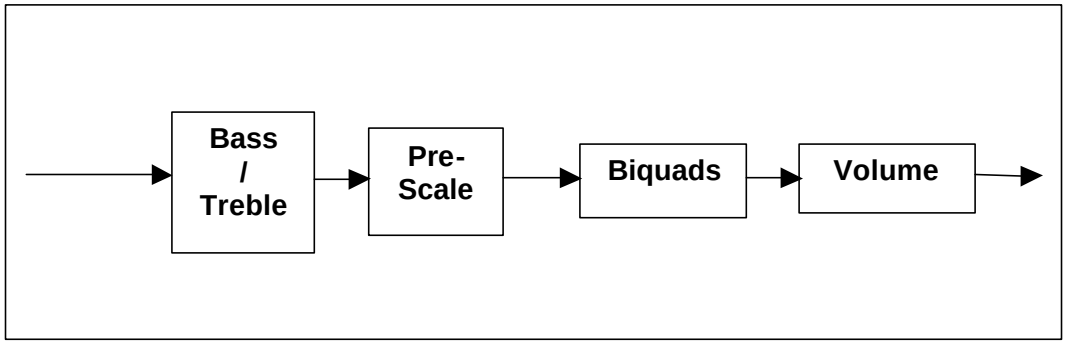


Figure 16. Digital Audio Signal Flow.

12.4. Power-down Ctrl/Status Register (PCSR) (address 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EAPD		PR5	PR4									1	1	1	0

BIT	R/W	RST	NAME	DESCRIPTION
D12	R/W	0	PR4	Setting this bit to 1 the BIT_Clk and the SDATA_IN signal will be fixed to the digital low level. To resume the normal operation either a hardware reset or a *softReset* must be performed.
D13	R/W	0	PR5	In order to set the device in a power-down-like condition this bit must be set to 1. This will stop the device internal clock: only the PL and AC'97, I^2C clocks will still be running. The DSP starts the power-down sequence (volume fade-out and MUTE).
D15	R/W	1	EAPD	The value of this bit is checked by the DSP in order to recognize an external power amplifier power-down request. As a consequence the DSP starts the power-down sequence (volume fade-out and MUTE).

NOTE: Bit D0, D3 will be masked to show the value before writing into the RAM register, other bits will simply pass through.

12.5. Extended Audio ID Register (address 28h) AC'97 Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ID0	0	0	0	0	0	1	1	1	0	0	0	0	1	1

The Extended Audio ID is a read-only register that identifies which extended audio features are supported (see AC'97 revision 2.1 specification, Section A2.1). The extended features supported are Variable Rate PCM Audio (VRA), Double rate PCM Audio (DRA), PCM Center (CDAC), PCM Surround (SDAC) and PCM LFE (LDAC).

Code ID0, at D14, reports the status of the SA pin. Code ID1, at D15, always reports 0. Hence, the configurations are primary (00) if SA pin is 0 or Secondary (01) if SA pin is 1.

12.6. Extended Audio Status and Control Register (address 2Ah) AC'97 Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						0	1	1	1					DRA	VRA

VRA = 1 enables Variable Rate Audio mode (sample rate control register and SLOTREQ signaling)
DRA = 1 enables Double Rate Audio mode

Bits D9 – D6 are read only status of the extended audio feature readiness. When a write request is issued the actual data written into the RAM register is 'xxxxxx0111xxxxxx'.
For more details refer to AC'97 rev 2.1, section A2.2

12.7. Audio Sample Rate Control Registers (address 2Ch – 34h) AC'97 Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

In VRA mode, two frequencies are supported 48.0 kHz (BB80h) and 44.1 kHz (AC44h). If one of these values is written to the 2Ch register, that value will be echoed back when read, otherwise the closest (higher in case of a tie) sample rate supported is returned. The content of the 2Eh and 30h register is copied from the 2Ch register.

If the Double Rate Audio (DRA) mode is active, the sample rate programmed will be multiplied by 2x. For example: When running at 88.2KHz, the DRA bit will be programmed to 1, and the sample rate programmed would be 44.100KHz.

The default value after a cold or warm register reset for these registers is 48kHz, (BB80h). The content of the sample rate register (32h and 34h) stays always at BB80h.

12.8. 6-Channel Volume Control Register (address 36h – 38h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	LFE6	LFE5	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
Mute	LSR6	LSR5	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

These read/write registers control the output volume of the optional six I^2S PCM channels, and values written to the fields behave the same as the Play Master Volume Register (Index 02h), which offers attenuation but no gain. There is an independent mute (1=on) for each channel. Note, center channel volume applies to AC97 input only.

The default value after reset for this register (8080h) corresponds to 0dB attenuation with mute on.

12.9. Configuration Register A (CRA): address 5Ah

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SRC_ By Pass	DRLL _dBg	SRC_ THR_ 1	SRC_ THR_ 0	SPDI F_ Mode	I2S_ SPDI F_Set	MCK OUT_ Mode	PLL_ By Pass	PLL_ Factor	DDX_ PWr Mode	DDX_ ZDEn able	DDX_ Rst	DDX Gain_ 1	DDX Gain_ 0	I2SI Dbuff Mode	AC97 FC Mode

Table 10

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	0	AC97_FC_Mode	AC'97 Full Compliant Mode (0 to enable). When in FC mode any read of registers will return only valid bits: bits marked as 'reserved' by AC'97 v2.0 specification will return 0, regardless of the RAM contents.
D1	R/W	0	I2SI_DBUFF_Mode	Enable Double Buffer mode for the I^2S input interface (write 1 to enable this option). This is recommended ONLY if this interface is operated in SYNC mode (SRC bypassed).
D2	R/W	0	DDX_Gain_0	DDX Gain setting (LSb/MSb). These two bits will set the DDX stage gain and the compression as shown in Table 11. This setting is active ONLY if the DDX Gain Register (Addr. 62h) bit D15 is 0.
D3	R/W	0	DDX_Gain_1	
D4	R/W	1	DDX_Rst	DDX Reset (active high)
D5	R/W	1	DDX_ZD_Enable	DDX Zero Detect Feature. If this bit is 1 the feature is enabled.
D6	R/W	1	DDX_PwrMode	DDX Power Mode. (1 = Fixed for DDX-2060).
D7	R/W	0	PLL_Factor	PLL factor . Always write a '0' to this bit. '0' (x2) using 24.576MHz crystal or clock input.
D8	R/W	1	PLL_Bypass	PLL Bypass. Setting this bit to 0 will bypass the PLL; internal master clock will be directly connected to XTI pin.
D9	R/W	0	MCKOUT_Mode	MCKOut Mode: 12.288 MHz (1) or 24.576MHz (0).
D10	R/W	0	I2S_SPDIF_Sel	I^2S – S/PDIF Selector. Select the input source: set to 0 for I^2S input, 1 for S/PDIF input.
D11	R/W	0	SPDIF_Mode	S/PDIF Mode. Set to 0 to select Analog mode, 1 to select Digital mode.
D12	R/W	1	SRC_THR_0	Sample Rate threshold (LSb/MSb). These bits are used to select the threshold frequency enabling the SRC anti-alias filter. Table 12 shows the threshold selections.
D13	R/W	0	SRC_THR_1	
D14	R/W	0	DRLL_dbg	DRLL Debug Mode. This bit is used for a test mode. Set to 0 for normal operation.
D15	R/W	0	SRC_Bypass	SRC Bypass. Setting this bit to 1 the SRC block can be bypassed and the selected input I/F is directly connected to the DSP.

Note: In TEST_MODE – PLL_Bypass = 0

DDX_GAIN_0	DDX_GAIN_1	DDX Gain	DDX Compression
0	0	1x	NO
0	1	2x	NO
1	0	2x	YES
1	1	3	YES

Table 11. DDX Gain

DDX Gain Compression

Since a full-scale output of the GC/Vol block is mapped to full output modulation, any signal exceeding 0 dB FS at the output of the GC/Vol block will clip. The purpose of the compression algorithm is to reduce the gain of the system when 0 dB FS has been exceeded. This eliminates clipping, thus performing an output limiting function. This yields constant output once the gained input exceeds 0 dB FS.

With DDX_GAIN_0 set to 1, the output of the GC/Vol block is compared to a threshold set just below 0 dB FS. When the GC/Vol exceeds this threshold the system gain is reduced following a set time constant at a set gain reduction rate. The gain reduction is stored as a variable. If the subsequent output of GC/Vol remains below a lower threshold for a set time, the gain is increased following another set time, at a set gain rate. Thus, seven constants determine the attack, release and limiting characteristics of the compression algorithm. These constants have been tuned for the lowest perceived audio distortion when reducing the dynamic range of a recording due to 0dB FS being exceeded.

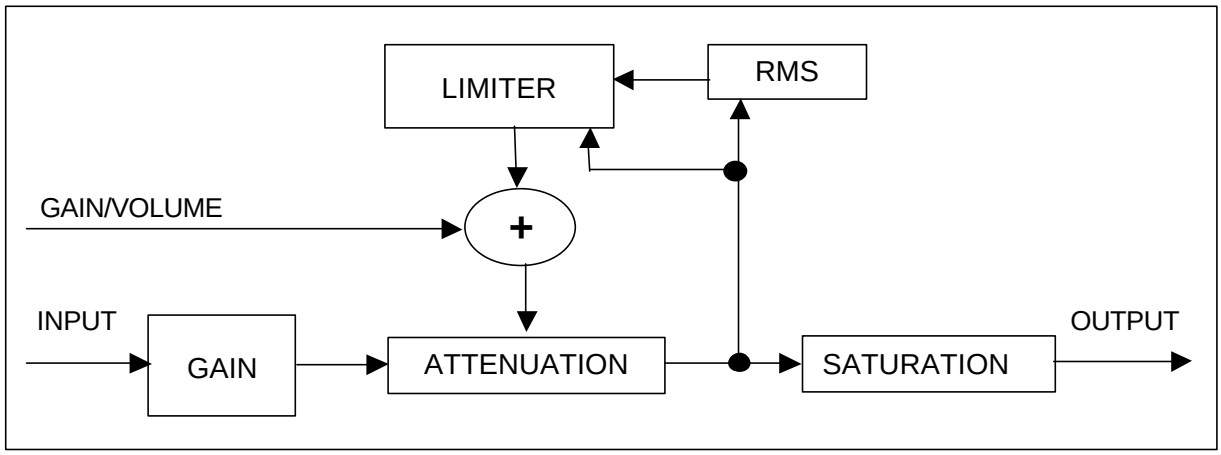


Figure 17. Gain Limiter.

SRC_THR_0	SRC_THR_1	Threshold Frequency
0	0	INACTIVE
0	1	58.875 to 61.125kHz
1	0	78.973 to 81.000kHz
1	1	Always active

Table 12. SRC Threshold

12.10. Configuration Register B (CRB) (address 5Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
I2SO_MSb LSb	I2SO_LRCK_Master	I2SO_LRCK_Pol	I2SO_BCK_Master	I2SO_BICK_Pol	I2SO_Align_2	I2SO_Align_1	I2SO_Align_0	I2SI_MSb LSb	I2SI_LRCK_Master	I2SI_LRCL_Pol	I2SI_BCK_Master	I2SI_BICK_Pol	I2SI_Align_2	I2SI_Align_1	I2SI_Align_0

Table 13

BIT	R/W	RST	NAME	DESCRIPTION
D0	R/W	1	I2SI_Align _0	I^2S (Input) Alignment. Using these bits the word alignment can be adjusted with respect to the LRCK edges. Please refer to the related paragraph for more details. The default value is mode 1. (See Table 2)
D1	R/W	0	I2SI_Align_1	
D2	R/W	0	I2SI_Align_2	
D3	R/W	1	I2SI_BICK_Pol	I^2S (Input) BICK Polarity. This bit should be configured according to the serial protocol used. In order to sample incoming data on the rising edge (data changes on the falling edge) this bit should be set to 1. Set to 0 to reverse the sampling edge.
D4	R/W	0	I2SI_BCK_Master	I^2S (Input) Master/Slave Selection. The I^2S input interface can be configured as either master or slave: if the master mode is selected (1) the BICK line will be an output (64 x 48KHz fixed). Otherwise (0) slave mode is selected and this line is an input.
D5	R/W	0	I2SI_LRCK_Pol	I^2S (Input) LRCK Polarity. Set to 0 to receive LEFT samples when LRCK is low, 1 otherwise
D6	R/W	0	I2SI_LRCK_Master	I^2S (Input) Master/Slave Selection. The I^2S input interface can be configured as either master or slave: if the master mode is selected (1) the LRCK line will be an output (48KHz fixed). Otherwise (0) slave mode is selected and this line is an input (continuous frequency between 32KHz and 96KHz).
D7	R/W	1	I2SO_MSbLSb	I^2S (Input) MSb/LSb Selection. Use this bit to select how the sample word is received by the I^2S input interface: set to 0 to configure as LSb first, 1 MSb first.
D8	R/W	1	I2SO_Align_0	I^2S (Output) Alignment. Using these bits the word alignment can be adjusted with respect to the LRCK edges. The default value is mode 1. (See Table 3)
D9	R/W	0	I2SO_Align_1	
D10	R/W	0	I2SO_Align_2	
D11	R/W	1	I2SO_BICK_Pol	I^2S (Output) BICK Polarity. This bit should be configured according to the used serial protocol. In order to sample out coming data on the rising edge (data changes on the falling edge) this bit should be set to 1. Set to 0 to reverse the sampling edge.
D12	R/W	1	I2SO_BCK_Master	I^2S (Output) Master/Slave Selection. The I^2S output interface can be configured as either master or slave: if the master mode is selected (1) the BICK line will be an output (64 x 48kHz). Otherwise (0) slave mode is selected and this line is an input.
D13	R/W	0	I2SO_LRCK_Pol	I^2S (Output) LRCK Polarity. Set to 0 to transmit LEFT samples when LRCK is low, 1 otherwise.
D14	R/W	1	I2SO_LRCK_Master	I^2S (Output) Master/Slave Selection. The I^2S output interface can be configured as either master or slave: if the master mode is selected (1) the LRCK line will be an output. Otherwise (0) slave mode is selected and this line is an input. In any case the frequency is fixed at 48kHz
D15	R/W	1	I2SO_MSbLSB	I^2S (Output) MSb/LSb Selection. Use this bit to select how the sample word is transmitted by the I^2S output interface: set to 0 to configure as LSb first 1, MSb first.

NOTE: Power-on default values will configure serial input interface as I^2S Slave and the output interface as I^2S Master.

12.11. Phantom Center Register (address 60h) (AC'97 only)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															Phantom

Setting bit D0=1 enables the Phantom Center Channel in AC'97 operation. When enabled, the content of the center channel is split and added to the L and R channels. Default setting is 0h.

12.12. DDX Gain Register (address 62h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bypass	GCEN	VOL4	VOL3	VOL2	VOL1	VOL0	X	X	X	X	X	X	X	X	X

bypass: 0: DDX gain determined by CRA Bits D2 and D3
1: DDX gain determined by DDX Gain Register bits D9 – D13

GCEN: 0: Disable Gain Compression (see section 12.9; CRA)
1: Enable Gain Compression

VOL4 … VOL0	dB Gain
00000	23.5
00001	22.5
00010	21.75
…	…
01111	12
10000	11.25
…	…
11101	1.5
11110	0.75
11111	0

DDX gain is variable from 0dB to 23.25dB in 0.75 steps.

12.13. Static EQ and Side Firing Register (address 70h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														EQ1	EQ0

This register controls the activation of the Static EQ and the Side Firing surround sound.

EQ1	EQ0	Result
0	0	EQ off (default)
0	1	EQ enabled
1	x	Side Firing + EQ

For more information on setting EQ parameters, see Section 9.2.

12.14. Bass Management Register (address 72h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															Bass Manage-ment

Setting bit D0=1 activates the Bass Management. For more information on Bass Management, see section 9.1. Default setting is 0h.

12.15. Bypass Register (address 74h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															Bypass

Setting bit D0=1 bypasses the DSP block. All channels are bypassed and output equal to input, regardless of all other algorithm register settings (Volume, Tone, Phantom, EQ). Default is 0h.

12.16. BIST and Status Register (BASR): (address 76h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DSP_ BIST_ START	DSP_ BIST_ RUN NING	DSP_ BIST_ STOP	DSP_ RAM	X	X	SRC_ SPRAM _2	SRC_ SPRAM _1	DDX_ DPRAM	DDX_ SPRAM _3	DDX_ SPRAM _2	DDX_ SPRAM _1	BIST_ STOP	BIST _START	SPDIF_ STATUS	SRC_ STATUS

NOTE: The "SRC Status" bit (register 0x77, bit 0 which determines SRC lock), does not provide a correct indication prior to receiving a valid input signal. The "SRC Status" bit 0 will indicate SRC lock , logic '0', whether or not valid input signals are applied. Subsequent to receiving a valid input signal, the "SRC Status" bit operates as intended, i.e. removing the input signal will cause an out-of-lock indication.

BIT	I/F	DSP	RST	NAME	DESCRIPTION
D0	R		1	SRC_Status	When 0, the digital PLL in the SRC is LOCKED. When 1 the digital PLL is OUT of LOCK
D1	R		1	SPDIF_Status	When 1, the SPDIF interface is out of lock. When 0 the interface is locked to the SPDIF stream input.
D2	W	R	0		Reserved
D3	R		0		Reserved
D4	R		0		Reserved
D5	R		0		Reserved
D6	R		0		Reserved
D7	R		0		Reserved
D8	R		0		Reserved
D9	R		0		Reserved
D10	R/W		1	AC3_AMEN	Enable auto-muting if AC3 frame header found
D11	R/W		0	CH1_AMEN	Enable auto-muting if no CH1_STATUS bit found
D12	R	R	0		Reserved
D13	R	R	0		Reserved
D14	R	R	0		Reserved
D15	W	R	0		Reserved

12.17. Coefficient Handling Registers (address 78h – 7Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W				C19	C18	C17	C16

See Section 10

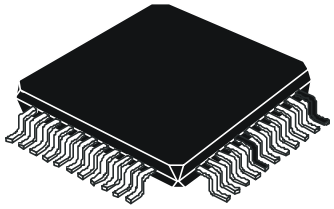
12.18. Vendor ID Register (address 7Ch – 7Eh) (AC'97 only)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0
0	1	0	0	1	0	1	0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

These registers are specific vendor identification for the DDX-4100A. Microsoft's Plug and Play Vendor ID code is "ALJ". The REV7 0 field is for the Vendor Revision number. These are read only registers, any request to one of these will be ignored.

DIM	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0º (min.), 3.5º (typ.), 7º (max.)					

OUTLINE AND MECHANICAL DATA



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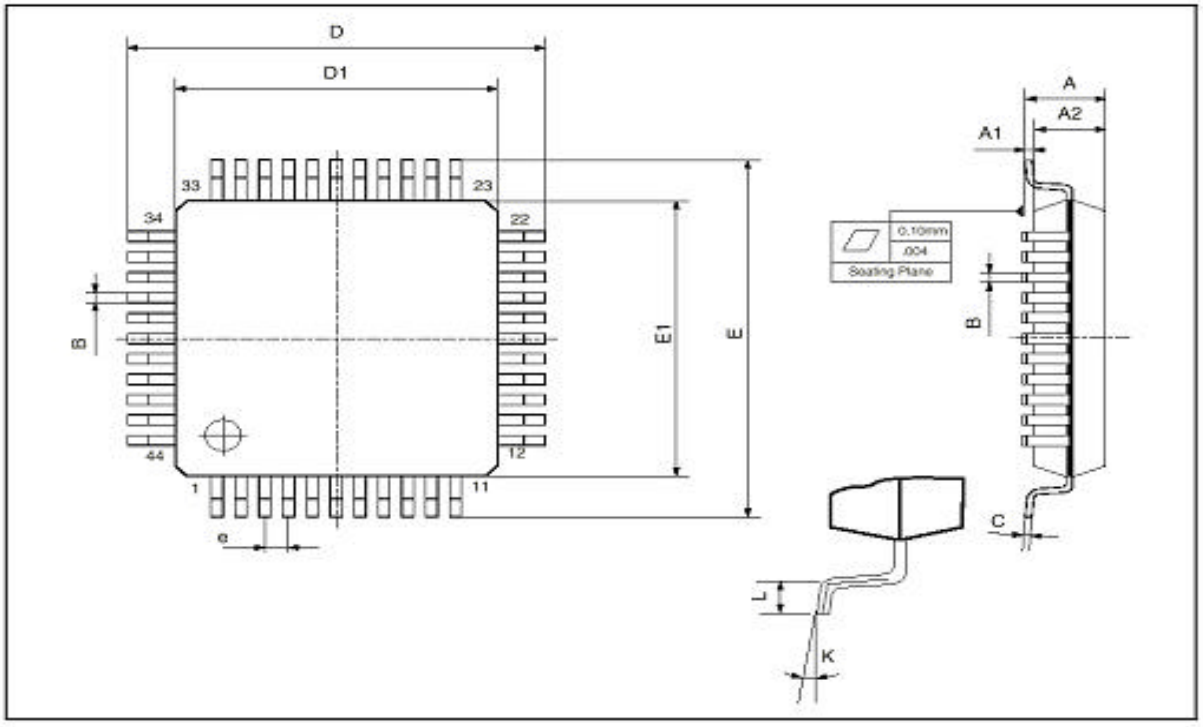

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