DESCRIPTION

PT2256V is an electronic volume controller IC utilizing CMOS Technology specially designed for use on audio equipment. It has 2 built-in channels making it ideally suitable for mono and stereo sound applications. PT2256V provides the Loudness Function, a wide frequency response range and a very low total harmonic distortion, thereby guaranteeing a highly effective and reliable performance. It is housed in 16-pin DIP or SOP and is functionally compatible with TC9235P. Pin assignments and application circuit are optimized for low cost advantages and easy PCB Layout.

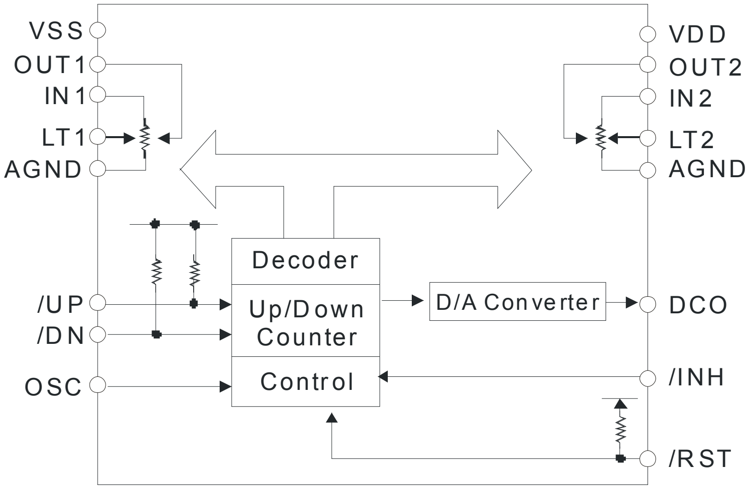
FEATURES

- CMOS Technology
- Low Power Consumption
- Wide Operation Voltage Range: VDD=4.5 ~ 11V
- Least External Components
- 2 Channels in the same chip
- 0dB to -78dB Attenuation can be controlled by UP and Down Pin
- 20dB Tap for Loudness Circuit
- Built-in DC Output Circuit (8 levels) for Volume Level Metering
- Wide Frequency Response Range
- Low Total Harmonic Distortion
- Available in 16 pins DIP or SOP

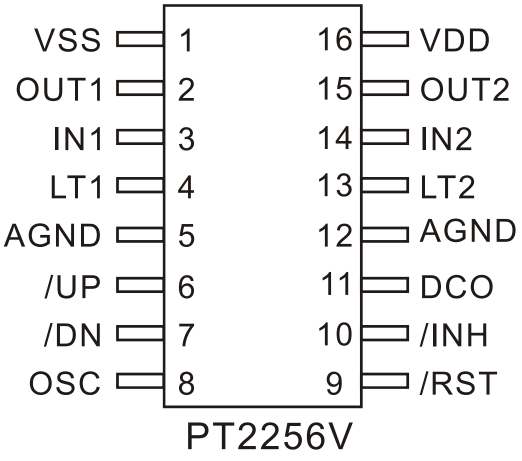
APPLICATION

- Audio Equipment Volume Control

BLOCK DIAGRAM


VSS
OUT1
IN1
LT1
AGND
/UP
/DN
OSC
Decoder
Up/Down Counter
Control
D/A Converter
VDD
OUT2
IN2
LT2
AGND
DCO
/INH
/RST

PIN CONFIGURATION



PIN DESCRIPTION

Pin Number	I/O	Description	Pin No.
VSS	-	Negative Power Supply	1
OUT1	O	Volume Output Pin 1	2
IN1	I	Volume Input Pin 1	3
LT1	O	Tap Output Pin 1 for Loudness Function	4
AGND	-	Analog Ground Pins 1	5, 12
UP	I	Volume UP Control Input Pin. The 1 step/1 push volume is controlled by pressing the UP Key. If the key has been pushed continuously increase. Built-in Pull-up Resistor.	6
DN	I	Volume DOWN Control Input Pin. The 1 step/1 push volume is controlled by pressing the DOWN Key. If the key is continuously pressed, the volume control will continuously decrease. Built-in Pull-up Resistor.	7
OSC	I/O	Oscillation Pin. The oscillation circuit of a resistor and capacitor connection. Oscillator is activated when the key is pressed.	8
RST	I	Reset Pin. This pin sets the initial volume level. The volume level is set to -46dB by “L” Input. Built-in Pull-up Resistor Low Active	9
/INH	I	Backup Mode Input Pin	10
DCO	O	DC Output Pin for Volume Level Meter	11
LT2	O	Tap Output Pin 2 for Loudness Function	13
IN2	I	Volume Input Pin 2	14
OUT2	O	Volume Output Pin 2	15
VDD	-	Positive Power Supply	16

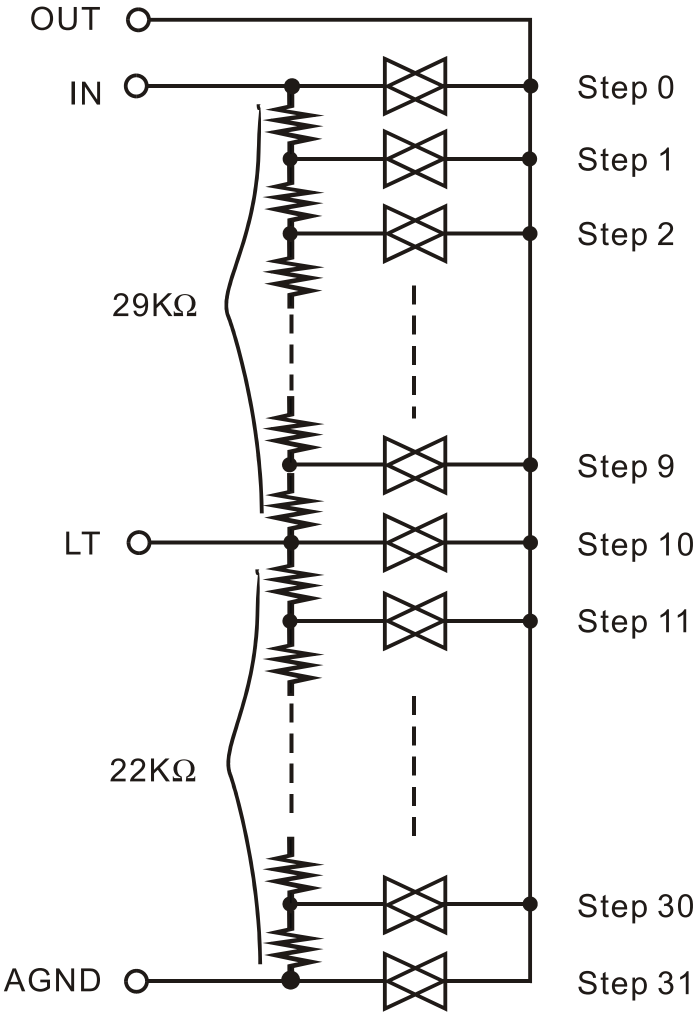
FUNCTION DESCRIPTION

ATTENUATION

The PT2256V volume control circuit consists of ladder resistors and analog switches. The Tap for loudness function is connected to the Step 10 (-20dB). When the (3.9KΩ) resistor is connected between LT and AGND pins, the attenuation is given in table below.

Step	Attenuation (dB)	Step	Attenuation (dB)
0	0	16	-32
1	-2	17	-34
2	-4	18	-36
3	-6	19	-38
4	-8	20	-40
5	-10	21	-42
6	-12	22	-46
7	-14	23	-50
8	-16	24	-54
9	-18	25	-58
10	-20	26	-62
11	-22	27	-66
12	-24	28	-70
13	-26	29	-74
14	-28	30	-78
15	-30	31	∞

The equivalent circuit is shown below:



Note:
1. Step 22 has an initial value of -46dB.

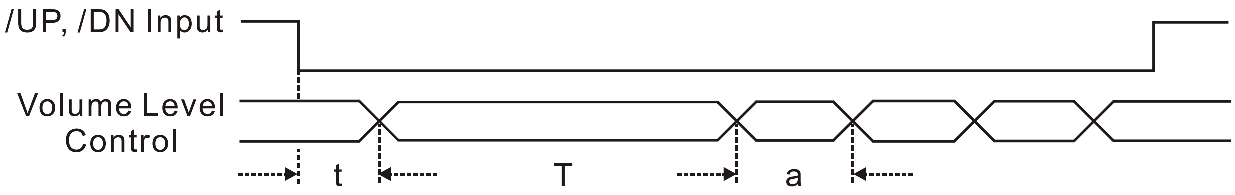
DC OUTPUT FOR VOLUME LEVEL

The DC Output for the Volume Level Meter is internally connected to the D/A Converter. PT2256V has 8 stages of output voltage with each stage corresponding to a particular volume level. Please refer to the table below:

Step	Attenuation (dB)	Output Voltage (V)
0-3	0-6	7/8 VDD
4-7	8-14	6/8 VDD
8-11	16-22	5/8 VDD
12-15	24-30	4/8 VDD
16-19	32-38	3/8 VDD
20-23	40-50	2/8 VDD
24-27	54-66	1/8 VDD
28-31	70-∞	0

UP/DOWN VOLUME CONTROL

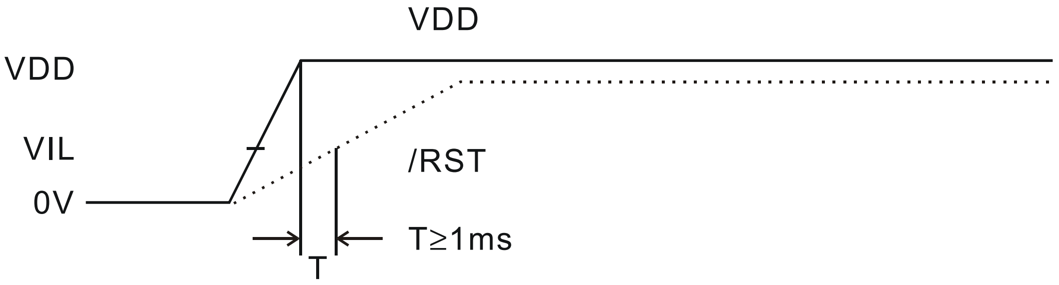
PT2256V features two Volume Control Pins, namely: UP and DN. UP is the control pin used to increase volume level while the DN is the control pin used to decrease the volume level. Thus, volume level may regulated using the Up or Down Keys. These keys are operated on a 1 step/1 push volume level control when UP or DN keys are set to “L” Level. If the keys are continuously pressed (input “Low”), then the volume level continuously steps up or down as the case maybe. Please refer to the diagram below for the timing of the key input.



Notes:
1. t= Preventive Time for Chattering (2.2 x 1/fosc)
2. T= Switching Time to Automatic Mode (10 x 1/fosc)
3. a=Up, Down Speed (2x1/fosc)

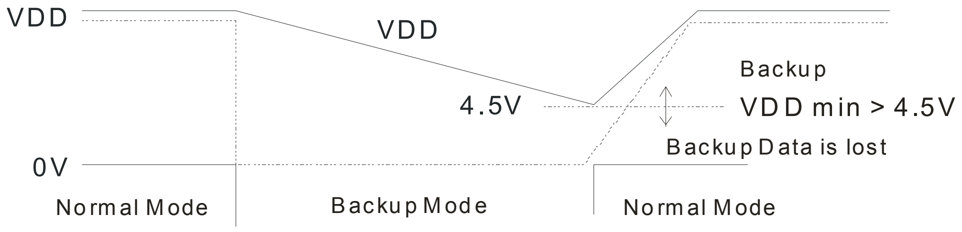
INITIALIZATION WHEN POWER ON

PT2256V has an auto-initialization function during the Power On period. When Power is turned ON, the volume level is set to the initial value of -46 dB by setting the RST pin to "L" level. Please refer to the diagram below.

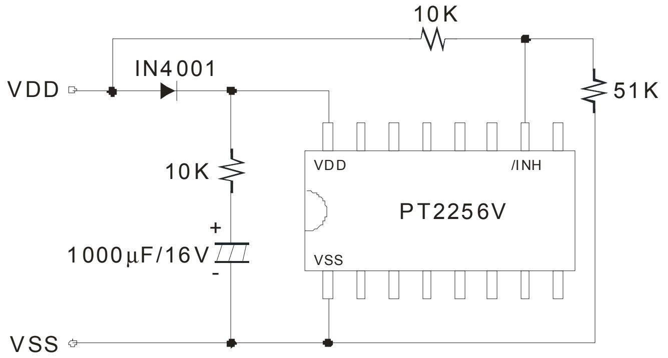

VDD
VDD
VIL
0V
/RST
T≥1ms
T

BACK UP WHEN POWER OFF

When the /INH Pin is set at "L" Level, all input and output pins are disabled and the current consumption is reduced to the minimum. Under this condition, the backup becomes possible. Please refer to the diagram below:


VDD
VDD
Backup
4.5V
VDD min > 4.5V
Backup Data is lost
0V
Normal Mode
Backup Mode
Normal Mode

The backup circuit is given below:

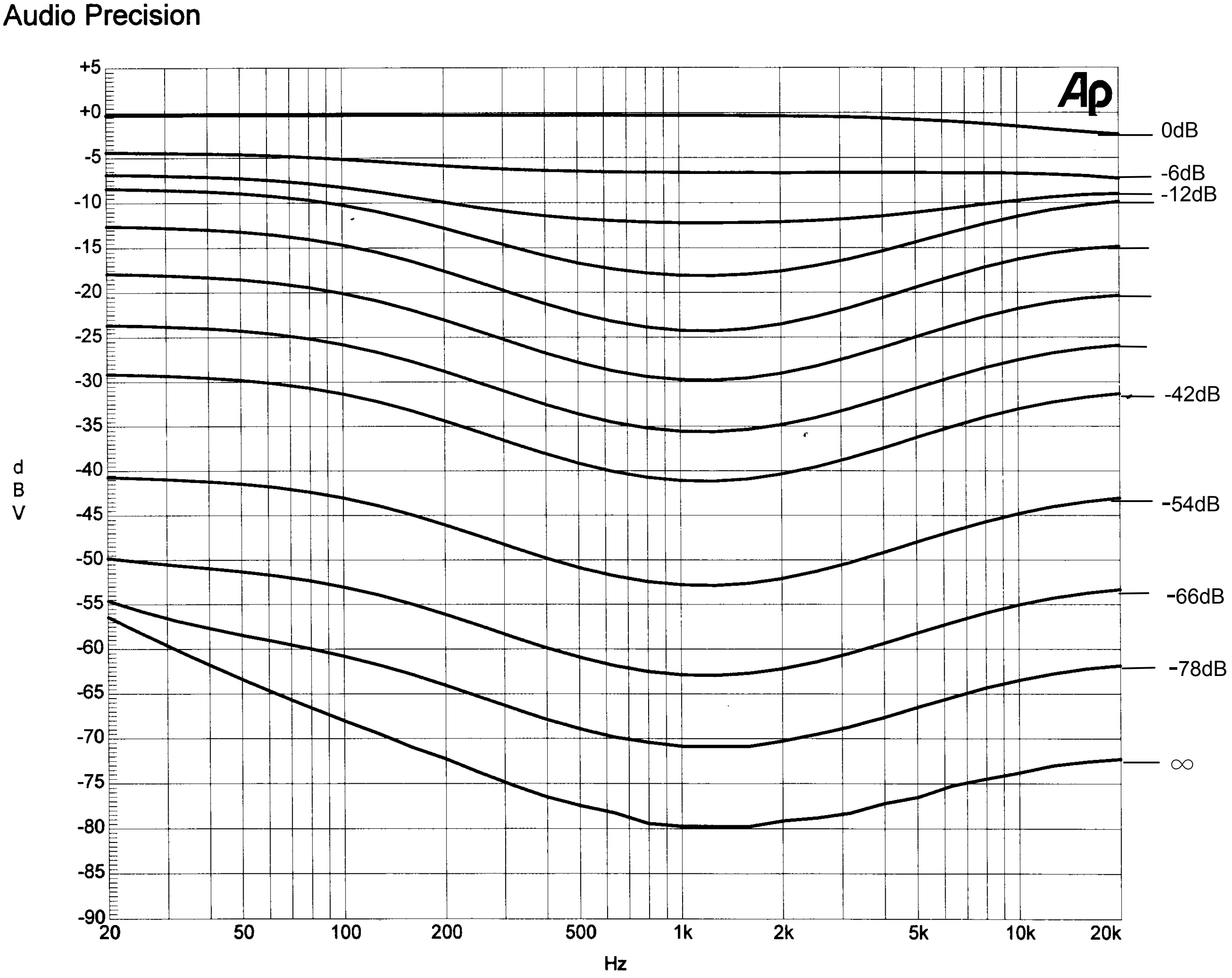

10K
IN4001
VDD
51K
10K
VDD
/INH
PT2256V
+
1000µF/16V
-
VSS
VSS

Notes:

1. If the VDD drops from 11V to 4.5V, then the backup is possible for a period of 6 days. However, if VDD-Vss drops below 4.5V, the backup becomes impossible.

LOUDNESS FREQUENCY RESPONSE

The figure below shows the Loudness Frequency Response Diagram.



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3 to 12	V
Input Voltage	VIN	-0.3 to VDD+0.3	V
Power Dissipation	PD	300	mW
Operating Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-65 ~ +150	℃

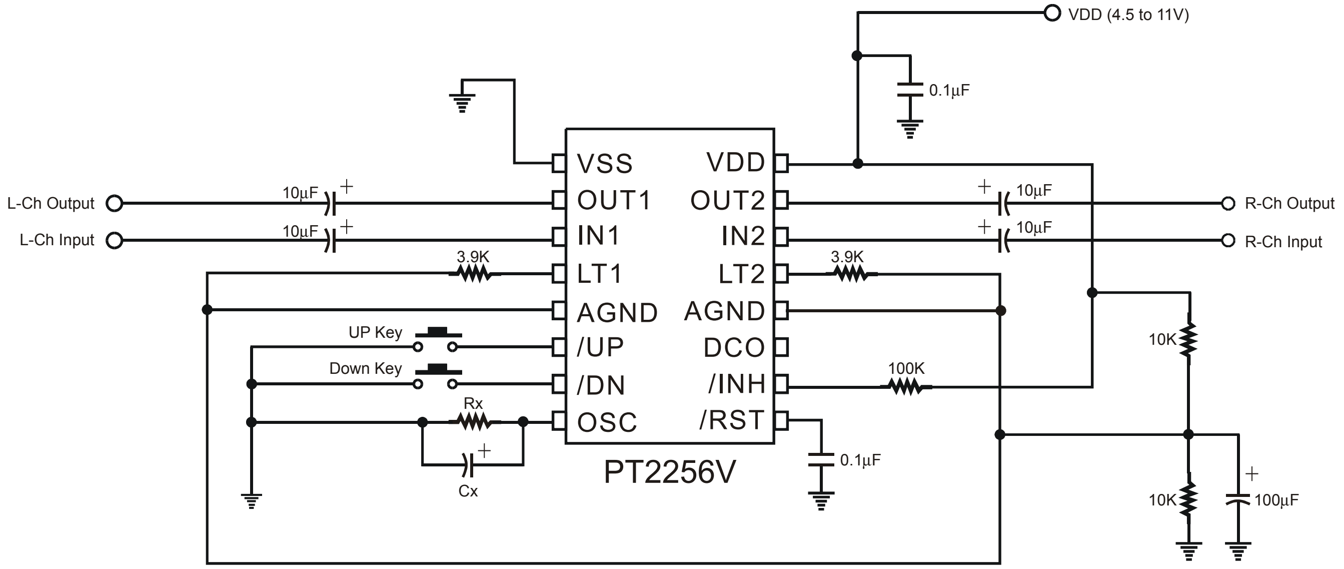
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, VDD=9V)

Parameter	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating Supply Voltage	VDD			4.5	9.0	11	V
Operating Supply Current	IDD	No Load, FOSC=20Hz		-	0.3	1.0	mA
Stand-by Current	ISB	OSC=0V, /INH=0V		-	0.3	10	μA
Backup Voltage	VOD	/INH Pin=0V		2.0	-	11	V
Backup Current	IOD			-	0.1	1.0	μA
High Level Input Voltage	VIH	/UP, /DN, /RST		0.7VDD	-	VDD	V
		/INH		0.8VDD	-	VDD	
Low Level Input Voltage	VIL	/UP, /DN, /RST		0	-	0.3VDD	V
		/INH		0	-	0.7VDD	
Voltage Resistor	RVR	Between IN~AGND Resistor		45	54	75	KΩ
		Between IN~LT Resistor		26	29	45	
		Between LT~AGND Resistor		19	22	32	
High Level Input Current	IIH	/INH Input Pin, VIL=VDD		-1	-	1	mA
Low Level Input Current	IIL	/INH Input Pin, VIN=0V		-1	-	1	mA
Pull-up Resistor	Rup	/UP, /DN, /RST Input Pin		50	70	100	KΩ
Analog Switch ON Resistor	RON	When 0dB, Between IN1~OUT1 and IN2~OUT2 Resistor		-	400	500	Ω
Attenuation Error	△ATT	Test Attenuation Value		-	0	±2.0	dB
Balance between Left and Right	△RVR	Volume Resistor Error between Left and Right		-	0	±3.0	%
Total Harmonic Distortion	THD	FIN=1KHz, VIN=1Vrms, RL=100KΩ, Rg=600Ω	0dB	-	0.01	-	%
Maximum Attenuation	ATTMAX		∞dB	-	90	-	dB
Cross Noise	CT		0dB	-	90	-	dB
Output Noise	VN		0dB	-	-100	-	dB
OSC Frequency	FOSC	CX=2.2μf, Rx=33KΩ		-	18	-	Hz
Output Resistance	ROUT	FIN=1KHz, VIN=1Vrms, Volume Control=0dB		550	650	750	Ω
Maximum Input Amplitude	VIN	FIN=1KHz, Volume Control=0dB, THD<0.08%	VDD=9V	-	-	3.5	Vrms

APPLICATION CIRCUIT

SINGLE POWER SUPPLY (NO LOUDNESS AND NO BACKUP CIRCUIT)


VDD (4.5 to 11V)
0.1µF
VSS
VDD
OUT1
OUT2
IN1
IN2
LT1
LT2
AGND
AGND
/UP
DCO
/DN
/INH
OSC
/RST
PT2256V
L-Ch Output
L-Ch Input
10µF
10µF
3.9K
UP Key
Down Key
Rx
Cx
R-Ch Output
R-Ch Input
10µF
10µF
3.9K
100K
0.1µF
10K
10K
100µF

Notes:

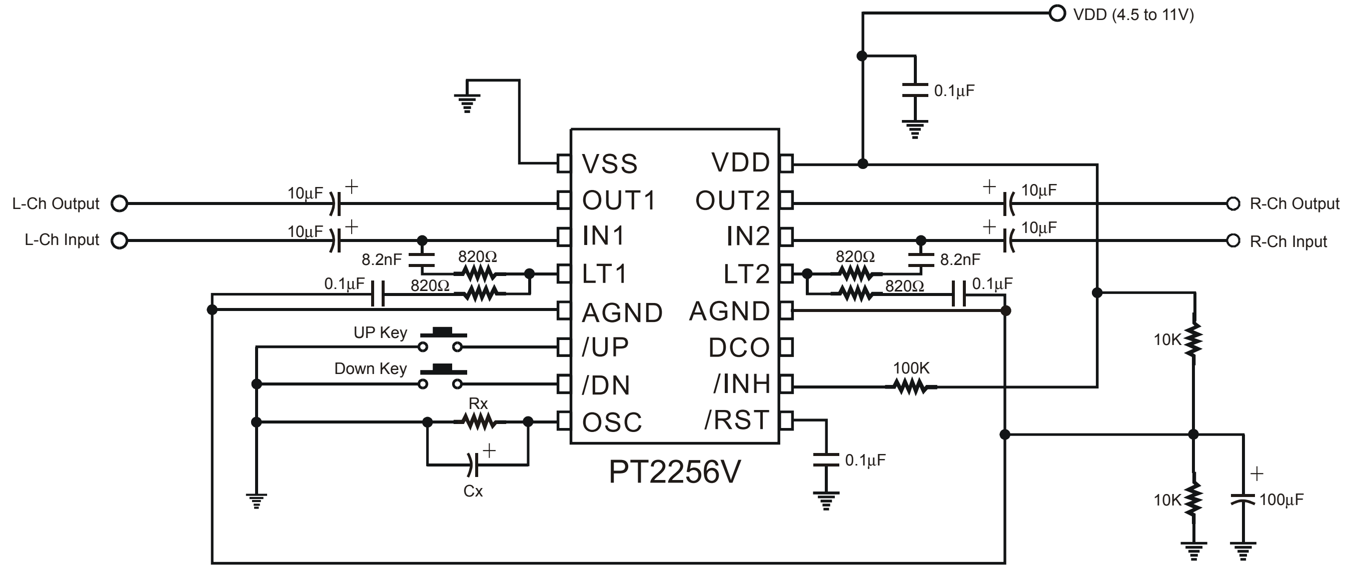
1. Modifying the values of Rx and Cx affects the Oscillator Frequency of the IC. If the Fosc value is big, then the volume control change is fast. Likewise, if the Fosc value is small, the volume control change is slow. It is suggested that Rx= 33K, Cx=2.2µF.

2. The table for the Rx, Cx and Fosc values are given below:

Rx	Cx	Fosc
33K	1.0µF	34.1Hz
33K	2.2µF	17.8Hz
33K	10µF	3.4Hz

Rx	Cx	Fosc
33K	1.0µF	34.1Hz
51K	1.0µF	22.7Hz
100K	1.0µF	11.8Hz

INCLUDING LOUDNESS BUT NO BACKUP CIRCUIT


VDD (4.5 to 11V)
0.1µF
L-Ch Output
L-Ch Input
10µF
10µF
8.2nF
820Ω
820Ω
0.1µF
UP Key
Down Key
Rx
Cx
VSS
OUT1
IN1
LT1
AGND
/UP
/DN
OSC
VDD
OUT2
IN2
LT2
AGND
DCO
/INH
/RST
PT2256V
R-Ch Output
R-Ch Input
10µF
10µF
820Ω
8.2nF
820Ω
0.1µF
100K
0.1µF
10K
10K
100µF

Notes:

1. Modifying the values of Rx and Cx affects the Oscillator Frequency of the IC. If the Fosc value is big, then the volume control change is fast. Likewise, if the Fosc value is small, the volume control change is slow. It is suggested that Rx= 33K, Cx=2.2µF.

2. The table for the Rx, Cx and Fosc values are given below.

Rx	Cx	Fosc
33K	1.0µF	34.1Hz
33K	2.2µF	17.8Hz
33K	10µF	3.4Hz

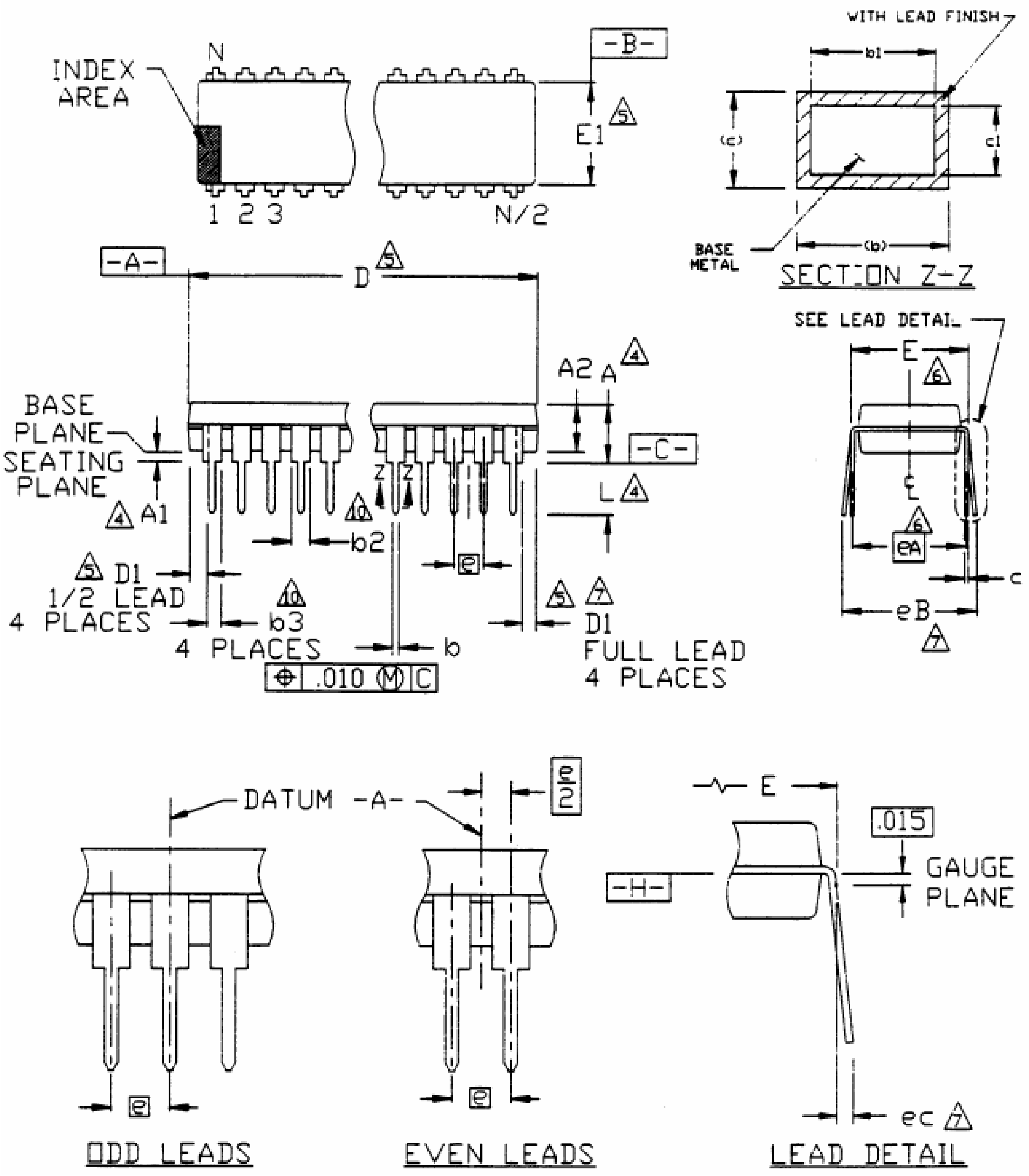
Rx	Cx	Fosc
33K	1.0µF	34.1Hz
51K	1.0µF	22.7Hz
100K	1.0µF	11.8Hz

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2256V	16 Pins, DIP, 300mil	PT2256V
PT2256V-S	16 Pins, SOP, 300mil	PT2256V-S
PT2256V-SN	16 Pins, SOP, 150mil	PT2256V-SN

PACKAGE INFORMATION

16PINS, DIP, 300MIL


INDEX AREA
N
1 2 3
N/2
-B-
E1
5
WITH LEAD FINISH
b1
(c)
c1
BASE METAL
(b)
SECTION Z-Z
-A-
D
5
SEE LEAD DETAIL
E
6
A2
A
4
BASE PLANE
SEATING PLANE
-C-
L
4
4 A1
Z Z
10
b2
e
5 D1
1/2 LEAD
4 PLACES
10
b3
4 PLACES
b
⊕ .010 Ⓜ C
5 7
D1
FULL LEAD
4 PLACES
℄
6
eA
c
eB
7
DATUM -A-
e/2
E
.015
-H-
GAUGE PLANE
e
e
ec 7
ODD LEADS
EVEN LEADS
LEAD DETAIL

Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.780	0.790	0.800
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 bsc	
eA		0.300 bsc	
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:

1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D”, “D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -c-. “eB” and “eC” are measured at the lead tips with the loads unconstrained.
6. “N” is the number of terminal positions. (N=16)
7. Pointed or rounded lead tips are preferred to ease insertion.
8. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25 mm).
9. Distance between leads including Dambar protrusions to be 0.005 inch minimum.
10. Datum plane -H- coincident with the bottom of lead, where lead exits body.
11. Refer to JEDEC MS-001 Variation AB.

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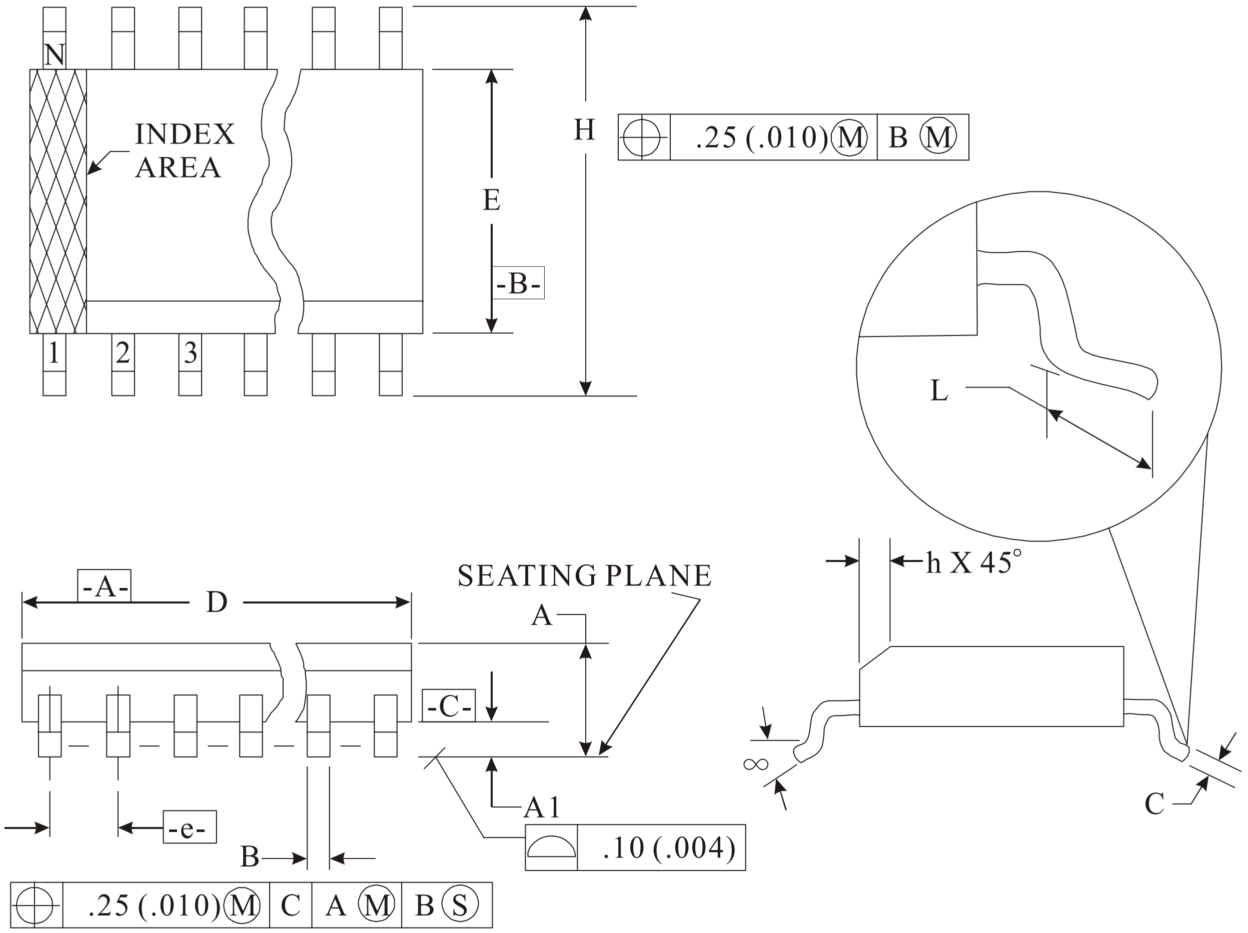
16PINS, SOP, 300MIL


N
INDEX AREA
1
2
3
E
-B-
H
.25 (.010) Ⓜ B Ⓜ
L
-A-
D
SEATING PLANE
A
-C-
A1
.10 (.004)
-e-
B
.25 (.010) Ⓜ C A Ⓜ B Ⓢ
h X 45°
α
C

Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	10.10	10.50
E	7.40	7.60
e	1.27 BSC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. N is the number of the terminal positions (N=16)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension : MILLIMETER.
9. Refer to JEDEC MS-013, Variation AA.

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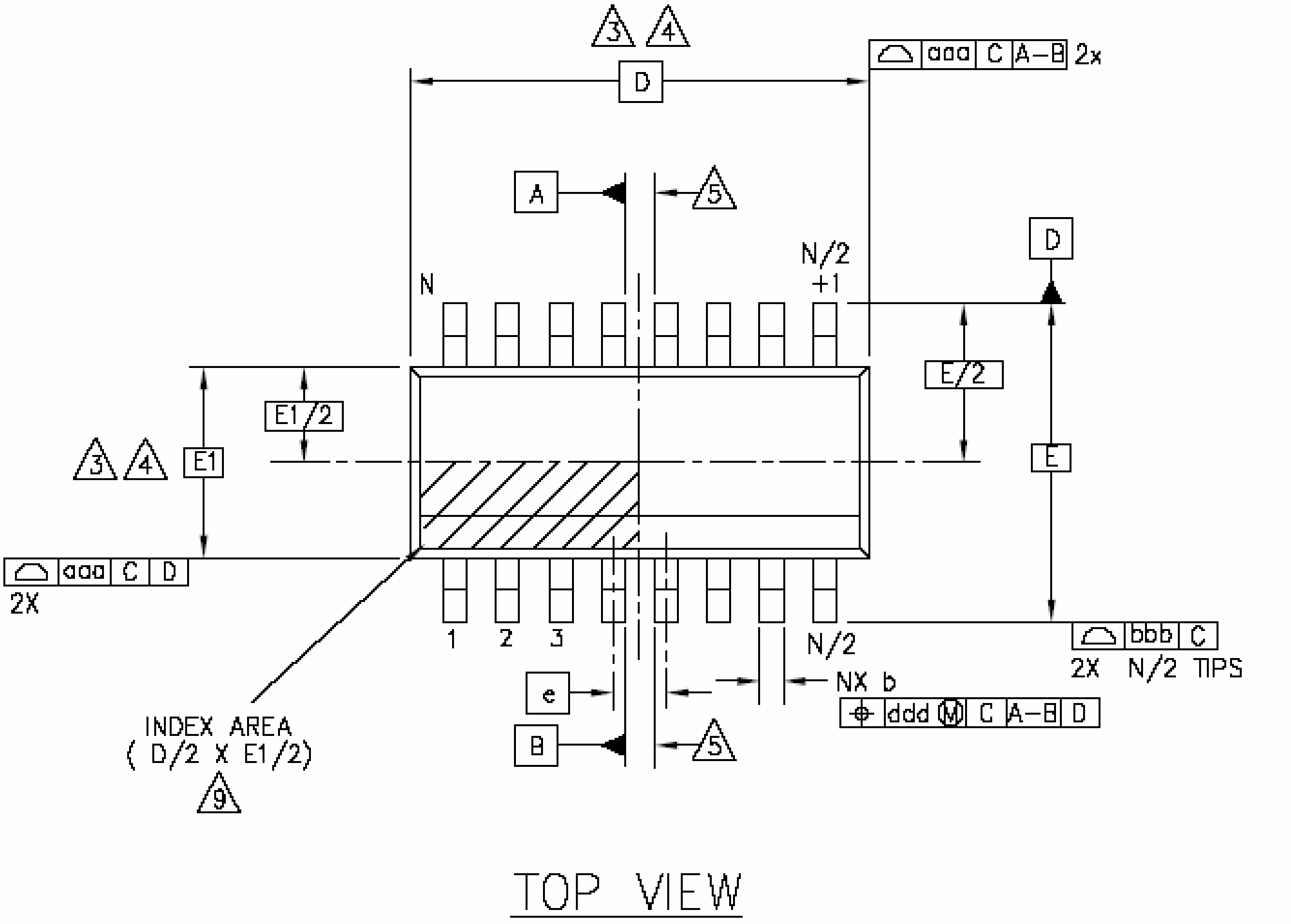
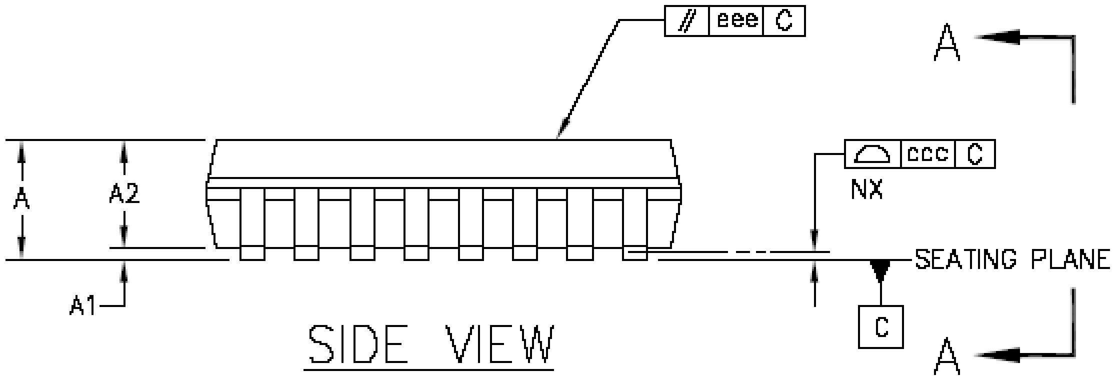
16 PINS, SOP, 150MIL

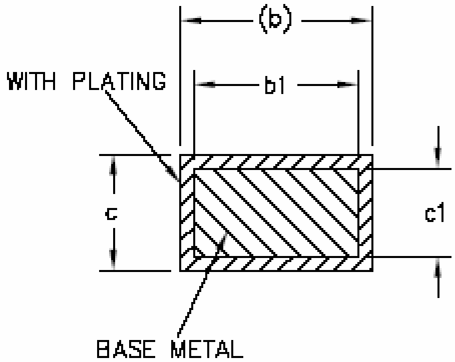

3
4
D
aaa C A–B 2x
A
5
N
N/2 +1
D
E/2
E1/2
3
4
E1
E
aaa C D
2X
1 2 3
N/2
bbb C
2X N/2 TIPS
e
NX b
ddd M C A–B D
B
5
INDEX AREA
(D/2 X E1/2)
9

TOP VIEW

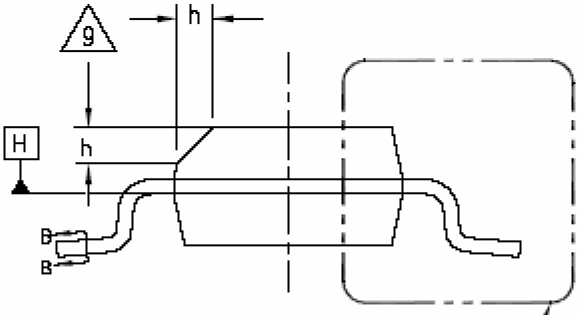

// eee C
A
ccc C
NX
A
A2
A1
SEATING PLANE
C
A

SIDE VIEW

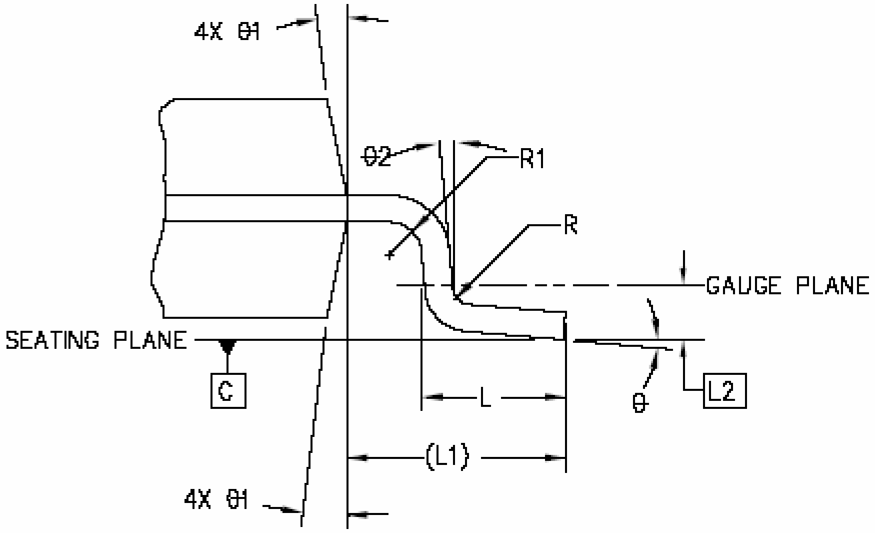
SEE SHEET 2


(b)
WITH PLATING
b1
c
c1
BASE METAL

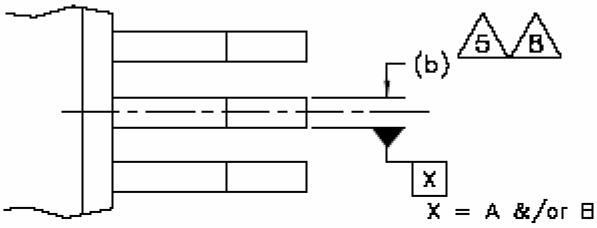
SECTION B–B
7


9
h
H
h
B
B
SEE VIEW C

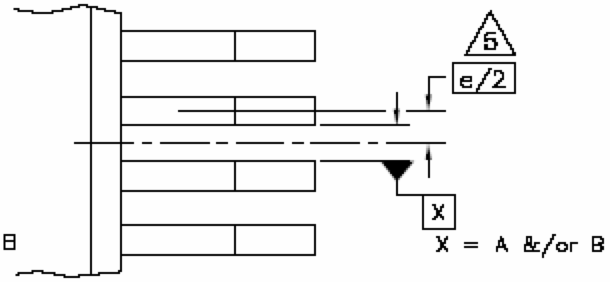
VIEW A–A
SHEET 1


4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1

VIEW C



ODD LEAD SIDES
TOPVIEW



EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	9.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Note:

1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=16)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AC.

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