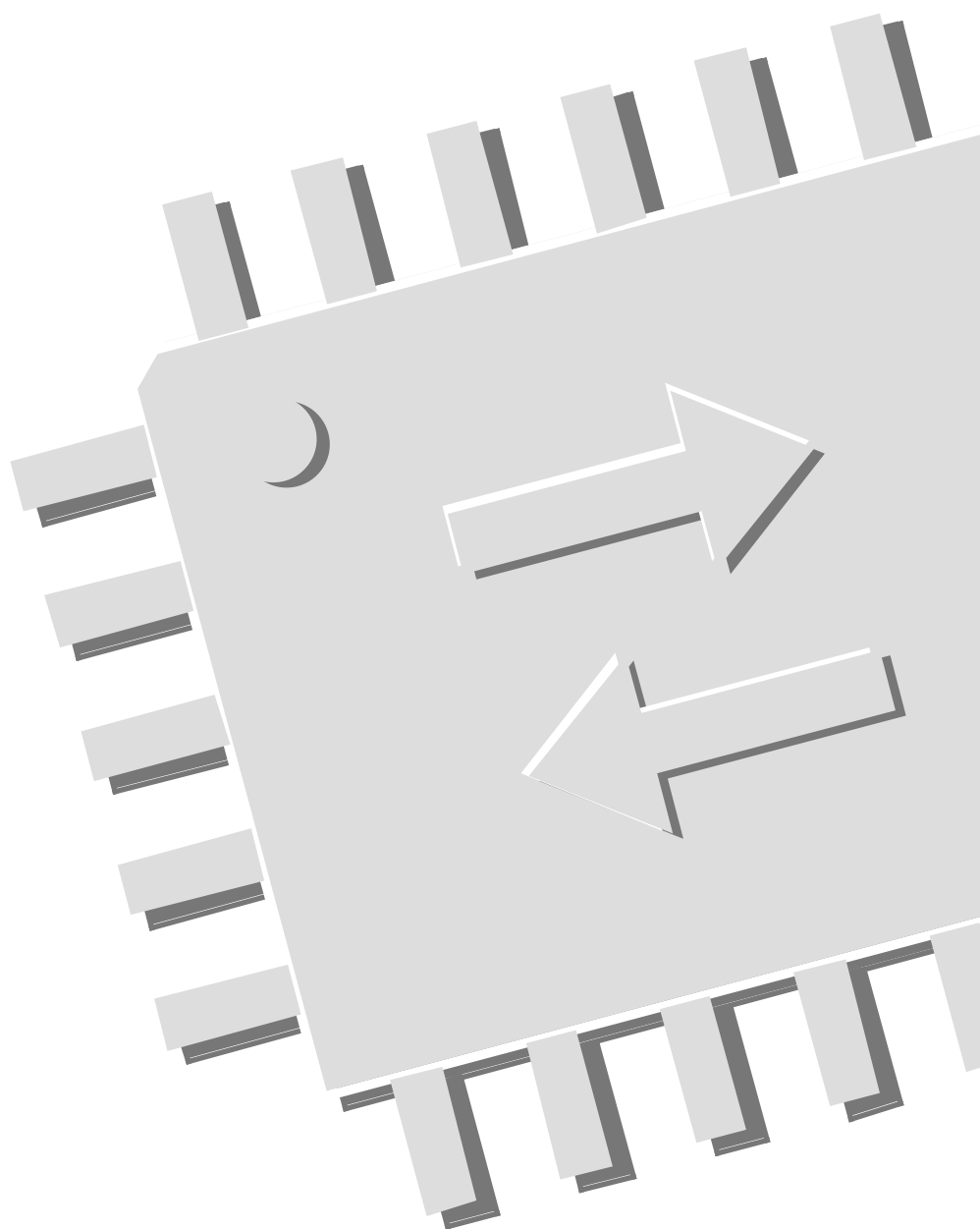


LINK (IEEE 1394)

MD8412

Users Manual

PRELIMINARY



MEMO

History

Revision	Date	Contents
0.92	1996.12.03	Original

MEMO

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1 General Descriptions

The MD8412 is a link layer controller for high-speed serial buses, designed in accordance with the IEEE draft standard, IEEE 1394 -1995. It involves all necessary functions for the link layer, and also functions to relieve the burden of the system for isochronous transfer. Therefore, it is suitable for being incorporated in equipment on the side of peripheral terminals.

1-1 Features

- ☐ Packing for transmission and unpacking for reception, according to IEEE 1394 -1995
- ☐ Cycle master support
- ☐ Parity generation and error detection by 32-bit CRC
- ☐ Detection of dropped cycle start messages
- ☐ Direct with PHY chip (MD8402) and interface by AC coupling
- ☐ 3-speed support of 100/200/400Mb/sec.
- ☐ Control of the No. of transfers in each cycle during isochronous transfer
- ☐ Automatic insertion of a header in isochronous packet during transmission and automatic header separation and routing during reception
- ☐ Support of outbound retry sequence
- ☐ Feasibility of selecting a host-bus width from 8/16/32-bit, enabling easy connection with a general-purpose MPU/microcomputer
- ☐ Support of both big and little-endians during selection of host bus 16/32-bit

1-2 Applications

- | | | |
|---|--------------------------------------|--|
| <input type="checkbox"/> Digital camera | <input type="checkbox"/> Digital VTR | <input type="checkbox"/> Digital audio |
| <input type="checkbox"/> Electronic musical instruments | <input type="checkbox"/> Scanner | <input type="checkbox"/> Printer |
| <input type="checkbox"/> Various storages | | |

1-3 Internal block diagram

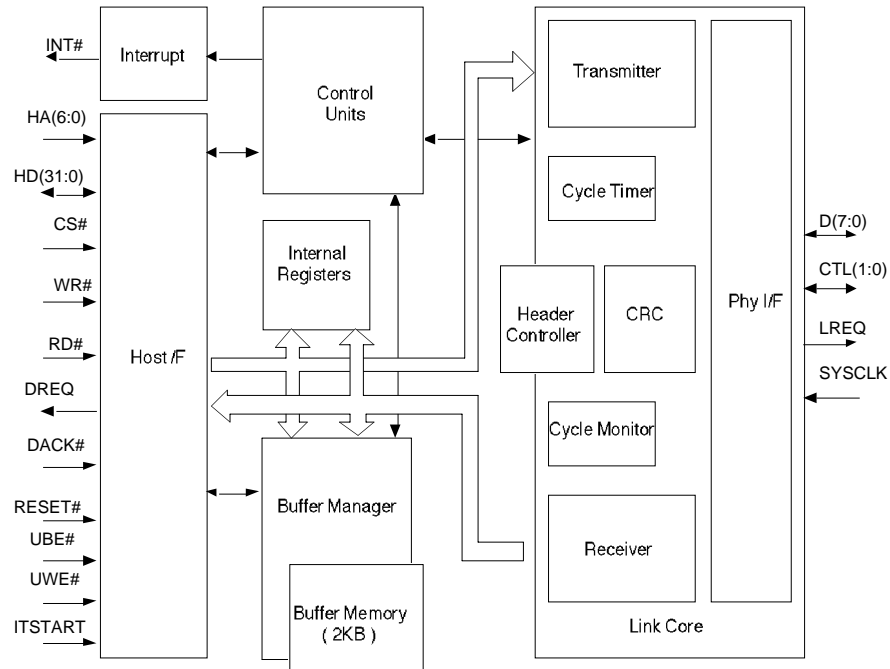


Figure 1-3-1 MD8412 Block Diagram

1-4 Functional outlines

1-4-1 Host interface

The host interface is composed of asynchronous buses in a width of SRAM-style 8/16/32-bit. Since DMA control functions are provided inside, DREQ signals can be generated according to the state of a buffer, enabling high-speed data transfer.

Bus width changeover of 8/16/32 can be controlled by a signal of UWE#, UBE#, A1, or A0. It is possible to change register and buffer access operation. All registers can be directly accessed from the host. In DMA transfer, internal buffer selection is effected to enable gaining access to the selected buffer.

1-4-2 PHY interface

An interface is available, which enables direct connection with the PHY chip to process a physical layer according to IEEE 1394. Either 100Mbps or 200Mbps is acceptable for the PHY chip to be connected.

In the IEEE1394 Draft, the connection mode for the PHY and LINK chips is classified to the following two kinds:

- DC connection
- AC connection

This IC supports both kinds of connections.

1-4-3 Transmitter

The transmitter reads out data from an asynchronous transmission buffer or an isochronous transmission buffer in the MD8412, and sends out a PHY interface packet through formatting into each packet format defined by IEEE P1394. If the cycle master bit is 1 and the node using the MD8412 is a route, then a cycle start packet is also

sent out to indicate the head of the isochronous cycle.

1-4-4 Receiver

The receiver receives a packet from the PHY interface and identifies if this packet is the one to be acquired by the node of MD8412. If it is found as an asynchronous packet, it is identified with a node address of MD8412. If it is an isochronous packet, it is identified with a preset channel number. If a packet is headed to this node, routing is effected toward the asynchronous reception buffer or the isochronous reception buffer by writing the data therein. For a broadcast packet and the snoop mode, no judgment is effected and data are written in their buffer.

1-4-5 Built-in buffer

The MD8412 incorporates a buffer in 512 32(bit) configuration with a capacity of 2K-byte in total. This is a temporary buffer intended for data rate absorption between transmitter and host bus. The host performs data access to this buffer.

The MD8412 controls this buffer by dividing it into a maximum of 4 areas. Two of the divided areas are used at random for asynchronous transmission and reception. The remaining two areas depend on isochronous modal setting. Each buffer size is designated at the register. Status information, such as full or empty in the buffer, can be known at the host in the divided unit.

1-4-6 Isochronous transfer functions

The MD8412 possesses isochronous functions. It incorporates a cycle timer so that a cycle start packet can be transmitted in the unit of 125Ésec when the node seizing the MD8412 is of the cycle master. Its trigger is an 8KHz signal entered through the CYCLEIN pin, obtained as a result of generation of a clock signal of 49.152MHz, coming from the PHY chip.

When the above-mentioned node is not of the cycle master, synchronism with the cycle master is secured through compensation of the cycle master within the MD8412, based on the value of that packet, each time a cycle start packet is received from another cycle master node.

The MD8412 is provided with two types of isochronous modes. One is a mode intended to gain access to the host with a packet image. The other is a mode for host access with an image of data themselves. (To be described in detail later)

The user determines the mode, according to the nature of data source to be handled in the isochronous transfer mode.

2 Terminal Description

2-1 Functional description for terminals

Signal	Type	Pin	No. of Pin	Contents															
PHY Interface																			
SCLK	I		1	Master clock: A 49.152MHz clock signal fed from the PHY chip. The MD8412 employs this clock as a master clock signal. Usually connected to this signal pin of the PHY chip.															
LREQ	O		1	Link request: The MD8412 uses this signal when making a request of register access in the PHY chip and when using a serial bus. Usually connected to this signal pin of the PHY chip.															
CTL(0:1)	I/O		2	PHY-LINK control: An interface control signal for data transmission/reception with the PHY chip. Usually connected to this signal pin of the PHY chip.															
D(0:7)	I/O		8	PHY-LINK data bus: A data bus for data transmission/reception with the PHY chip. D(1:0) is used for packet transmission/reception at 100Mbps, D(3:0) is used at 200Mbps, and all bits are used at 400Mbps.															
DIRECT	I		1	PHY I / F direct select signal : A changeover signal used to selectdirect or isolation connection of I / F with PHY. 0 : Isolation connection 1 : Direct connection															
LPS	O		1	Link status : An LPS signal to PHY. Output in the following combination available by register setting <table><tr><td>DIRECT input</td><td>LPSON bit</td><td>LPS output</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>Clock output of about 2MHz</td></tr></table>	DIRECT input	LPSON bit	LPS output	1	0	0	1	1	1	0	0	0	0	1	Clock output of about 2MHz
DIRECT input	LPSON bit	LPS output																	
1	0	0																	
1	1	1																	
0	0	0																	
0	1	Clock output of about 2MHz																	
Host Interface																			
HA(6:0)	I		7	Host address: A host address for register selection.															
HD(31:0)	I/O		32	Host data bus: A data bus for register data access. In combination with other signals, effective bit width is changeable among 31, 16, and 8 bits. Combinations will be described later.															
WR#	I		1	Write enable: A writing signal for host data bus.															
RD#	I		1	Read enable: A reading signal for host data bus.															
CS#	I		1	Chip select: A chip select signal for host data buses.															
UWE#	I		1	Upper write enable: An enable signal of the upper word (16-bit) for a 32-bit data bus. With active low of this signal, the upper 16-bit is also asserted on the data bus.															
UBE#	I		1	Upper byte enable: An enable signal of the upper byte in 16-bit of the upper/lower word for a 32-bit data bus. With active low of this signal, the upper 8-bit is also asserted in the upper and lower words, respectively.															
DREQ	O		1	Data request: A request signal for DMA transfer. Asserted only for packet and data transfer.															
DACK#	I		1	Data acknowledge: An acknowledge signal for DMA transfer. Asserted only for packet and data transfer.															
INT#	O		1	Interrupt signal: An interrupt signal for announcement to the host. This signal is asserted when any factor arises in the interrupt register.															

Table 2-1 MD8412 Terminal Table (1)

Signal	Type	Pin	No. of Pin	Contents
Others				
CYCLEIN	I		1	Isochronous cycle input : An external clock for counting the internal cycle timer in 8KHz unit. When CycleSource bit is " 1 " in the control register, this clock becomes valid.
CYCLEOUT	O		1	Isochronous cycle output : A cycle clock output generated by counting the internal cycle timer of the MD8412.
RESET#	I		1	Reset : A system reset signal of the MD8412.
Test Terminals				
TEST	I		4	A signal for testing.
Power supply				
VDD	I			5.0V power supply.
VSS	I			GND

Table 2-2 MD8412 Terminal Table (2)

3 Control Register

3-1 Method of register access

For 32-bit access, each register gains a description of header address only. Accordingly, the following addresses are used for 8- and 16-bit.

	7	6	5	4	3	2	1	0
Index +3	BYTE(adrs+3)							
	15	14	13	12	11	10	9	8
Index +2	BYTE(adrs+2)							
	23	22	21	20	19	18	17	16
Index +1	BYTE(adrs+1)							
	31	30	29	28	27	26	25	24
Index	BYTE(adrs)							

Figure 3-1-1 Register Address on 8-Bit Bus

	7	6	5	4	3	2	1	0
Index +2	WORD-L(adrs+2)							
	15	14	13	12	11	10	9	8
	WORD-H(adrs+2)							
	23	22	21	20	19	18	17	16
Index	WORD-L(adrs)							
	31	30	29	28	27	26	25	24
	WORD-H(adrs)							

Figure 3-1-2 Register Address on 16-Bit Bus

3-2 Contents of register

3-2-1 Version Register

Index 00h
Initial value 0000 0000h

This register provides chip version and revision number. It is effective in software for IEEE 1394-LINK chip control in the future.

7	6	5	4	3	2	1	0
Revision							
15	14	13	12	11	10	9	8
Revision							
23	22	21	20	19	18	17	16
Version							
31	30	29	28	27	26	25	24
Version							

Bit 15~0 Revision: Revision number of IC chip (R-initial value: 0000h)
ndicates the revision number of MD8412. This figure begins with ÉÅ0ÉÇ and increases each time revision is made.

Bit 31~16 version: Version number of IC chip (R-initial value: 0000h)
Indicates the version number of MD8412. "0000h" is always read out of the MD8412.

3-2-2 Control Register

Index 04h

Initial value 0000 0000h

This register makes settings for each operational configuration of the chip, enable, etc. Generally, this register setting is made shortly after the closure of the POWER switch. The MD8412 configuration should have been defined in advance.

7	6	5	4	3	2	1	0
			LPSOn			ReceiveEn	TransmitEn
15	14	13	12	11	10	9	8
23	22	21	20	19	18	17	16
	IsoMode				CycleSource	CycleMaster	CycleTimerEn
31	30	29	28	27	26	25	24
		DMAWidth					Little

Bit 0 TransmitEn: Transmit Enable bit (RW- Initial value: 0b)

- 0 = Transmitter disabled
- 1 = Transmitter enabled

Setting is made to decide if the MD8412 transmitter is enabled or not. In the case of enable, the following transmission is performed:

- Asynchronous packet
- Cycle start packet with a cycle master bit enabled
- Isochronous packet for cycle start

This bit is automatically set at 1 when a request for bus reset is received from the PHY chip.

Bit 1 ReceiveEn: Receive Enable bit (RW- Initial value: 0b)

- 0 = Receiver disabled
- 1 = Receiver enabled

Setting is made to decide if the MD8412 receiver is enabled or not. In the case of enable, the following reception is performed:

- Synchronous packet addressed from another node to this node
- Isochronous packet of the designated channel
- Reception in snoop mode

Bit 4 LPSOn : Ink power status on bit (RW - initial value : 0b)

This bit is used to control the LPS signal supplied to the PHY chip. According to the status of the DIRECT terminal, contents of output are different.

DIRECT terminal	LPSOn bit	LPS terminal output
High	0	Low
High	1	High
Low	0	Low
Low	1	Clock of about 1MHz

Bit 16 **CycleTimerEn:** Cycle Timer Enable bit (RW- Initial value: 0b)

0 = Cycle timer disabled

1 = Cycle timer enabled

Setting is made to decide if the MD8412 cycle timer is enabled or not.

Bit 17 **CycleMaster:** Cycle Master bit (RW- Initial value: 0b)

0 = Receiving a cycle start packet from a node in another route, cycle timer control is effected. To be set at 0 when this node cannot belong to an ordinary route.

1 = When this bit is 1 a cycle start packet is generated each time the MD8412 cycle timer carries.

Bit 18 **CycleSource:** Cycle Sourcer bit (RW- Initial value: 0b)

0 = The cycle timer is counted with 24.576MHz of the master clock that is a clock signal fed from the PHY chip, in order to control the isochronous cycle.

1 = The cycle timer is updated at the rising point of a signal entered from the CYCLEIN terminal.

The updating source is set up for the internal timer that is in charge of isochronous time control.

Bit 22~20 **IsoMode:** Isochronous Mode bit (RW- Initial value: 0b)

Isochronous Mode	Transmission	Reception
000	Normal	Normal
001	Normal	Auto
010	Auto	Normal
011	-	Auto
100	Auto	Auto
101	-	Normal
1xx	Reserved	

Settings of normal mode and auto-mode are made for both isochronous transmission and reception.

The number of corresponding isochronous channels is as specified below, according to the mode of transmission or reception:

Transmission in normal mode	No. of channels for packets where buffer areas are not full for each isochronous cycle. For each cycle, however, the number of packets for each channel is limited to 1.
Transmission in auto-mode	Limited to 1 channel. A normal mode is used if more channels are needed to support.
Reception in normal mode	For '101', packets for maximum of 4 channels can be received. For '010', however, the number of channels is limited to 3. Setting for channel designation is made at the IsoConfigReg.
Reception in auto-mode	Limited to 1 channel. Only for '011', however, 2-channel reception is possible. In this case, routing is effected on the buffer for each channel. (At that time, isochronous transmission is disabled.)

Bit 24 **Little:** Little-endian bit (RW- Initial value: 0b)

- 0 = Data of ATF, ARF, ITF, IRF buffer are handled as a Big-endian.
- 1 = Data of ATF, ARF, ITF, IRF buffer are handled as a Little-endian.

Bit 29~28 **DMAWidth :** DMA Transfer Data Width bit(RW - Initial value : 00b)

- 00 = 8-bit (Byte) transfer
- 01 = 16-bit (Word) transfer
- 10 = 32-bit (Quadlet) transfer
- 11 = Reservation

3-2-3 Node Identification Register

Index 08h
Initial value 0000 FFFFh

7	6	5	4	3	2	1	0
BusNumber-L		NodeNumber					
15	14	13	12	11	10	9	8
BusNumber-H							
23	22	21	20	19	18	17	16
31	30	29	28	27	26	25	24
IDValid							

Bit 5~0 NodeNumber: Node Number bit (RW- Initial value: 3Fh)

This value is used to set up a 6-bit node number to be defined in the IEEE1212 space. During transmission, this value is used in the source area of the IEEE P1394 packet format header. When receiving a packet, the destination node number of this packet is examined and when found to coincide with this value, the packet is received. It is rejected in otherwise case.

Usually, the node number is read from the PHY chip and setting is made at this register after the completion of bus reset and end of self-identification phase.

Bit 15~6 BusNumber: Bus Number bit (RW- Initial value: 3FFh)

This value is used to set up a 10-bit bus number to be defined in the IEEE1212 space. During transmission, this value is used in the source area of the header area in the IEEE P1394 packet format header. During reception, this BusNumber bit is disregarded.

Bit 31 IDValid: ID Valid bit (RW- Initial value: 00b)

0 = Only the packet (broadcast packet) is received, where the value of NodeNumber is addressed as Fh . In other cases, the packet is rejected.

1 = Only the packet is received, for which the value of NodeNumber is addressed in the IEEE1212 address space set by the above-mentioned register. A broadcast packet is also received.

When the state of bus reset arises, this register is automatically cleared to 00b . The node number is generally determined after the completion of bus reset and end of self-identification phase.

Accordingly, this value is set up after the host has set it in the NodeNumber register.

3-2-4 Reset Register

Index 0Ch
Initial value 0000 0000h

7	6	5	4	3	2	1	0
	ResetDMA	ResetLink	ResetTx	ResetIRF	ResetARF	ResetITF/ IRF	ResetATF
15	14	13	12	11	10	9	8
23	22	21	20	19	18	17	16
31	30	29	28	27	26	25	24

Bit 0 ResetATF: Reset ATF bit: (RW- Initial value: 0b)

- 0 = Normal condition
- 1 = Buffer area initialized for asynchronous transmission

Only the buffer area for asynchronous transmission is returned to initial state. At that time, however, all data in that area are lost. All status flags of this buffer are also returned to their initial state.

When $\overline{EN1E\ddot{U}}$ is set, and when internal initialization is completed later, this bit is automatically set at $\overline{EN0E\ddot{U}}$.

Bit 1 ResetITF/IRF: Reset ITF/IRF bit (RW- Initial value: 0b)

- 0 = Normal condition
- 1 = Buffer area initialized for isochronous transmission/reception

When IsoMode setting is for other than '011' isochronous transmission buffer is restored to initial conditions. When it is for $\overline{EN011E\ddot{U}}$ mode, only the buffer area is restored to initial conditions for isochronous channel reception designated by isochronous configuration 2,3 register. At that time, however, all data in that area are lost. All status flags of this buffer are also returned to their initial state.

When $\overline{EN1E\ddot{U}}$ is set, and when internal initialization is completed later, this bit is automatically set at $\overline{EN0E\ddot{U}}$.

Bit 2 ResetARF: Reset ARF bit(RW - Initial value : 0b)

- 0 = Normal condition
- 1 = Buffer area initialized for asynchronous reception

Only the buffer area for asynchronous reception is returned to initial state. At that time, however, all data in that area are lost. All status flags of this buffer are also returned to their initial state.

When $\overline{EN1E\ddot{U}}$ is set, and when internal initialization is completed later, this bit is automatically set at

ÉÑ0ÉÜ.

Bit 3 ResetIRF: Reset IRF bit (RW- Initial value: 0b)

0 = Normal condition

1 = Buffer area initialized for isochronous reception

Only the buffer area for isochronous channel reception specified by the isochronous configuration register is returned to initial state. At that time, however, all data in that area are lost. All status flags of this buffer are also returned to their initial state.

When ÉÑ1ÉÜ is set, and when internal initialization is completed later, this bit is automatically set at ÉÑ0ÉÜ.

Bit 4 ResetTx: Reset Transmitter bit (RW- Initial value: 0b)

0 = Normal condition

1 = Transmitter being reset

Transmitter is reset to set up a transmission-enabled condition. If a packet is being transmitted, that transmission is supported. When ÉÑ1ÉÜ is set, and when internal initialization is completed later, this bit is automatically set at ÉÑ0ÉÜ.

Bit 5 ResetLink: Reset Link Core bit (RW- Initial value: 0b)

0 = Normal condition

1 = Link core being reset

Link Core is reset to support all operation. When ÉÑ1ÉÜ is set, and when internal initialization is completed later, this bit is automatically set at ÉÑ0ÉÜ.

Bit 6 ResetDMA: Reset DMA bit (RW- Initial value: 0b)

0 = Normal condition

1 = DMA control being reset

DMA control is reset to set up a condition enabling DMA transfer. DMA is required to complete transfer in the Quadlet unit. The DMA transfer pointer in the Quadlet unit is cleared with this bit and the pointer is set in the header position in the Quadlet unit. When ÉÑ1ÉÜ is set, and when internal initialization is completed later, this bit is automatically set at ÉÑ0ÉÜ.

3-2-5 Asynchronous Buffer Size Set Register

Index 10h

Initial value 007F 00FFh

In this register, an assignment size is specified to assign an asynchronous area to the internal buffer having a 2KB capacity. This size is specified in the Quadlet unit.

7	6	5	4	3	2	1	0
ATotalSize							
15	14	13	12	11	10	9	8
							ATotalSize
23	22	21	20	19	18	17	16
ARxBufferSize							
31	30	29	28	27	26	25	24
							ARxBufferSize

Bit 8~0 ATotalSize: Asynchronous Total Buffer bit (RW- Initial value: 0FFh)

All buffer sizes for asynchronous transmission and reception are specified in the Quadlet unit. All data (isochronous also) remaining in the buffer before modification are abandoned.

Bit 24~16 ARxBufferSize: Asynchronous Receive Buffer Size bit (RW- Initial value: 07Fh)

Buffer size for asynchronous reception is specified in the Quadlet unit. In this case, this value must always be smaller than the one set by TotalSize. If this value is changed, all data remaining in the asynchronous transmission/reception buffer are abandoned. There is no influence in the isochronous domain.

By the above-mentioned two setting values, the transmission buffer size is defined as:

$$ATransmitBufferSize = ATotalSize - ARxBufferSize$$

3-2-6 Isochronous Buffer Size Set Register

Index 14h

Initial value 007F 00FFh

In this register, an assignment size is specified to assign an isochronous area to the internal buffer having a 2KB capacity. This size is specified in the Quadlet unit.

7	6	5	4	3	2	1	0
ITotalSize							
15	14	13	12	11	10	9	8
							ITotalSize
23	22	21	20	19	18	17	16
IRxBufferSize							
31	30	29	28	27	26	25	24
							IRxBufferSize

Bit 8~0 ITotalSize: Isochronous Total Buffer bit (RW- Initial value: 0FFh)

All buffer sizes for isochronous transmission and reception are specified in the Quadlet unit. When IsoMode is ÉÑ011ÉÜ , however, transmission buffer is lost and setting is made in the receiving buffer for two channels.

Bit 24~16 IRxBufferSize: Isochronous Receive Buffer Size bit (RW- Initial value: 07Fh)

Buffer size for isochronous reception is specified in the Quadlet unit. In this case, this value must always be smaller than the one set by TotalSize. If this value is changed, all data remaining in the isochronous transmission/reception buffer are abandoned.

If IsoMode is not ÉÑ011ÉÜ , the transmission buffer size is defined as follows by the above-mentioned two setting values:

$$\text{ITransmitBufferSize} = \text{ITotalSize} - \text{IRxBufferSize}$$

When IsoMode is ÉÑ011bÉÜ , contents of the Isochronous Configuration 3 register are stored in the buffer being set by the IRxBufferSize, and contents of the Isochronous Configuration 2 register are stored in the buffer being set by the ITransmitBufferSize.

When IsoMode is ÉÑ101bÉÜ , ITotalSize and IRxBufferSize must be set at the same value.

3-2-7 Packet Control Register

Index 18h
Initial value 0000 1020h

7	6	5	4	3	2	1	0
		RxSelfID	EnSnoop				
15	14	13	12	11	10	9	8
			WritePending		BusyCtrl		
23	22	21	20	19	18	17	16
31	30	29	28	27	26	25	24

Bit 4 EnSnoop: Enable Snoop bit (RW- Initial value: 0b)

- 0 = Normally, only the packet mapped in this node address is received.
1 = Snoop mode assumed.

Regardless of the node address assumed, a snoop mode is set up so that all packets, except PHY control packets carried on the serial bus, can be received. When a packet is received, the Ack code is not returned. All packets received in this mode are stored in the IRF buffer.

Bit 5 RxSelfID: Receive Self ID bit (RW- Initial value: 1b)

- 0 = No SelfID packet is inserted in the buffer.
1 = SelfID packet is input in the buffer.

This bit makes setting to decide whether the SelfID packet received in the Self ID phase after bus reset should be put in the buffer area for reception Async.

Bit 10~8 BusyCtrl: Busy Control bit (RW- Initial value: 000b)

- 000 = A Busy Acknowledge is returned according to the dual phase retry protocol only if there is no vacancy of one packet to be received at the internal Async reception buffer.
001 = An Acknowledge is returned in BusyA status only if there is no vacancy of one packet to be received at the internal Async reception buffer.
010 = An Acknowledge is returned in BusyB status only if there is no vacancy of one packet to be received at the internal Async reception buffer.
011 = An Acknowledge is returned in BusyX status only if there is no vacancy of one packet to be received at the internal Async reception buffer.
100 = A Busy Acknowledge is returned according to the dual phase retry protocol irrespective of whether there is vacancy of one packet to be received at the internal Async reception buffer.
101 = An Acknowledge is returned in BusyA status for all packets received irrespective of whether there is vacancy of one packet to be received at the internal Async reception buffer.

110 = An Acknowledge is returned in BusyB status for all packets received irrespective of whether there is vacancy of one packet to be received at the internal Async reception buffer.

111 = An Acknowledge is returned in BusyX status for all packets received irrespective of whether there is vacancy of one packet to be received at the internal Async reception buffer.

When the MD8412 node is of inbound and a busy status acknowledge is returned for the packet from the outbound node transmitted to MD8412, contents of that status are set in this register.

Bit 12 WritePending: Write Request Ack-Pending bit (RW- Initial value: 1b)

0 = Ack-Complete is returned when reception is normal with Ack code for Write Request packet.

1 = Ack-Pending is returned when reception is normal with Ack code for Write Request packet.

When a Write Request packet is normally received, the Ack code generally returns Ack-Complete. If the packet cannot be received normally, due to lack of buffer capacity or the like, Ack-Busy is returned. When this bit is set at 1, the Ack code returns Ack-Pending under the condition that reception is normal. In other words, Split Transaction of Write Request is to be executed. Upon completion of Write Request processing, the host is required to transmit a Write Response packet. The table below shows types of Ack codes to be sent back for each packet. Items mark by O are Ack codes.

Packet	WritePending = '0b'			WritePending = '1b'		
	ack_complete	ack_pending	ack_busy	ack_complete	ack_pending	ack_busy
Write Request	O	-	O	-	O	O
Read Request	-	O	O	-	O	O
Write Response	O	-	O	O	-	O
Read Response	O	-	O	O	-	O
Lock Request	-	O	O	-	O	O
Lock Response	O	-	O	O	-	O

3-2-8 Diagnostic Status Register

Index 1Ch

Initial value 0000 0000h

It is possible to know various status information in this register.

7	6	5	4	3	2	1	0
					BusyState		
15	14	13	12	11	10	9	8
RetryTimeOut		AckStatus		ATAck			
23	22	21	20	19	18	17	16
				ARStatus			
31	30	29	28	27	26	25	24
						ITBusy	ATBusy

Bit 2 BusyState: Busy State bit (R- Initial value: 0b)

0 = Acknowledge is returned with BusyA

1 = Acknowledge is returned with BusyB

When Busy Acknowledge is to be issued at the next opportunity, this node indicates the type of this Acknowledge.

Bit 11~8 ATAck: AT Ack bit (R- Initial value: 0000b)

0000 =No Ack

0001 =ack_complete

0010 =ack_pending

0011 =Reserved

0100 =ack_busy_X

0101 =ack_busy_A

0110 =ack_busy_B

0111~1100 = Reserve

1101 =ack_data_error

1110 =ack_type_error

1111 = Reserve

For the packet sent from the transmitter during transmission, contents of Acknowledge (Ack code) returned from the destination node are reflected in this register. The reflection timing is when a busy flag for showing the packet being processed in the transmitting asynchronous buffer is negated. This value is held until this Busy is negated for the next packet transmission.

Bit 13~12 AckStatus: Ack Status bit (R- Initial value: 00b)

00 = Normal reception

01 = Parity error

10 = Packet lost (indicating that no Acknowledge packet has been sent in the specified time)

11 = Reserve

For the transmitted Asynchronous packet, the status of Acknowledge packet returned from the destination node is indicated.

Bit 15 RetryTimeOut: Retry Time Out bit (R- Initial value: 0b)

0 = Normal

1 = Retry time-out

This bit indicates a condition that a retry phase is started, but it is not completed within the retry count value in the ATRetry register. This value is held until the next packet transmission is performed.

Bit 19~16 ARStatus: AR Status bit (R- Initial value: 0000b)

When an Asynchronous packet is received, the status of Acknowledge returned to the source node is indicated in this register. The value of this packet is kept in this register until everything of the packet has been read out of the MD8412.

Bit 24 ATBusy: AT Busy bit (R- Initial value: 0b)

0 = Indicates that ATGo issuing is possible.

1 = Indicates that ATGo issuing is impossible, and that a packet is presently being processed for the previously issued ATGo.

This bit is asserted upon the issuing of ATGo for Asynchronous transmission. It is negated when return of this Acknowledge has been set in the ATAck register. The host cannot issue the next ATGo while this bit is being asserted. Even though it is attempted, it is disregarded. When a packet transmission turns to be a retry operation, this bit is never negated until the said Retry is finished.

Bit 25 ITBusy: IT Busy bit (R- Initial value : 0b)

0 = Indicates that ITGo issuing is possible.

1 = Indicates that ITGo issuing is impossible, and that a packet is presently being processed for the previously issued ITGo.

For isochronous transmission in normal IsoMode, this bit is asserted with ITGo issued, and negated upon completion of packet transmission. The host cannot issue the next ITGo until this bit is being asserted. Even though it is attempted, it is disregarded.

3-2-9 Phy Control Register

Index 20h
Initial value 0000 0000h

Using this register, a register in PHY chip is accessed. When reading a certain register, its register address is set in the RegAddr register and the RdReg bit is made active. With the RdReg bit being active, a read request for the addressed register is made to the PHY chip and the RdReg bit is then cleared. Contents of the addressed register from the PHY chip are entered in the RegData register. The write request to the PHY register for the data in the RegData register is also made by triggering the WrReg bit of the PHY address set in the RegAddr register.

7	6	5	4	3	2	1	0
RegData							
15	14	13	12	11	10	9	8
	RegRcvd	RdReg	WrReg	RegAddr			
23	22	21	20	19	18	17	16
31	30	29	28	27	26	25	24

Bit 7~0 RegData: Register Data bit (RW- Initial value: 00h)

With a Write request, data being transferred to PHY are stored. With Read request also, data transferred from PHY are stored. When reading out the contents of this register, contents of RegData are read out, the value taken from PHY with the previous Read request. In other words, the value taken from the host cannot be directly read out. To read out, a Read request must be sent to PHY.

Bit 11~8 RegAddr: Register Address bit (RW- Initial value: 00h)

The address value of PHY being accessed is set.

Bit 12 WrReg: Write Register bit (RW- Initial value: 0b)

- 0 = Normal condition
- 1 = Write request issued

A Write request is issued toward the PHY register. After this Write request, this bit is cleared.

Bit 13 RdReg: Read Register bit (RW- Initial value: 0b)

- 0 = Normal condition
- 1 = Read request issued

A Read request is issued toward the PHY register. After this Read request, this bit is cleared.

Bit 14 RegRcvd: Register Data Received bit (RW- Initial value: 0b)

- 0 = Normal condition
- 1 = Indicating that data from PHY have been stored in RegData after the issuing of Read request

After a Read request has been issued toward the PHY register, PHY_RD_DATA is set upon the storage of PHY data in RegData. Since then, PHY_RD_DATA is cleared to PHY_RD_DATA when reading is attempted once from this register.

3-2-10 ATRetries Register

Index 24h
 Initial value 0000 0001h

There is a function of performing automatic retry when asynchronous packet transmission is attempted by the MD8412 node and Busy Acknowledge is returned from this destination node. The number of retries is set in this register. Once a retry phase is assumed, a busy flag of the ATGo register is never negated until any Acknowledge other than Busy is returned from the destination node or the preset number of retries is attained. In this state, the next packet transmission is disabled.

7	6	5	4	3	2	1	0
RetryCount				MaxRetryCount			
15	14	13	12	11	10	9	8
23	22	21	20	19	18	17	16
31	30	29	28	27	26	25	24

Bit 3~0 MaxRetryCount: Maximum Retry Count bit (RW- Initial value: 01h)

This register sets up the maximum number of retries for Busy Acknowledge from the destination node. If the retry phase is not completed within this set value, a retry time-out status flag is given in the ATAck register to complete the retry phase attempted by the MD8412. Since then, packet data are flushed within the ATF buffer. The maximum number that can be set is 15. When $\overline{EN}0000\overline{E}\overline{U}$ is set, the MD8412 does not assume a retry phase automatically. In this case, packet data are flushed for Busy Acknowledge. When an error Acknowledge is returned in the retry phase, retry is suspended at that time point and contents of the buffer are flushed. Further operation is halted by presenting a flag (AckErr).

Bit 7~4 RetryCount Retry Count bit (R- Initial value: 00h)

The number of present retries is indicated in the middle of a retry attempted from MD8412.

3-2-11 Cycle Timer Register

Index 28h
Initial value 0000 0000h

The present cycle timer value is indicated. As described below, this register is divided into three areas. When the node employing MD8412 is of CycleMaster and a cycle start packet is being transmitted, this register value is loaded. In otherwise case, the cycle timer value in the received cycle start packet is loaded in this register in order to update the cycle timer. Timing to load is when the Lo byte of CycleOffset has been written.

7	6	5	4	3	2	1	0
CycleOffset							
15	14	13	12	11	10	9	8
CycleCount				CycleOffset			
23	22	21	20	19	18	17	16
CycleCount							
31	30	29	28	27	26	25	24
CycleSeconds							CycleCount

Bit 11~0 CycleOffset Cycle Offset bit (RW- Initial value: 00h)
This area is used for counting up with a 24.576MHz clock. It is actuated with Modulo3072.

Bit 24~24 CycleCount Cycle Count bit (RW- Initial value: 00h)
This area is used for counting up when the CycleField register carries to count Isochronous cycles. It is actuated with Modulo8000.

Bit 31~25 CycleSeconds Cycle Seconds bit (RW- Initial value: 00h)
This area is used for counting up when the CycleCount register carries to count seconds. It is actuated with Modulo128.

3-2-12 Isochronous Packet Length Register

Index 2Ch

Initial value 0004 0000h

When IsoMode is assumed and its transmission mode is Auto (setting value = 010BÉÇ or 100bÉÇ), the data volume of one packet to be transferred in each isochronous cycle is set in this register.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8
23	22	21	20	19	18	17	16
ITLength							
31	30	29	28	27	26	25	24
				ITLength			

Bit 27~16 ITLength: Isochronous Transmit Length bit (RW- Initial value: 04h)

Length of a packet being transmitted is set in this register. During transmission, this value is used at the header part.

3-2-13 Isochronous Configuration Register 1,2,3,4

Index 30h, 34h, 38h, 3Ch

Initial value 0000 0000h

For transmission/reception of an isochronous packet, this register group determines how MD8412 handles this packet. In some cases, registers are not used according to the number of registers by IsoMode setting nor the definition in each register.

7	6	5	4	3	2	1	0
StopSync						IsoRxEn	SyncEn
15	14	13	12	11	10	9	8
Sync				StartSync			
23	22	21	20	19	18	17	16
						Speed	
31	30	29	28	27	26	25	24
Tag		Channel					

Bit 0 **SyncEn:** Sync Enable bit (RW- Initial value: 0b)

- 0 = Packet transmission/reception is effected regardless of the contents of StartSync and StopSync. During AutoMode transmission, contents of the Sync register are reflected at any time in the Sync area of the packet header.
- 1 = In the Receive mode, packet reception is controlled with the channel number of the above setting plus StartSync and StopSync. During AutoMode transmission, contents of Start Sync are entered in the Sync field of the packet header to be transmitted shortly after the ITSTART terminal or the ITStart register has been turned active. Since then, contents of Sync are entered in StopSync shortly after ITSTART is turned non-active.

Bit 1 **IsoRxEn:** Isochronous Receive Enable bit (RW- Initial value: 0b)

- 0 = Isochronous reception disabled
- 1 = Isochronous reception enabled

Setting is made to define whether isochronous reception is enabled or not.

Bit 7~4 **StopSync:** Stop Sync bit (RW- Initial value: 00h)

When SyncEn=1, reception control is effected with the Sync field values of this bit and packet. Once packet reception is started with StartSync and after a packet has been received, with which its register value coincides with the Sync field of a packet of the set channel number, packet reception is suspended thereafter. When SyncEn=0 in the auto-transmission mode, and if transmission is stopped by the ITSTART terminal or the ITStart register, this value is written in the Sync field of the last packet received shortly before stoppage.

Bit 8~11 **StartSync:** Start Sync bit (RW- Initial value: 00h)

When SyncEn=1, reception control is effected with the Sync field value of this bit and packet. Reception is started again with a packet whose register value coincides with the Sync field value of the packet with the preset channel number. When SyncEn=0 in the auto-transmission mode, and when transmission is started with the ITSTART terminal or the ITStart register, this value is written in the Sync field of the packet to be sent first.

Bit 15~12 Sync: Sync bit (RW- Initial value: 00h)

For 00h and 100h in IsoMode, in the isochronous transmission auto-mode, this register sets up a value so that the MD8412 can input this value in the Sync field of the packet header. In other modes, this register remains to be disabled. With SyncEn=0 this value is written at any time. When SyncEn=1 this value is written in a packet other than the start/end packet, with the ITSTART terminal or the ITStart register.

Bit 17~16 Speed: Speed bit (RW- Initial value: 00b)

- 00 = Transmission at 100Mbps
- 01 = Transmission at 200Mbps
- 10 = Transmission at 400Mbps
- 11 = Reserved

In the transmission mode, the transfer speed is set up for transmission to be effected over the cable. In the reception mode, this register remains to be disabled.

Bit 29~24 Channel: Channel bit (RW- Initial value: 00h)

In auto-transmission mode, a channel is specified for the isochronous packet. The channel number set here is loaded in the packet header for transmission. In the reception mode, an isochronous channel intended for reception in both modes is set up. The setting range is from 0 to 63.

Bit 31~30 Tag: Tag bit (RW- Initial value: 00h)

In auto-transmission mode, a tag is specified for an isochronous packet. The setting range is from 0 to 3.

The relationship between contents of the IsoMode register and this configuration register group is shown below.

Mode	ICR Number	Transit/Receive	Channel	Speed	SyncEn	Sync	StartSync	StopSync
000	1	Normal Transmit	-	-	-	-	-	-
	2, 3, 4	Normal Receive	Valid	-	Valid	-	Valid	Valid
001	1	Normal Transmit	-	-	-	-	-	-
	2	Auto Receive	Valid	-	Valid	-	Valid	Valid
				3, 4 (Unused)				
010	1	Auto Transmit	Valid	Valid	Valid	Valid	Valid	Valid
	2, 3, 4	Normal Receive	Valid	-	Valid	-	Valid	Valid
011	2, 3	Auto Receive	Valid	-	Valid	-	Valid	Valid
				1, 4 (Unused)				
100	1	Auto Transmit	Valid	Valid	Valid	Valid	Valid	Valid
	2	Auto Receive	Valid	-	Valid	-	Valid	Valid
				3, 4 (Unused)				
101	1, 2, 3, 4	Normal Receive	-	Valid	Valid	-	Valid	Valid

*ICR : Isochronous Configuration Register

3-2-14 ATF Data Register

Index 40h

Initial value 0000 0000h

This is a register for writing asynchronous packet transmission data. Data are written in the internal buffer for asynchronous transmission. In cases other than host 32-bit access, it is always necessary to write data in the Quadlet unit.

7	6	5	4	3	2	1	0
ATFData							
15	14	13	12	11	10	9	8
ATFData							
23	22	21	20	19	18	17	16
ATFData							
31	30	29	28	27	26	25	24
ATFData							

3-2-15 ARF Data Register

Index 44h

Initial value 0000 0000h

This is a register for reading asynchronous packet reception data. Data are read from the internal buffer for asynchronous reception. In cases other than host 32-bit access, it is always necessary to read data in the Quadlet unit.

7	6	5	4	3	2	1	0
ARFData							
15	14	13	12	11	10	9	8
ARFData							
23	22	21	20	19	18	17	16
ARFData							
31	30	29	28	27	26	25	24
ARFData							

3-2-16 ITF/IRF Data Register

Index 48h
 Initial value 0000 0000h

In cases other than $\text{ISO011b}\checkmark$ in IsoMode, this register is used for isochronous transmission data writing. Data are written in the internal buffer for isochronous transmission. In the case of $\text{ISO011b}\checkmark$ this register is used for isochronous reception data reading and data are read from the internal buffer for asynchronous reception. In cases other than host 32-bit access, it is always necessary to write data in the Quadlet unit. When IsoMode= $\text{ISO011b}\checkmark$, this register is used for a packet to be set by the Isochronous Configuration Register-2. ResetITF/IRF is used when resetting the internal reception buffer from which data are read.

7	6	5	4	3	2	1	0
ITF/IRFData							
15	14	13	12	11	10	9	8
ITF/IRFData							
23	22	21	20	19	18	17	16
ITF/IRFData							
31	30	29	28	27	26	25	24
ITF/IRFData							

3-2-17 IRF Data Register

Index 4Ch
Initial value 0000 0000h

This register is used for isochronous reception data read-out. Data are read from the internal buffer for asynchronous reception. In cases other than host 32-bit access, it is always necessary to write data in the Quadlet unit. When IsoMode=ÉÇ011bÉÇ, this register is used for a packet to be set by the Isochronous Configuration Register-3. ResetIRF is used when resetting the internal reception buffer from which data are read.

7	6	5	4	3	2	1	0
IRFData							
15	14	13	12	11	10	9	8
IRFData							
23	22	21	20	19	18	17	16
IRFData							
31	30	29	28	27	26	25	24
IRFData							

3-2-18 Buffer Status and Control Register

Index 50h

Initial value 0000 0055h

This register is used for asynchronous transmission/ reception. It is used for the status control of internal buffer for isochronous transmission/reception and for the flush control for an asynchronous reception buffer.

7	6	5	4	3	2	1	0
	IRFEmpty	ITF/IRF Full	ITF/IRF Empty		ARFEmpty	ATFFull	ATFEmpty
15	14	13	12	11	10	9	8
	SelectDreq		DreqEn				ARFFlush
23	22	21	20	19	18	17	16
IRFcount							
31	30	29	28	27	26	25	24
							IRFcount

Bit 0 **ATFEmpty:** ATF Empty bit (R- Initial value: 1b)

0 = Indicating a condition that the buffer is not empty

1 = Indicating a condition that the buffer is empty

This bit indicates that the asynchronous transmission buffer being accessed from the ATFData register is empty.

Bit 1 **ATFFull:** ATF Full bit (R- Initial value: 0b)

0 = Indicating a condition that the buffer is not full

1 = Indicating a condition that the buffer is full

This bit indicates that the asynchronous transmission buffer being accessed from the ATF Data register is full.

Bit 2 **ARFEmpty:** ARF Empty bit (R- Initial value: 1b)

0 = Indicating a condition that the buffer is not empty

1 = Indicating a condition that the buffer is empty

This bit indicates that the asynchronous reception buffer being accessed from the ARF Data register is empty.

Bit 4 **ITF/IRFEmpty:** ITF/IRF Empty bit (R- Initial value: 1b)

0 = Indicating a condition that the buffer is not completely empty

1 = Indicating a condition that the buffer is completely empty

This bit is used for transmission in IsoMode in cases other than $\text{É}011\text{bÉ}$. It is also used for reception in the case of $\text{É}011\text{bÉ}$. It indicates that the isochronous buffer being accessed from the ITF/IRF Data register is empty.

Bit 5 **ITF/IRFFull:** ITF/IRF Full bit (R- Initial value: 0b)

0 = Indicating a condition that the buffer is not full

1 = Indicating a condition that the buffer is full

This bit is used for transmission in IsoMode in cases other than ISO_MODE_011b . It is also used for reception in the case of ISO_MODE_011b . It indicates that the isochronous buffer being accessed from the ITF/IRF Data register is full.

Bit 6 **IRFEmpty:** IRF Empty bit (R- Initial value: 1b)

0 = Indicating a condition that the buffer is not empty

1 = Indicating a condition that the buffer is empty

Bit 8 **ARFFlush:** ARF Flush bit (RW- Initial value: 0b)

0 = Normal condition

1 = Flushing effected

This bit is used to flush data if it is unnecessary for the host to read out the packet when one packet is being read from the asynchronous reception buffer to be accessed from the ARF Data register.

Bit 12 **DreqEn:** Dreq Enable bit (RW- Initial value: 0b)

0 = DREQ signal is left non-active at any time

1 = DREQ signal is turned active as the status of contents chosen by SelectDreq.

This bit is intended to make the DREQ signal valid.

Bit 14~13 **SelectDreq:** Select Dreq bit (RW- Initial value: 00b)

00 = This bit is reflected on the DREQ signal as the status being equivalent to that of the ATFFull bit for the buffer being accessed by the ATF Data register.

01 = This bit is reflected on the DREQ signal as the status being equivalent to that of the ATFEmpty bit for the buffer being accessed by the ATF Data register.

10 = This bit is reflected on the DREQ signal as the status being equivalent to that of the ITFFull bit in the transmission mode and that of IRFEmpty bit in the reception mode, for the buffer being accessed by the ITF/IRF Data register.

11 = This bit is reflected on the DREQ signal as the status being equivalent to that of the IRFEmpty bit for the buffer being accessed by the IRF Data register.

This register is used to determine what buffer status in the chip should be reflected on the DREQ signal.

Bit 24~16 **IRFcount** IRF count bit (R- Initial value: 00b)

This bit is used to indicate the data size in the Quadlet unit, stored in the buffer (IRF or ITF/IRF) chosen by the SelectDreq bit in the auto-mode.

3-2-19 Interrupt Register

Index 54h

Initial value 0000 0000h

By reading out data from this register, the host can know a variety of interrupt factors in MD8412. All bits in this register indicate with ÉÑ1ÉÜ that an interrupt factor has arisen.

7	6	5	4	3	2	1	0
CycleSeconds	CycleStart	CycleDone	CycleLost	CmdReset			
15	14	13	12	11	10	9	8
PhyInt	BusReset		PhyRegRcvd	AckErr	TCodeErr	HdrErr	SentRej
23	22	21	20	19	18	17	16
ATxEnd	IRFRxEnd	ITF/IRF RxEnd	ARxEnd	ITxEnd	ITFNoTx	IRFFlush	ITF/IRF Flush
31	30	29	28	27	26	25	24

Bit 3 CmdReset: Command Reset bit (R- Initial value: 0b)

This bit is set at ÉÑ1ÉÜ when a packet is received, addressed to the reset area in the CSR space.

Bit 4 CycleLost: Cycle Lost bit (R- Initial value: 0b)

If the MD8412 node is not of the Cycle Master, this bit is set at ÉÑ1ÉÜ when a CycleStart packet is received and the internal cycle timer is updated, but the next CycleStart packet cannot be received in 250Élsec by that cycle timer.

Bit 5 CycleDone: Cycle Done bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when a certain isochronous cycle is over.

Bit 6 CycleStart: Cycle Start bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when a new isochronous cycle is started.

Bit 7 CycleSeconds: Cycle Seconds bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when a cycle timer possessed by MD8412 has counted 1 second.

Bit 8 SentRej: Sent Reject bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when an asynchronous packet is received, but this packet cannot be completely received because of lack of a vacant space enough to accommodate the packet capacity in the receiving buffer, and a busy Acknowledge packet is returned from MD8412 to the source node.

Bit 9 HdrErr: Header Error bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ during reception of a packet, if the received packet contains an error header. In such a case, in isochronous reception, data transfer to that receiving buffer is not performed and this packet is

canceled.

Bit 10 TCodeErr: TCode Error bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ during transmission of a packet, if a code not supported by MD8412 is set in the TCode area of the packet header.

Bit 11 AckErr: Ack Error bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ for a transmitted asynchronous packet, if an Acknowledge packet returned from the destination node cannot be normally received.

Bit 12 PhyRegRcvd: PHY Register Received bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when data from PHY are stored in RegData after the issuing of a Read request toward the PHY register.

Bit 14 BusReset: Bus Reset bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when PHY is turned in bus reset mode.

Bit 15 PhyInt: Phy Interrupt bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when an interrupt factor is sent from PHY connected to MD8412.

Bit 16 ITF/IRFFlush: ITF/IRF Flush bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when MD8412 makes isochronous reception, but a packet routed to the IFT/IRF buffer cannot be normally received for the following reasons, thus causing the received data canceled:

- No vacant area for the received packet data in the isochronous reception buffer.
- CRC error present in packet header and pay-load area.
- No coincidence between the data length setting value in the packet header and the actual quantity of data in the pay-load area.

Bit 17 IRFFlush: IRF Flush bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when MD8412 makes isochronous reception, but a packet routed to the IRF buffer cannot be normally received for the following reasons, thus causing the received data canceled:

- No vacant area for the received packet data in the isochronous reception buffer.
- CRC error present in packet header and pay-load area.
- No coincidence between the data length setting value in the packet header and the actual quantity of data in the pay-load area.

Bit 18 ITNoTx: Isochronous No Transmit bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ during isochronous transmission by MD8412 in auto-mode, if this transmission cannot be accomplished after reception of the Cycle Start packet.

Bit 19 ITxEnd: Isochronous Transmit End bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when isochronous transmission is attempted by MD8412 in normal mode, and a group of packets has been completely transferred for different channels required to be transferred by ITGo.

Bit 20 ARxEnd: Asynchronous Receive End bit (R- Initial value: 0b)

Set at ÉÑ1ÉÜ when asynchronous reception is performed by MD8412 and data are stored in the ARF buffer.

Bit 21 ITF/IRFRxEnd: Isochronous Receive End (ITF/IRF) bit (R- Initial value: 0b)

Set at $\bar{E}N1\bar{E}U$ when isochronous reception is performed by MD8412 and data are stored in the IFT/IRF buffer.

Bit 22 **IRFRxEnd**: Isochronous Receive End (IRF) bit (R- Initial value: 0b)

Set at $\bar{E}N1\bar{E}U$ when isochronous reception is performed by MD8412 and data are stored in the IRF buffer.

Bit 23 **ATxEnd**: Asynchronous Transmit End bit (R- Initial value: 0b)

Set at $\bar{E}N1\bar{E}U$ when asynchronous transmission is performed by MD8412 and an Ack code returned from the destination is received upon completion of transmission operation. This bit is also set at $\bar{E}N1\bar{E}U$ when retry operation is performed and its retry phase is completed, or when AckErr is set in the middle of operation.

3-2-20 Interrupt Mask Register

Index	58h
Initial value	0000 0000h

When each Interrupt factor in the Interrupt register need not be reflected on the INT# signal, it is masked by this register. Arrangements of this register are the same as those for the Interrupt register. Each bit is masked by setting at $\bar{E}N1\bar{E}U$.

3-2-21 TGo Register

Index 5Ch
Initial value 0000 0000h

For transmission of an asynchronous packet and transmission of an isochronous packet in normal IsoMode, $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$ is set at the TGo register in this register to inform the MD8412 of packet transmission. The host transmits the sending packet to the internal buffer of MD8412, and then sets up this TGo register. With $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$ of this TGo register, the MD8412 begins to send a packet, assuming that one packet consists of data written in the buffer by then. In isochronous transmission, however, actual transmission of data begins with CycleStart shortly after the issuing of ITGo. According to the Go command issued, the ATBusy bit is turned $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$ or asynchronous transmission and the ITBusy bit is turned $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$ for isochronous transmission. By this operation, the host can identify that the MD8412 has started transmission operation. The timing to permit the next TGo issuing is after the ATBusy bit is turned $\overline{\text{EN0}}\overline{\text{E}}\overline{\text{U}}$ for asynchronous transmission and the ITBusy bit is turned $\overline{\text{EN0}}\overline{\text{E}}\overline{\text{U}}$ for isochronous transmission. Even when TGo is issued while ATBusy or ITBusy is $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$, the MD8412 disregards it. Even when $\overline{\text{EN0}}\overline{\text{E}}\overline{\text{U}}$ is written in this register, such an attempt is invalid.

7	6	5	4	3	2	1	0
					ITStart	ITGo	ATGo
15	14	13	12	11	10	9	8
23	22	21	20	19	18	17	16
31	30	29	28	27	26	25	24

Bit 0 **ATGo:** AT Go bit (RW- Initial value: 0b)

By writing $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$ in this register, the MD8412 is informed of the start of asynchronous packet transmission.

Bit 1 **ITGo:** IT Go bit (RW- Initial value: 0b)

By writing $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$ in this register, the MD8412 is informed of the start of isochronous packet transmission. This bit is valid only if IsoMode is normal.

Bit 2 **ITStart:** IT Start bit (RW- Initial value: 0b)

By writing $\overline{\text{EN1}}\overline{\text{E}}\overline{\text{U}}$ in this register, the MD8412 is informed of the start of isochronous packet transmission in auto-mode. By writing $\overline{\text{EN0}}\overline{\text{E}}\overline{\text{U}}$ therein, the MD8412 can know the stoppage of operation. This bit is valid only if IsoMode is Auto. The relationship with the ITSTART signal terminal is logical OR.

3-3 Registers

Register	Adrs	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Version	00h	Version																Revision																				
Control	04h				DMAWidth																												ReceiveEn	TransmitEn				
Node Identification	08h	IDValid																BusNumber						NodeNumber														
Reset	0Ch																															ResetDMA	ResetRx	ResetTrans	ResetIRF	ResetARF	ResetITF/IRF	ResetATF
Asynchronous	10h								ARcvBufferSize												ATotalSize																	
Isochronous	14h								IRcvBufferSize												ITotalSize																	
Packet Control	18h																																					
Diagnostic Status	1Ch							ITBusy	ATBusy						ARStatus			RetryTimeOut		Ack Status	ATAck																	
Phy Control	20h																		RegRcvd	RdReg	WrReg	RegAddr			RegData													
ATRetries	24h																																					
Cycle Timer	28h	CycleSeconds						CycleCount						CycleOffset																								
BandWidth Control	2Ch					ITLength																																
Isochronous Configuration 1	30h	Tag	Channel												Speed	Sync		StartSync			StopSync														IsoRxEn	SyncEn		
Isochronous Configuration 2	34h	Tag	Channel												Speed	Sync		StartSync			StopSync														IsoRxEn	SyncEn		
Isochronous Configuration 3	38h	Tag	Channel												Speed	Sync		StartSync			StopSync														IsoRxEn	SyncEn		
Isochronous Configuration 4	3Ch	Tag	Channel												Speed	Sync		StartSync			StopSync														IsoRxEn	SyncEn		

Table 3-4-1 Registers 1

Register	Adrs	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
ATF Data	40h	ATF Data																																						
ARF Data	44h	ARF Data																																						
ITF/IRF Data	48h	ITF/IRF Data																																						
IRF Data	4Ch	IRF Data																																						
Buffer Status and Control	50h										IRFcount									SelectDreq		DreqEn								ARFlush			IRFEmpty	ITF/IRFEmpty	ITF/IRFEmpty			ARFEmpty	ATFFull	ATFEmpty
Interrupt	54h										ATxEnd	IRFRxEnd	ITF/IRFRxEnd	ARxEnd	ITxEnd	ITNoTx	IRFFlush	ITF/IRFFlush	PhyInt	BusReset		PhyRegRcvd	AckErr	TCodeErr	HdrErr	SendRej	CycleSeconds	CycleStart	CycleDone	CycleLost	CmdReset									
Interrupt Mask	58h										ATxEnd	IRFRxEnd	ITF/IRFRxEnd	ARxEnd	ITxEnd	ITNoTx	IRFFlush	ITF/IRFFlush	PhyInt	BusReset		PhyRegRcvd	AckErr	TCodeErr	HdrErr	SendRej	CycleSeconds	CycleStart	CycleDone	CycleLost	CmdReset									
TGo	5Ch																															ITStart	ITGo	ATGo						

Table 3-4-2 Registers 2

4 Data Format

4-1 Asynchronous

4-1-1 Quadlet Transmit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														spd		tLabel						rt		tCode				priority			
destinationID																destinationOffset-H															
destinationOffset-L																															
quadlet data (for write request and read response)																															

Table 4-1-1 Quadlet Transmit format (Asynchronous)

spd : speed field

This field is used to designate the transfer speed. Refer to Table 4-6-6 regarding setting values.

tLabel : Transaction label field

This field is used to define a unique tag for each transferred transaction. The tLabel sent for requesting is used as a transaction label for correct response. The values used are valid in the range of 0h~Fh.

rt : retry field

This field is used to define whether this packet is in the middle of making a retry. The retry protocol is followed by the destination node. Refer to Table 4-6-1 regarding setting values.

tCode : Transaction code field

This field is used to set up a transaction code. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.

priority : priority field

This field is valid in the back plane environment. Therefore, the MD8413 is required to set up 0000b, without fail.

destinationID : destination ID field

This field is used to set up destination bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

destinationOffset : destination Offset Address field

This field is used to define the lower 48-bit address of the destination node for the requested packet. The setting value need be defined in the quadlet unit in the case of a read request for quadlet data and a write request for quadlet data.)

quadletData:quadlet data field
This field is used to set up actual transfer data (1 Quadlet).

4-1-2 Block Transmit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														spd		tLabel					rt		tCode					priority			
destinationID															destinationOffset-H																
destinationOffset-L																															
dataLength															extended_tCode																
block data quadlet 1																															
other block data quadlets																															
													padding(if necessary)																		

Table 4-1-2 Block Transmit format (Asynchronous)

- spd

: speed field

This field is used to designate the transfer speed. Refer to Table 4-6-6 regarding setting values.
- tLabel

:Transaction label field

This field is used to define a unique tag for each transferred transaction. The tLabel sent for requesting is used as a transaction label for correct response. The values used are valid in the range of 0h~FFf.
- rt

: retry field

This field is used to define whether this packet is in the middle of making a retry. The retry protocol is followed by the destination node. Refer to Table 4-6-1 regarding setting values.
- tCode

: Transaction code field

This field is used to set up a transaction code. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.
- priority

: priority field

This field is valid in the back plane environment. Therefore, the MD8413 is required to set up 0000b, without fail.
- destinationID

: destination ID field

This field is used to set up destination bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.
- destinationOffset

:destination Offset Address Field

This field is used to define the lower 48-bit address of the destination node for the requested packet. The setting value need be defined in the quadlet unit in the case of a read request for quadlet data and a write request for quadlet data.

dataLength : data length field

This field is used to set up data length for the blockData field. The maximum value of the setting value depends on that of the speed field. Refer to Table 4-6-4 regarding details.

extended_tCode : extended transaction code field

This field is used to define the extension tCode. This extended_tCode becomes valid only if tCode is ÉÅlock requestÉÇ or ÉÅlock responseÉÇ. For other tCodes, 0000h must be set in this register. Refer to Table 4-6-5 regarding details.

blockData : block data field

This field is used to set up actual transfer data. If the dataLength field is not defined with a multiple of 4, this field need be filled with 00h to complete it in the Quadlet unit.

4-1-3 Quadlet Receive

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
destinationID																tLabel				rt		tCode				priority					
sourceID																destinationOffset-H															
destinationOffset-L																															
quadlet data (for write request and read response)																															
																spd															ackSent

Table 4-1-3 Quadlet Receive format (Asynchronous)

destinationID : destination ID field

The destination bus of this packet and the node ID are saved in this field. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

tLabel : Transaction label field

This field is used to define a unique tag for each transferred transaction.

rt : retry field

This field is used to define whether this packet having been sent is in the middle of making a retry. Refer to Table 4-6-1 regarding setting values.

tCode : Transaction code field

A transaction code is saved in this field. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.

- priority

: priority field

This field is valid in the back plane environment. Therefore, the MD8413 is required to save 0000b, without fail.
- sourceID

: source ID field

This field is used to save the source bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.
- destinationOffset

:destination Offset Address field

This field is used to save the lower 48-bit address of the destination node for the requested packet.
- quadletData

: quadlet data field

This field is used to save transferred data.
- spd

: speed field

This field is used to designate the received speed. Refer to Table 4-6-6 regarding setting values.
- ackSent

: ackSent field

This field saves the Ack code returned as an acknowledge signal after this packet has been received. Refer to Table 4-6-7 regarding details.

4-1-4 Block Receive

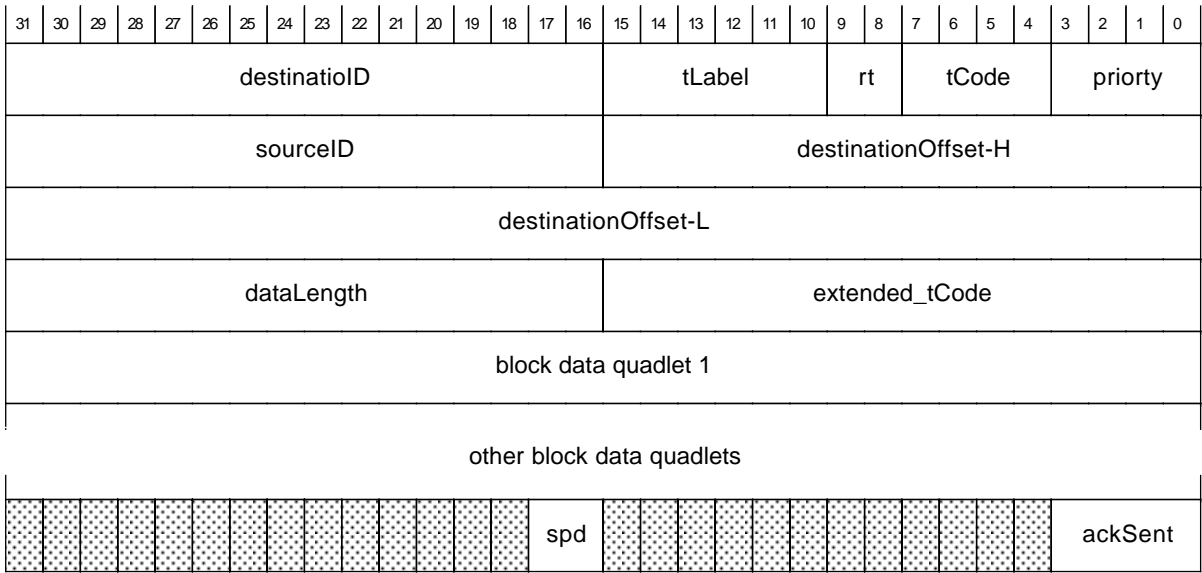


Table4-1-4 Block Receive format (Asynchronous)

- destinationID

: destination ID field

The destination bus of this packet and the node ID are saved in this field. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.

- tLabel** : Transaction label field
This field is used to define a unique tag for each transferred transaction.
- rt** : retry field
This field is used to define whether this packet having been sent is in the middle of making a retry.
Refer to Table 4-6-1 regarding setting values.
- tCode** : Transaction code field
A transaction code is saved in this field. The transaction code is used to define the packet type. Refer to Table 4-6-2 regarding setting values.
- priority** : priority field
This field is valid in the back plane environment. Therefore, 0000b is always saved.
- sourceID** : source ID field
This field is used to save the source bus and node ID. The upper 10 bits out of the length of 16 bits are used to set up the destination bus ID and the lower 6 bits are used to set up the destination physical ID. Some figures in the setting value may have special meanings. Refer to Table 4-6-3 regarding details.
- destinationOffset** : destination Offset Address field
This field is used to save the lower 48-bit address of the destination node for the requested packet.
- dataLength** : data length field
This field is used to set up data length for the blockData field.
- extended_tCode** : extended transaction code field
This extended_tCode becomes valid only if tCode is ÉÅlock requestÉÇ or ÉÅlock responseÉÇ. For other tCodes, 0000h is saved in this register.
- blockData** : block data field
The transferred data are saved in this field.
- spd** : speed field
This field is used to designate the received speed. Refer to Table 4-6-6 regarding setting values.
- ackSent** : ackSent field
This field saves the Ack code returned as an acknowledge signal after this packet has been received.
Refer to Table 4-6-7 regarding details.

4-2 Isochronous

4-2-1 For Normal Mode

4-2-1-1 Transmit

Table4-2-1 Block Transmit format (Isochronous:normal)

dataLength	: data length field
This field is used to set up data length for the blockData field.	
tag	: tag field
This field is used to set up Tag for Isochronous transmit.	
channel	: channel field
This field is used to set up Channel number for Isochronous transmit.	
spd	: speed field
This field is used to designate the transfer speed.	
sy	: sync field
This field is used to set up Sync data for Isochronous transmit.	
Isochronous Data	: Isochronous data field
This field is used to set up actual transfer data. If the dataLength field is not defined with a multiple of 4, this field need be filled with 00h to complete it in the Quadlet unit.	

4-2-1-2 Receive

Table4-2-2 Block Receive format (Isochronous:normal)

dataLength	: data length field
This field is used to designate the received data length for the blockData field.	
tag	: tag field
This field is used to designate the received Tag data.	
channel	: channel field
This field is used to designate the received Channel number.	
sy	: sync field
This field is used to designate the received Sync data.	
tCode	: Transaction code field
A transaction code is saved in this field. The transaction code values is 00h~03h.	

isochronous Data : Isochronous data field
The transferred data are saved in this field.

4-2-2 For Auto Mode

4-2-2-1 Transmit

Table4-2-3 Block Transmit format (Isochronous:auto)

Isochronous Data : Isochronous data field
This field is used to set up actual transfer data. If the dataLength field is not defined with a multiple of 4, this field need be filled with 00h to complete it in the Quadlet unit.

4-2-2-2 Receive

Table4-2-4 Block Receive format (Isochronous:auto)

isochronous Data : Isochronous data field
The transferred data are saved in this field.

4-3 Snoop

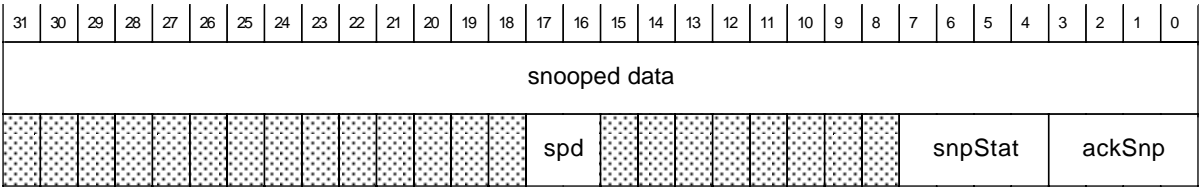


Table4-3-1 Snoop Receive format

snoopedData : snooped data field
Third field is used to save the snooped data.

spd : speed field
This field is used to save the received speed. Refer to Table 4-6-6 regarding setting values.

snpStat : snooped Status field
This field saves the Ack code to be returned as a status (acknowledge) signal after this packet has been received. Actually, however, the Ack code is not returned. Refer to Table 4-6-7 regarding details.

ackSnp : snooped ack-code field
This field saves the received Ack code. In other words, a node that has received this packet corresponds to the returned Ack code.

4-4 SelfID Packet

After the identification quadlet data shown in Table 4-4-1 have been saved, an actual SelfID packet is saved.

This operation is completed with the last quadlet ID data as shown in Table 4-4-4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1110b				0	0	0	0

Table4-4-1 SelfID Packet Receive format(first quadlet)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	phy_ID						0	L	gap_cnt						sp	del	C	pwr			p0	p1	p2	i	m					
logical inverse of first quadlet																															

Table4-4-2 SelfID Packet Receive format(SelfID Packet #0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	phy_ID							1	n	rsv	pa	pb	pc	pd	pe	pf	pg	ph	r	m										
logical inverse of first quadlet																															

Table4-4-3 SelfID Packet Receive format(SelfID Packet #1, #2, & #3)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ackSent						

Table4-4-4 SelfID Packet Receive format(last quadlet)

	n	pa	pb	pc	pd	pe	pf	pg	ph
pkt #1	0	p3	p4	p5	p6	p7	p8	p9	p10
pkt #2	1	p11	p12	p13	p14	p15	p16	p17	p18
pkt #3	2	p19	p20	p21	p22	p23	p24	p25	p26

Table4-4-5 SelfID Packet Receive format(pn)

phy_ID : physical_ID field

A node ID of the PHY chip used to send this packet.

L : link_active field

0 = LINK is not active.

1 = Active link and transaction layer are present in this node.

gap_cnt : gap_count field

A present value of the PHY_CONFIGURATION.gap_count field for this node is saved.

sp : PHY_SPEED field

00 = 98.304Mbps
 01 = 98.304 and 196.608Mbps
 10 = 98.304 and 196.608 and 393.216Mbps
 11 = Reserved

Available speeds are saved.

del : PHY_DELAY field

00 = 144ns or less (~14/BASE_RATE)

01~11= Reserved.

The delay time of the repeater in the worst case is saved.

C : CONTENDER field

When this field is set and the link_active field is also set, this node indicates that it can be a bus or isochronous resource manager.

pwr : POWER_CLASS field

000 = The node does not require power supply.

001 = The node does has its own power supply that can feed a minimum of 15W.

010 = The node does has its own power supply that can feed a minimum of 30W.

011 = The node does has its own power supply that can feed a minimum of 45W.

100 = The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 2W to enable the LINK and upper layers.

101 = The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 2W to enable the LINK and upper layers.

110 = The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 5W to enable the LINK and upper layers.

111 = The node consumes a maximum of 1W of power from the cable. In addition, it consumes a maximum of 9W to enable the LINK and upper layers.

p0 ... p26 : NORT,child[NPORT],connected[NPORT]field

11 = Connected to the parent node.

10 = Connected to the parent node.

01 = Not connected to another PHY.

00 = This PHY is not offered.

The port status is shown.

i : initiated_reset field

If it is set, this node has issued present bus reset.

m : more_packets field

If it is set, this node indicates that another SelfID packet of this node is closely following.

n : Extended field

An extension SelfID packet sequence number (value from 0~2).

r,rsv : reserved field

Reserved.

4-5 PHY Control Packet

To send a PHY control packet, the first quadlet of data shown in Table 4-5-4 is saved in the ATF buffer, and the PHY Control Packet specified by 1394 is then saved. In this case, it is necessary to save the PHY Control Packet data together with the reversal data.

In actual transmission, the first quadlet is not sent and the PHY Control packet only is sent. Refer to the Draft regarding details.

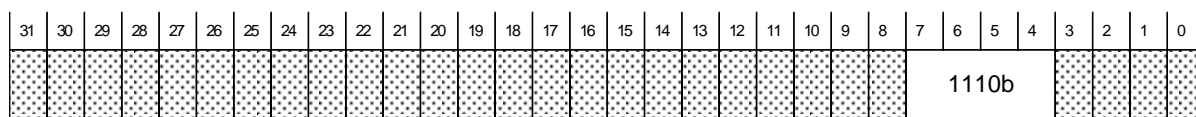


Table 4-5-1 PHY control packet format(first quadlet)

4-6 Code

The codes used for packet formatting specified by 1394 are shown. Refer to the 1394 Draft for details of each code.

Code	Name
00b	retry_1
01b	retry_X
10b	retry_A
11b	retry_B

Table 4-6-1 List of Retry code

Code	Name	Code	Name
0h	write request for data quadlet	8h	cycle start
1h	write request for data block	9h	lock request
2h	write response	Ah	isochronous data block
3h	reserved	Bh	lock response
4h	read request for data quadlet	Ch	reserved
5h	read request for data block	Dh	reserved
6h	read response for data quadlet	Eh	reserved
7h	read response for data block	Fh	reserved

Table 4-6-2 List of Transaction code (tCode)

destination bus_ID	destination node_ID	Contents
0~3FEh	0~3Eh	Transferred to the node defined by bus_ID and node_ID.
3FFh	0~3Eh	Transferred to the node defined by node_ID in local bus.
0~3FEh	3Fh	Broadcast transfer to the bus defined by bus_ID.
3FFh	3Fh	Broadcast transfer in local bus.

Table 4-6-3 List of Bus Number / Node Number

Data rate	Maximum payload size (byte)
100Mbps	512
200Mbps	1024
400Mbps	2048

Table 4-6-4 List of Data Length (Data Length)

Code	Name
0000h	reserved
0001h	mask_swap
0002h	compare_swap
0003h	fetch_add
0004h	little_add
0005h	bounded_add
0006h	wrap_add
0007h	vender-dependent
0008h - FFFh	reserved

Table 4-6-5 List of Extension Transaction Code(Extend tCode)

Code	Speed
00b	100Mbps
01b	200Mbps
10b	400Mbps
11b	reserved

Table 4-6-6 List of Speed Codes (spd)

Code	Name
0h	reserved
1h	ack_complete
2h	ack_pending
3h	reserved
4h	ack_busy_X
5h	ack_busy_A
6h	ack_busy_B
7h	reserved
8h	reserved
9h	reserved
Ah	reserved
Bh	reserved
Ch	reserved
Dh	ack_data_error
Eh	ack_type_error
Fh	reserved

Table 4-6-7 List of Acknowledge Codes (Ack)

5 Functional Description

5-1 Host interface

Control of MD8412 and transmission/reception data transfer are all conducted through host interface. Timing for host interface signals is controlled by the respective signals of CS#, RD#, WR#, HA(6:0), and HD(31:0) for asynchronous transfer as SRAM interface.

The internal register and the P1394 packet format are basically in the bus width of 32 bits. The MD8412 can, however, control the bus width so that it can be connected to an MPU that has an 8-bit, 16-bit, or 32-bit data bus.

5-1-1 Register access timing

As shown in Figure 5-1-1, access to a register is effected through the SRAM-like asynchronous bus.

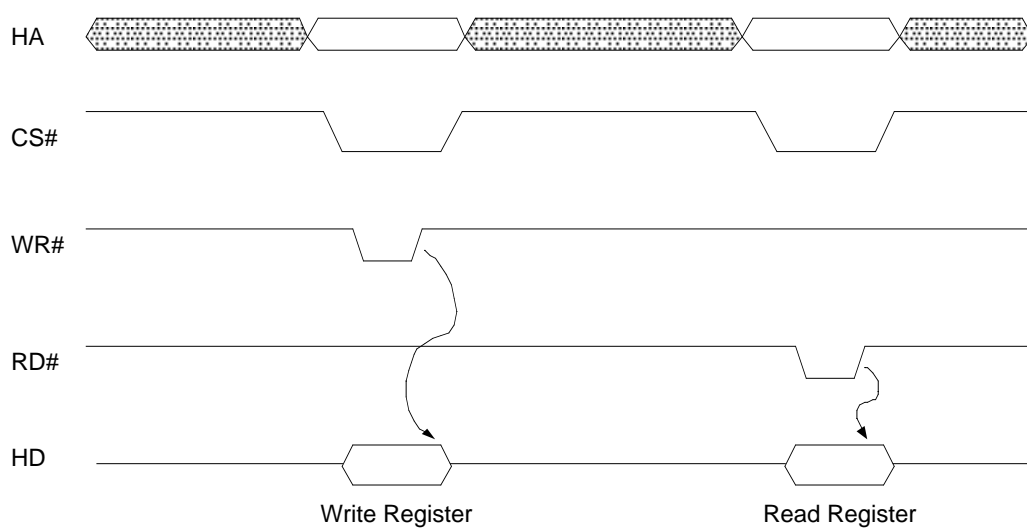


Figure 5-1-1 Host Access Timing

5-1-2 Host bus width

As shown in Table 5-1-1, a valid bit accessed from the host is determined by UWE#, UBE#, HA1, and HA0. Therefore, if controlling the MD8412 with an 8-bit MPU, the bit is fixed at UWE#=1 and UBE#=1 and the address and data bus are connected to HA(6:0) and HD(7:0). In this manner, direct control is possible.

UWE#	UBE#	HA1	HA0	access	Valid Host Bus	Buffer Bit Position
0	0	0	0	quadlet	31 - 0	31 - 0
1	0	0	0	word	15 - 0	31 - 16
1	0	1	0	word	15 - 0	15 - 0
1	1	0	0	byte	7 - 0	31 - 24
1	1	0	1	byte	7 - 0	23 - 16
1	1	1	0	byte	7 - 0	15 - 8
1	1	1	1	byte	7 - 0	7 - 0

Table 5-1-1 Valid Host Data Bus Accessed from the Host

For reading/writing in the byte unit with an 8-bit MPU, it is always necessary to do it in the unit of 4 bytes. For a 16-bit MPU, this must be done in the unit of 2 words. The register access normally operates when an ordinary address is specified and writing/reading is effected there. When performing writing/reading with transmission/reception buffer in the MD8412, data are stored in turn in the buffer, starting with an upper area as shown in Table 5-1-2. The same thing can be said for DMA transfer. The first one byte is written/read-out from the upper area. If the Little-endian bit is set at 1 with a 16- or 32-bit width, bytes are rearranged for buffer writing/reading, as shown in Table 5-1-2.

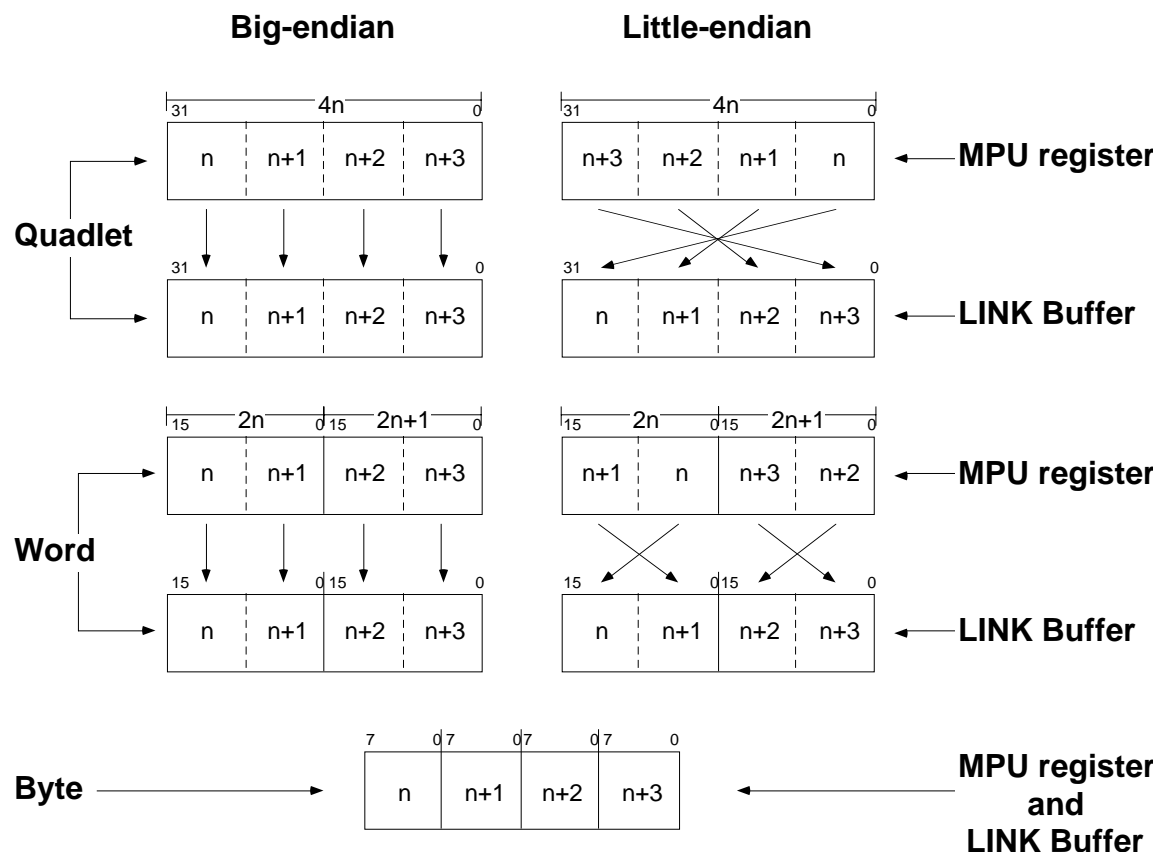


Table 5-1-2 Little / Big Endian Mode

5-1-3 DMA transfer

The MD8412 supports the DMA transfer functions to assure the method of data transfer with the transmission/reception buffer. The DMA mode is supported only that the DMA service request signal (DREQ) is of a level sense. Only one objective buffer for DMA transfer can be selected with the SelectDreq bit. Whether the DREQ signal should be made valid or not is controlled by the DreqEn bit. For DreqEn=1, the DREQ signal is valid, Table 5-1-3 shows the assert/negate conditions of the DREQ signal. For DreqEn=0, the DREQ signal always stays in the negate state. When transferring the transmission data, necessary data size is defined at the external DMAC and then data transfer is effected. Since then, DMA transfer is effected by setting DreqEn at 1 and issuing a DREQ request toward the DMAC. When transferring the reception data to the host side, the data length is read first and its value is set at the DMAC then execute the DMAC. Since then, DMA transfer is effected by setting DreqEn at 1 and issuing a DREQ request toward the DMAC.

SelectDreq Bit	Destination Buffer	DREQ Assert Condition	DREQ Negate Condition
00b	ATF	When ATF buffer is not full.	When ATF buffer is full (ATFFull='1')
01b	ARF	When data remain in ARF buffer.	When ARF buffer is full (ARFFull='1')
10b	ITF / IRF	When ITF buffer is not full.	When ITF buffer is full (ITFFull='1')
11b	IRF	When data remain in IRF buffer.	When IRF buffer is full (IRFFull='1')

Table 5-1-3 DREQ Signal Assert / Negate Conditions

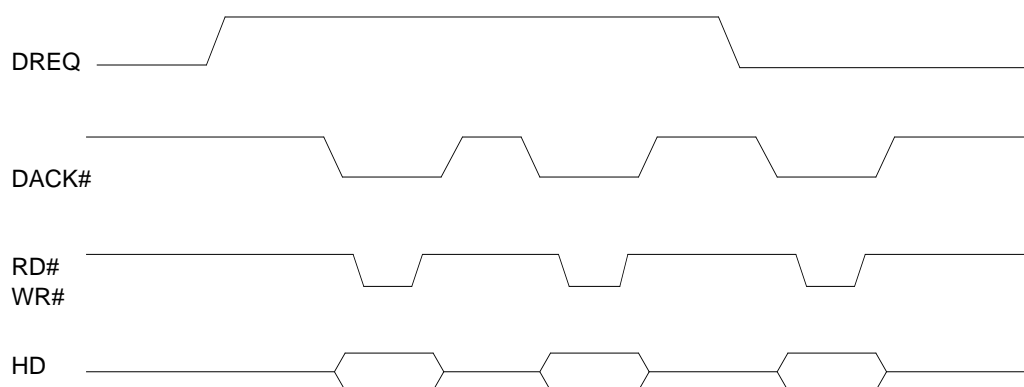


Figure 5-1-1 DMA Transfer Timing

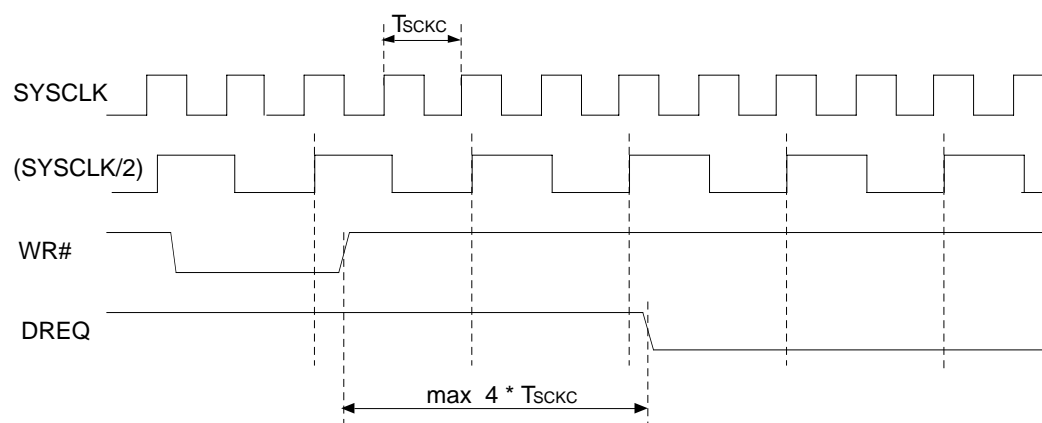


Figure 5-1-2 DREQ Negate Timing(WR#)

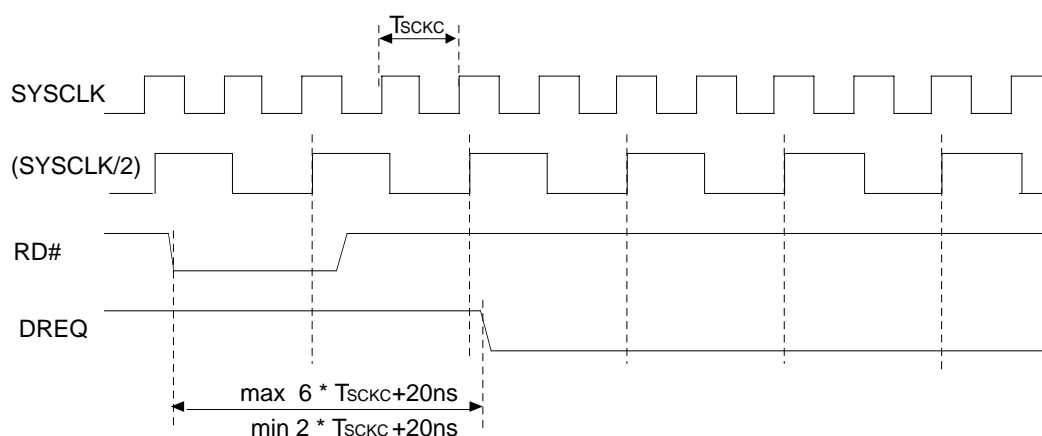


Figure 5-1-3 DREQ Negate Timing(RD#)

5-1-3 Interrupt processing

As a means of announcement to the host regarding the interrupt factor defined by the Interrupt register and the Interrupt Mask register, the MD8412 is provided with an INT# signal. This INT# signal is asserted under the condition that logical OR is established for the Interrupt factor not masked at the Interrupt Mask register with active low. Regarding the negate condition, all bits are cleared to 0 by reading them out from the Interrupt register.

5-2 PHY-chip interface

Interface with the PHY-chip is established with the SYSCLK, LREQ, D(7:0), CTL(1:0) signals. For connection with the PHY-chips that have various maximum speeds, the D(7:0) signal is used to select 100Mbps, 200Mbps, and 400Mbps. Connection with a 100Mbps PHY chip is made by D(1:0), that with a 200Mbps PHY-chip is made by D(3:0), and that with a 400Mbps PHY-chip is made by D(7:0) to enable communication.

5-2-1 Connecting method

Regarding the method of connection with PHY-chips, the MD8412 is designed to support DC connections only. Therefore, the method of connection is as shown in Figure 5-2-1.

Connection with the MD8412, a 200Mbps PHY-chip, is possible by making a connection between the lower 4 bits of the D(7:0) terminal and the MD8401. (See Figure 5-2-2)

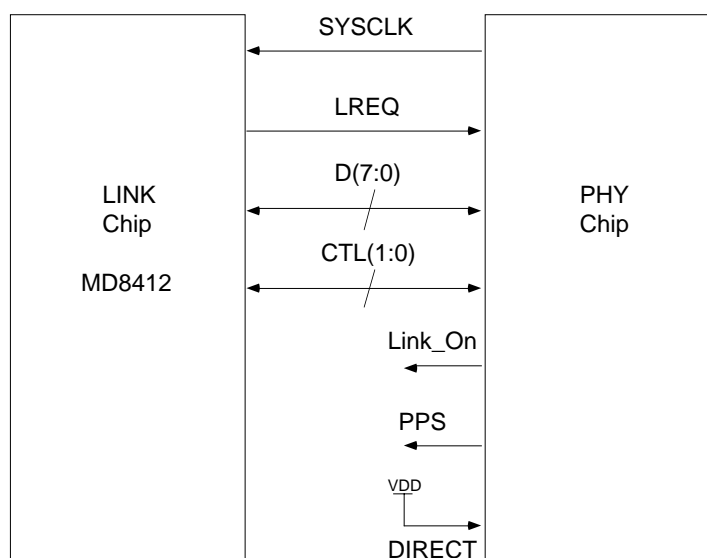


Figure 5-2-1 Connection between MD8412 and PHY-Chip

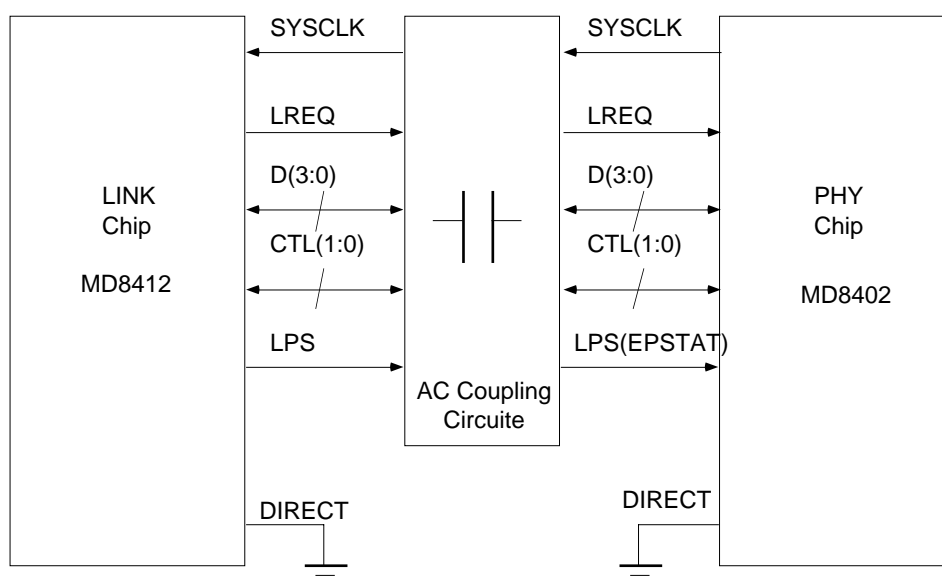


Figure 5-2-2 Connection between MD8412 and MD8402

5-2-2 PHY-chip control

To control the PHY-chip, the MD8412 employs communication means defined by the following 4 types of operation modes. Each operation mode is defined according to the condition of CTL(1:0) terminal.

CTL[0:1]	Operation	Contents
00b	Idle	Idle condition and nothing is operating (Default mode)
01b	Status	Status information transferred from PHY-chip
10b	Receive	Contents of received packet transferred from PHY-chip
11b	Transmit	PHY-LINK bus controlled for MD8411 to transfer a transmission packet to PHY-chip

Table 5-2-1 PHY-Chip Control Mode 1

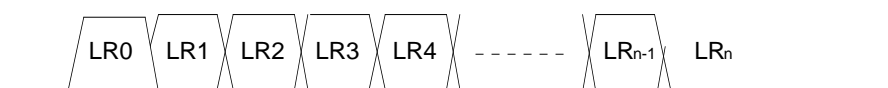
After control of the PHY-LINK bus has been enabled in the above Transmit mode, the operation mode shown in Table 5-2-2 is valid.

CTL[0:1]	Operation	Contents
00b	Idle	PHY-LINK bus released upon completion of transfer by MD8411
01b	Hold	- Bus held for MD8411 transfer until definition of data - MD8411 requesting for another packet sending without arbitration
10b	Transmit	Data of a transmission packet transferred to PHY-chip
11b	Reserved	Reserved

Table 5-2-2 PHY-Chip Control Mode 2

5-2-3 Request

As a request to access a register of the PHY-chip or a PHY-LINK bus, MD8412 sends a short serial stream to the LREC terminal. The stream involves information about the type requested, speed of the packet transferred, and the reading/writing command.



LRn = LREQn

Figure 5-2-3 LREQ Stream

5-2-3-1 LREQ

A request for PHY-LINK bus is placed in LREQ by a format with the length of 7 bits as shown in Table 5-2-3.

Bit(s)	Type	Contents
0	Start Bit	Showing the start of transfer. '1' is always transferred.
1-3	Request Type	Indicating a requested type as specified in Table 5-2-6.
4-5	Request Speed	Indicating the transfer speed of the requesting PHY-chip.
6	Stop Bit	Showing the end of transfer. '0' is always transferred.

Table 5-2-3 Request Format

LREQ[4:5]	Data Rate
00	100Mbps
01	200Mbps
10	400Mbps
11	>400Mbps

Table 5-2-4 Speed Format

A request for PHY-chip register read-out is placed in LREQ by a format with the length of 9 bits as shown in Table 5-2-5. A request for PHY-chip register writing is placed in LREQ by a format with the length of 17 bits as shown in Table 5-2-6.

Bit(s)	Type	Contents
0	Start Bit	Showing the start of transfer. '1' is always transferred.
1-3	Request Type	Indicating a requested type as specified in Table 5-2-6.
4-7	Address	Indicating register address of the read-out PHY-chip.
8	Stop Bit	Showing the end of transfer. '0' is always transferred.

Table 5-2-5 Read Register Format

Bit(s)	Type	Contents
0	Start Bit	Showing the start of transfer. '1' is always transferred.
1-3	Request Type	Indicating a requested type as specified in Table 5-2-6.
4-7	Address	Indicating register address of the writing-in PHY-chip.
8-15	Data	Indicating register data of the writing-in PHY-chip.
16	Stop Bit	Showing the end of transfer. '0' is always transferred.

Table 5-2-5 Write Register Format

LREQ[1:3]	Type	Contents
000	ImmReq	Immediate request
001	IsoReq	Isochronous request
010	PriReq	Priority request
011	FairReq	Fair request
100	RdReg	Reading out the contents of the set register
101	WrReg	Writing in the set register
110,111	Reserved	Reserved

Table 5-2-6 Request Type

5-2-4 Transfer

5-2-4-1 Status Request

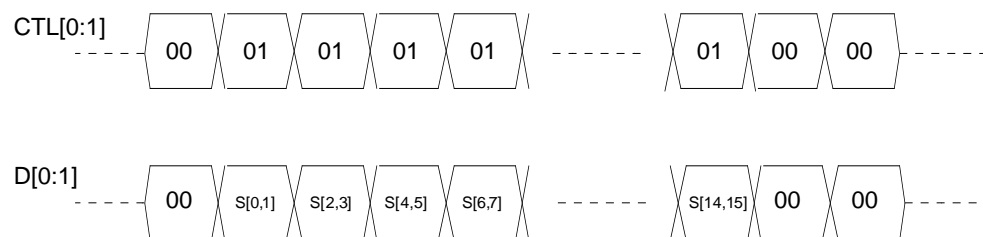


Figure 5-2-4 Status Request

Bit(Sn)	Type	Contents
0	Arbitration Reset Gap	Detection of arbitration Reset Gap
1	Fair Gap	Detection of Fair Gap
2	Bus Reset	Detection of Bus Reset
3	Phy Interrupt	Requesting the host for interrupt
4-7	Address	Address of the status-returning PHY register
8-15	Data	Status data

Table 5-2-7 Status Request Format

5-2-4-2 Transmit

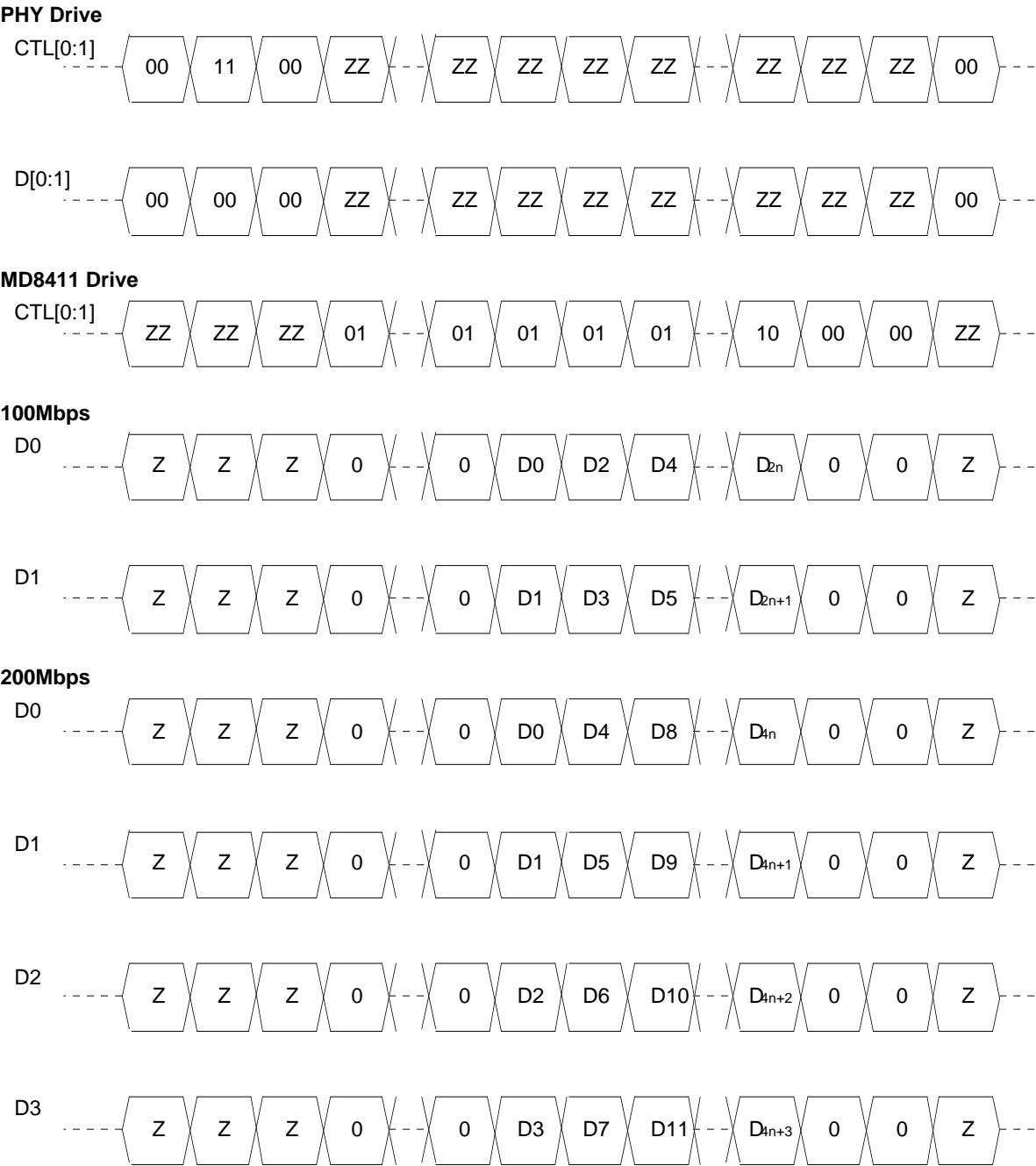
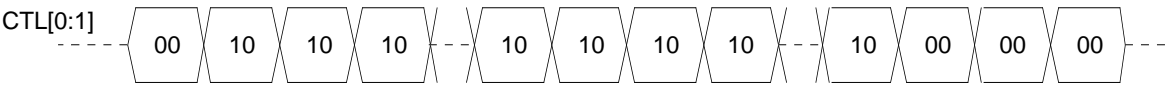


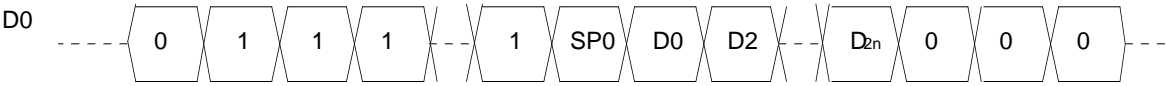
Figure 5-2-5 Transmit

5-2-4-3 Recwive

PHY Drive



100Mbps



200Mbps

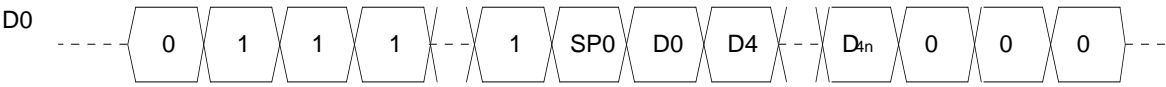


Figure 5-2-6 Receive

SP[0:7]	Data Rate
00xxxxxx	100Mbps
0100xxxx	200Mbps
01010000	400Mbps

Figure 5-2-7 Speed Code (SP[0:7])

5-3 Buffer access

5-3-1 Buffer configuration

The MD8412 incorporates a memory buffer with a total capacity of 2K-bytes in 512x32word configuration. To achieve rate absorption in terms of host access rate and serial bus transfer rate, the buffer is temporarily used between host bus and transmitter.

The buffer control block of MD8412 divides this buffer into a maximum of 4 blocks, and control is effected in the unit of divided sub-buffer.

Two blocks are assigned to asynchronous transmission and reception. (Referred to as ATF for asynchronous transmission buffer and ARF for asynchronous reception buffer)

When performing isochronous transmission or reception, the relevant buffers are assigned to the remaining two blocks. According to the contents of IsoMode setting register in the control register, however, combination of these two blocks is defined if they are to be used for transmit/receive, or receive/receive, or receive only. In the Isochronous mode other than IsoMode=011b or 101b, two sub-buffers are assigned for isochronous transmission and reception, respectively. When IsoMode=011b, two isochronous channels are limited to reception only, and hence isochronous transmission is impossible to achieve. When IsoMode =101b, only one sub-buffer for receive.

For these reasons, one of the two sub-buffers is changed over for isochronous reception when isochronous transfer is attempted, and the other is changed over for transmission and reception through IsoMode setting. (Referred to as ATF/IRF for asynchronous transmission/isochronous reception buffer and IRF for isochronous reception buffer hereafter)

>From the host, access is made to ATF from the ATF register, ARF from the ARF register, ITF/IRF from the ITF/IRF register, and ITF/IRF from the ITF/IRF register.

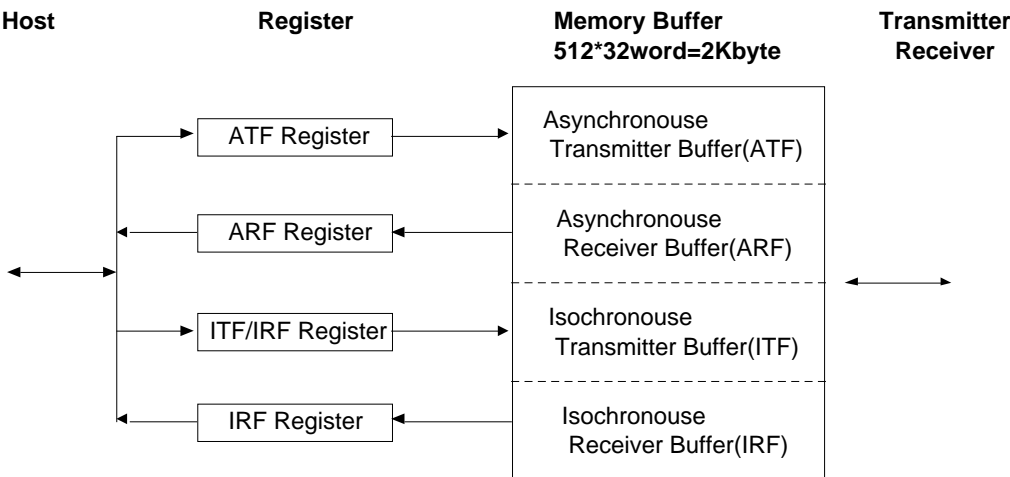


Fig. 5-3-1 Buffer Assignment in Cases Other than IsoMode=011b

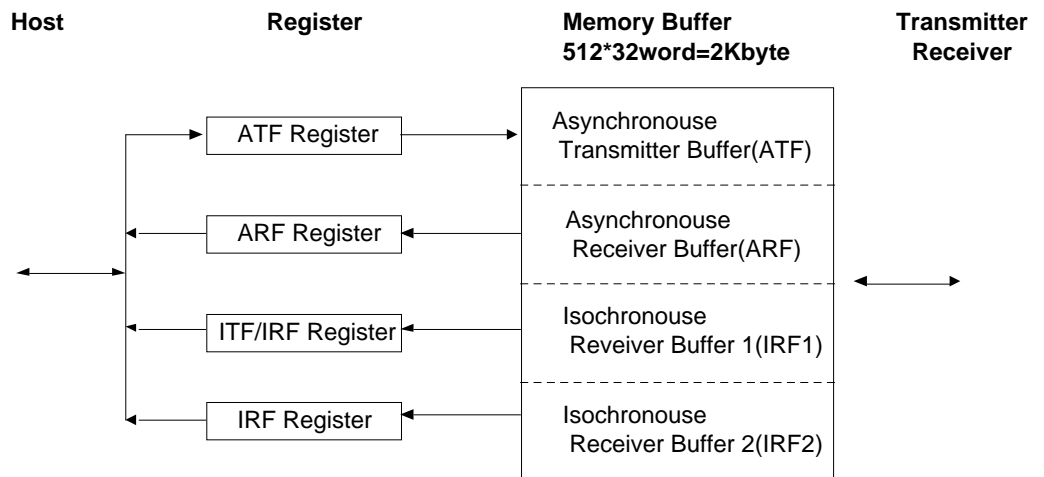


Fig. 5-3-2 Buffer Assignment in the Case of IsoMode=011b

5-3-2 Size setting for each sub-buffer

Before actual transmission/reception, it is first of all necessary to set up a sub-buffer size. Setting for asynchronous operation is made with an Asynchronous Buffer Size Set register and that for isochronous operation is made with an Isochronous Buffer Size Set register.

Asynchronous buffer size setting is made based on asynchronous transmission/reception total size (Total Size = ATF size + ARF size) and reception buffer size (ARF size). From these settings, the transmission buffer size is ATF size = Total size - ARF size. The setting unit is Quadlet.

The setting size must be at least more than the Quadlet figure of the transmitting packet for transmission, and more than the Quadlet figure of the receiving packet for reception. If the ATF size is set smaller than the transmitting packet size, the MD8412 cannot transmit this packet. If ARF is set smaller than the receiving packet size, the MD8412 returns Busy Acknowledge to the sending node and the packet buffering cannot be made completely within the ARF.

Setting for isochronous buffer size is similar to that for Asynchronous. For IsoMode setting other than 011b and 101b, ITF and IRF settings are made with Isochronous total buffer and IRF size. When IsoMode=011b, size setting is to be made for two IRF buffers. In this case also, total buffer size and IRF size are set.

In this case, the total size (ITotalSize) is a total of two receiving buffer sizes. IRF size (IRxBufferSize) is size of IRF buffer while an isochronous packet set by Isochronous Configuration Register-3 is received. Buffer size of the remaining one channel is Total Size - IRF Size. The sub-buffer for that size is ITF/IRF for an isochronous packet of Isochronous Configuration Register-2.

For IsoMod=010b, the isochronous buffer is not divided, and one receiving sub-buffer is set up. This buffer is IRF. For the size setting, contents of the total buffer size (ITotalSize) must be identical with those of IRxBufferSize.

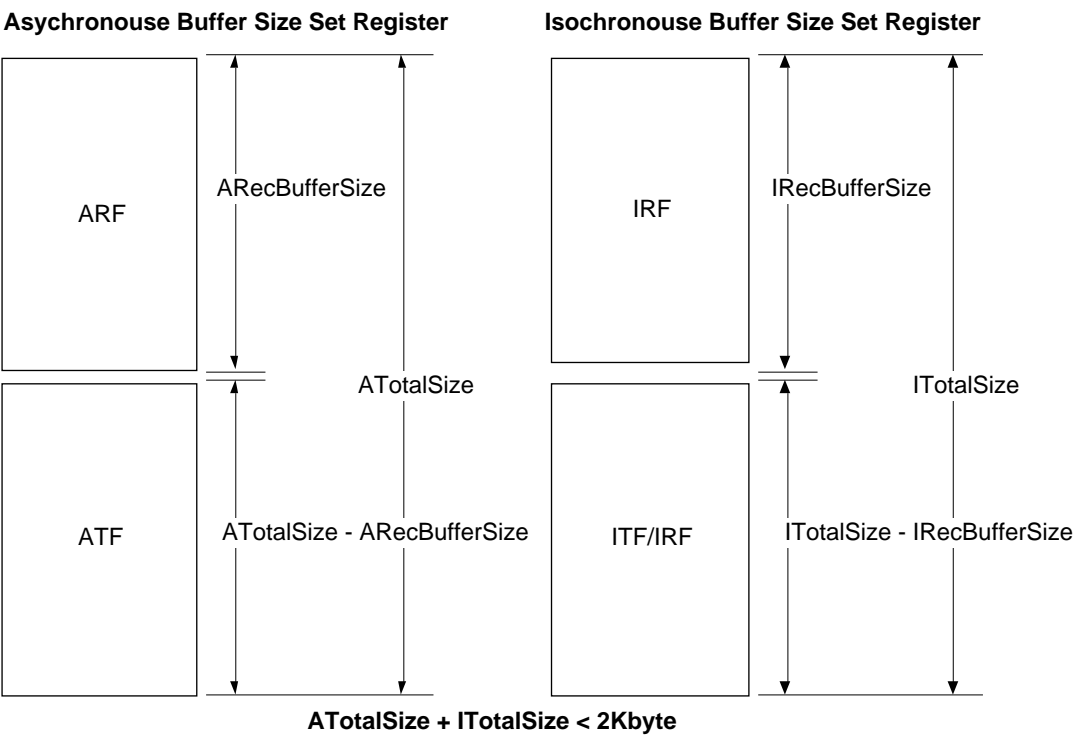


Figure 5-3-3 Sub-Buffer Size Assignment

5-3-3 Buffer access by bus width

As a method of access to a buffer, the MD8412 is provided with means of soft access and DMA access. Each method is described below.

5-3-3-1 Soft access

Since IEEE P1394 offers packet configuration of the Quadlet unit, method can differ according to the width of bus to be accessed. For a 32-bit width, data of one Quadlet can be written/read with a register corresponding to the directly controlling buffer. For an 8/16-bit width, however, data of one Quadlet must be divided and written/read 4 times for 8 bits, or twice for 16 bits.

At first, procedures of writing in the ATF buffer in 8-bit width are described below.

Data for 1 Byte are written in a 40h register. Writing is then forwarded in the order of 41h, 42h, and 43h. When writing for 43h is finished, data for one Quadlet become valid. Therefore, writing must be forwarded always in the order of 40h, 41h, 42h, and 43h.

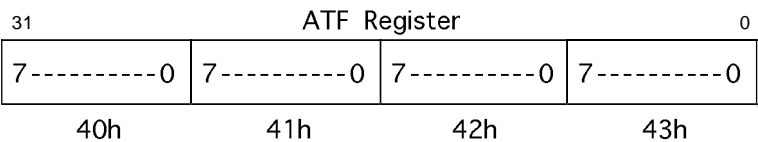


Figure 5-3-4 Register Operation (ATF) for 8-Bit Width Soft Access

Similarly, when reading out data from an ARF buffer, the reading order of 44h, 45h, 46h, and 47h must be followed. Situation is the same as for the isochronous ITF/IRF and IRF buffers.

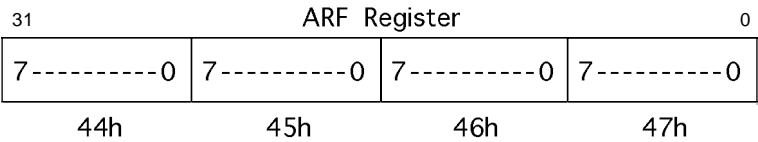


Figure 5-3-5 Register Operation (ARF) for 8-Bit Width Soft Access

When writing data in an ATF buffer in 16-bit width, writing for 8-bit width must be repeated 4 times. In this case, similar process must be followed for accessing, repeating writing twice.

At first, data for 1 word are written in a 40h register. Writing is then forwarded in the order of 42h. When writing for 42h is finished, data for one Quadlet become valid. Therefore, writing must be forwarded always in the order of 40h and 42h.

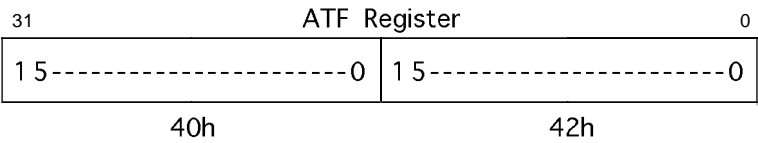


Fig. 5-3-6 Register Operation (ATF) for 16-Bit Width Soft Access

Similarly, when reading out data from an ARF buffer, it is necessary to read in the order of 44h and 46h. Situation is the same as for the isochronous ITF/IRF and IRF buffers.

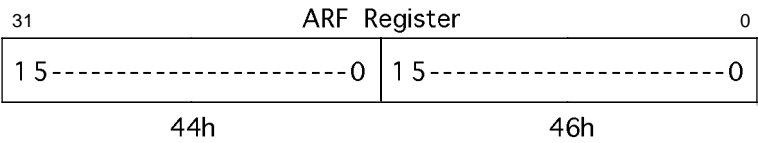


Figure 5-3-7 Register Operation (ARF) for 16-Bit Width Soft Access

5-3-3-2 DMA access

It is necessary to designate an objective buffer for DMA access using a SelectDreq bit.

At first, procedures for writing in an ATF buffer in 8-bit width are described below.

In the first place, SelectDreq=00b is set to make ATF an object of DMA transfer and DMAWidth=00b to designate 8-bit width transfer. When DMAC is started and DreqEn is then turned ON, a DREQ request is issued toward the DMAC and DMA transfer is started. In this case, the first 1 Byte is stored in 31~24 bit of the ATF buffer and the second Byte is stored in 23~16 bit. Likewise, the third Byte is stored in 15~8 bit and the 4th Byte is stored in 7~0 bit. Finally, data become valid as 1-Quadlet data. Accordingly, the number of DMA transfers must be always a multiple of 4.

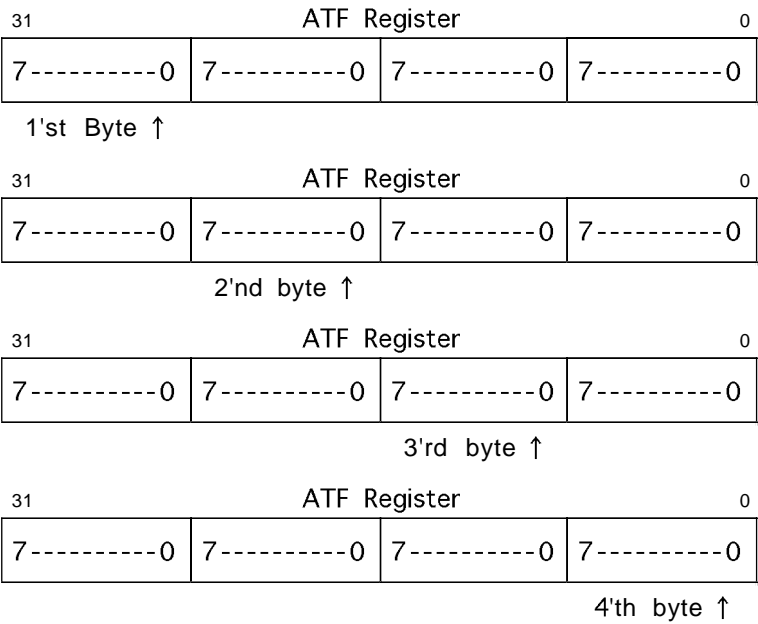


Figure 5-3-8 Register Operation (ATF) for 8-Bit Width DMA Access

Similarly, operation is the same when data are read from the ARF buffer by DMA transfer. Data are read from the upper area of 32 bit.

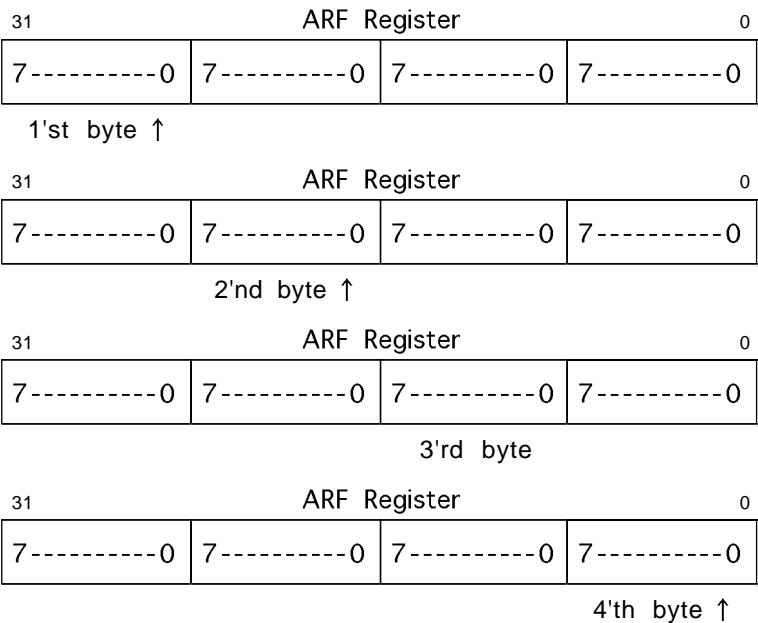


Figure 5-3-9 Register Operation (ARF) for 8-Bit Width DMA Access

Operation is the same as for 16-bit width. SelectDreq=00b is set to make ATF an object of DMA transfer, and DMAWidth=01b is set to designate 16-bit width transfer. When DMAC is started and DreqEn is turned on thereafter, a DREQ request is issued toward the DMAC, and DMA transfer is started. In this case, the first 1 Word is stored in 31~16 bit of the ATF buffer and the second Word is stored in 15~0 bit. Finally, data become valid as 1-Quadlet data. Accordingly, the number of DMA transfers must be always a multiple of 2.

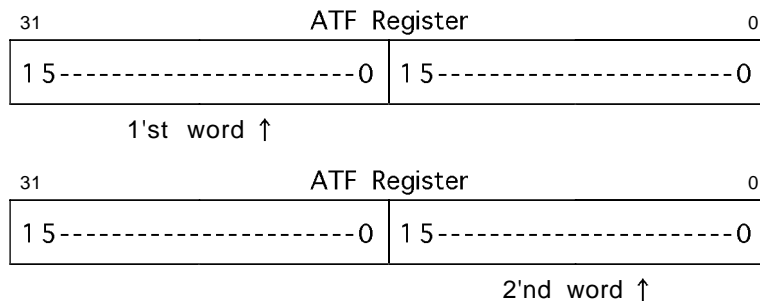


Figure 5-3-10 Register Operation (ATF) for 16-Bit Width DMA Access

Similarly, operation is the same when data are read from the ARF buffer by DMA transfer. Data are read from the upper area of 32 bits.



Figure 5-3-11 Register Operation (ARF) for 16-Bit Width DMA Access

5-3-4 Buffer control

Asynchronous buffer control is different from isochronous buffer control. Each control is described below.

5-3-4-1 Asynchronous buffer control

For both asynchronous transmission and reception, the host gains access to a buffer in the packet unit. Accordingly, as described previously, the size must always be larger than one packet when specifying a packet size for transmission and reception. Otherwise, the MD8412 cannot send out that packet in transmission phase. In reception phase, a BusyAck code is returned.

5-3-4-1-1 Transmission buffer

When data are sent from the host to a buffer in transmission phase and ATGo is issued, the data contained in the ATF are regarded as 1 packet. If there is still an empty in the ATF buffer after the issuing of ATGo, the host can write data of the next sending packet in this ATF. In this manner, the MD8412 performs reciprocal control of ATF in one-packet unit on host side and transmitter side. If the buffer status is not of Empty, the quantity of data the host can write next may be arbitrarily controlled according to the ATF size set by the

BufferSizeSet register and the packet size presently being handled for transmission by ATGo. Therefore, even though the BufferStatus register is not supervised, the host can identify vacancy in buffers at any time.

The packet data presently transmitted are kept buffered in the ATF until Ack code of complete or pending is returned from the related destination node. When the Ack code is Busy, the data buffered in the middle of retry phase are repeatedly transmitted according to the frequency of retry. When a retry count value is exceeded the max value, or complete or pending Ack code is returned during the operation, the area in the ATF, where the packet is contained, is automatically flushed. If an error Ack code is received in the retry phase, this phase is stopped at that time point and flushing is effected regardless of whether the retry maximum value is attained. In this case, even if the host has already written the next sending packet in a vacant area of ATF in the buffer, there is no influence on the data.

When ATF reset is effected with ResetATF bit in the Reset register, the ATF is restored to its initial condition and all data contained therein are lost, thus making the Empty flag active.

5-3-4-1-2 Reception buffer

Handling of the ARF for asynchronous reception buffer is basically the same as for transmission. When all contents of the received packet have been written in the ARF by the receiver, the host can read out the packet from the ARF. At that time, even though the host does not read out the packet from the ARF, writing operation into the ARF of the next packet from the receiver is effected, provided that there is still another vacancy in the ARF buffer. In this fashion, reciprocal control is effected even in the ARF. For example, assuming that the ARF presently contains one packet that can already be read out by the host and the next packet written from the receiver, the timing to permit writing of a new packet from the receiver into the ARF is defined as when the host has read out all contents of one packet. Therefore, under the condition that data of one packet plus α are remaining in the ARF, the receiver cannot write a new packet in the ARF. As a result, a BusyAck code is returned to the source node and a request is made for another transmission of the packet. When the host reads out a received packet from the MD8412 and concludes according to the contents that the header and successive data are not required for a certain reason, the host can flush all the data from the ARF using the ARFFlush bit in the BufferControl register, without performing wasteful reading of these data. Even when writing of a packet by the receiver has been already finished into the ARF, there is no influence on these data.

When ARF reset is effected with ResetARF bit in the Reset register, the ARF is restored to its initial condition and all data contained therein are lost. If the Full bit has been active, it is turned non-active.

5-3-4-2 Isochronous buffer control

5-3-4-2-1 For normal mode

Buffer control for isochronous transmission in normal mode is basically the same as for asynchronous buffer control. Control of transmission buffers is also reciprocally performed. Difference from asynchronous operation is that it is not a reciprocal changeover of a packet unit between host side and transmitter side, but it is done in the unit of packet group for several different channels to be transmitted in a certain isochronous cycle.

The number of packets that can be stored in the buffer during transmission is for the maximum number of channels insofar as the buffer has a vacant area. Packets for several channels that must be transmitted by the host in some cycle period are written in the ITF/IRF buffer and ITGo is then issued. The MD8412 transmits all data contained in ITF/IRF at that time point, using a cycle start shortly after the issuing of ITGo. In isochronous transmission, when packets have been transmitted, packet data are flushed from the ITF/IRF.

Unlike the previous modes, buffer control for reception is not reciprocally performed and one-directional FIFO control is effected. For reception, a maximum of 4 different channels can be received, set by the

Isochronous Configuration Register. The MD8412 automatically flushes the packet under the conditions that there is no empty area in the buffer for the received quantity of packet data, there is a CRC error in the packet header and pay-load area, and there is no coincidence between the header length value and the quantity of data in actual pay-load area.

5-3-4-2-2 For auto-mode

In auto-mode, one sub-buffer is assigned to one channel. Accordingly, the total number of channels applicable to transmission/reception is limited to 2. The combination is dependent on the IsoMode register. In the reception mode of two channels for IsoMode=0110, buffering is effected through routing to the two sub-buffers, according to the respective reception channels set by each Isochronous Configuration Register. Unlike the other modes, buffer control is not reciprocally performed and one-directional FIFO control is effected. During transmission, the MD8412 reads out data from the buffer for the amount of preset transmission data length value, and packet transmission is effected in synchronization with cycle start. If the quantity of data in the buffer is not enough to attain the preset length value at that time, packet transmission in that cycle is not effected, but a condition is waited until the specified amount of data has been written by the host. In this way, the host is not conscious of buffer writing in packet unit and data streams are written so that the transmission buffer ITF/IRF is not full.

Even in reception, one-directional FIFO control takes place, but the unit of announcement to the host is that of individual packet reception. Under the same condition as for the isochronous normal reception mode, the objective packets are automatically flushed.

5-4 Isochronous transfer control (auto-mode)

5-4-1 Length control

5-4-2 Sync control

5-5 Cycle Master

To maintain isochronous operation, a Cycle Master is always required on the bus. To obtain this Cycle Master, it is necessary to generate a cycle start event to be triggered by a CYCLE_TIME register that is synchronized with the 8kHz clock. This function is incorporated in the MD8412 which, therefore, has a capability of being a Cycle Master.

To become a Cycle Master, the CycleMaster bit is set at 1. This is, however, possible only if there is an announcement that the own node is a route. Being a Cycle Master, a cycle start packet is generated, synchronized with the cycle start event. It is controlled by the CycleTimerEn bit.

The 8kHz frequency, being a clock for the cycle start event generated in the Cycle Master, is obtained through internal frequency division from 49.152MHz of the master clock supplied from the PHY-chip, or by feeding an external 8kHz to the CYCLEIN terminal. Therefore, selection is needed. This setting is controlled by the CycleSource bit.

5-6 32-bit CRC

The packet data transmitted from the MD8412 are attached with a 32-bit CRC at the header block and the data block, as defined in the P1394 Draft. During reception, CRC is computed from data at the header block and the data block, in order to make comparison with the CRC data attached in the received packet. If there is no coincidence as a result of comparison, an announcement is given to the HdrErr bit located in the Interrupt register or the AckStatus bit of the Diagnostic Status register.

The following expression is used as the CRC polynomial:

$$X^{32} + X^{30} + X^{26} + X^{25} + X^{24} + X^{18} + X^{15} + X^{14} + X^{12} + X^{11} + X^{10} \\ + X^9 + X^6 + X^5 + X^4 + X^3 + X + 1$$

5-7 Control Flow

5-7-1 Asynchronous Transmission

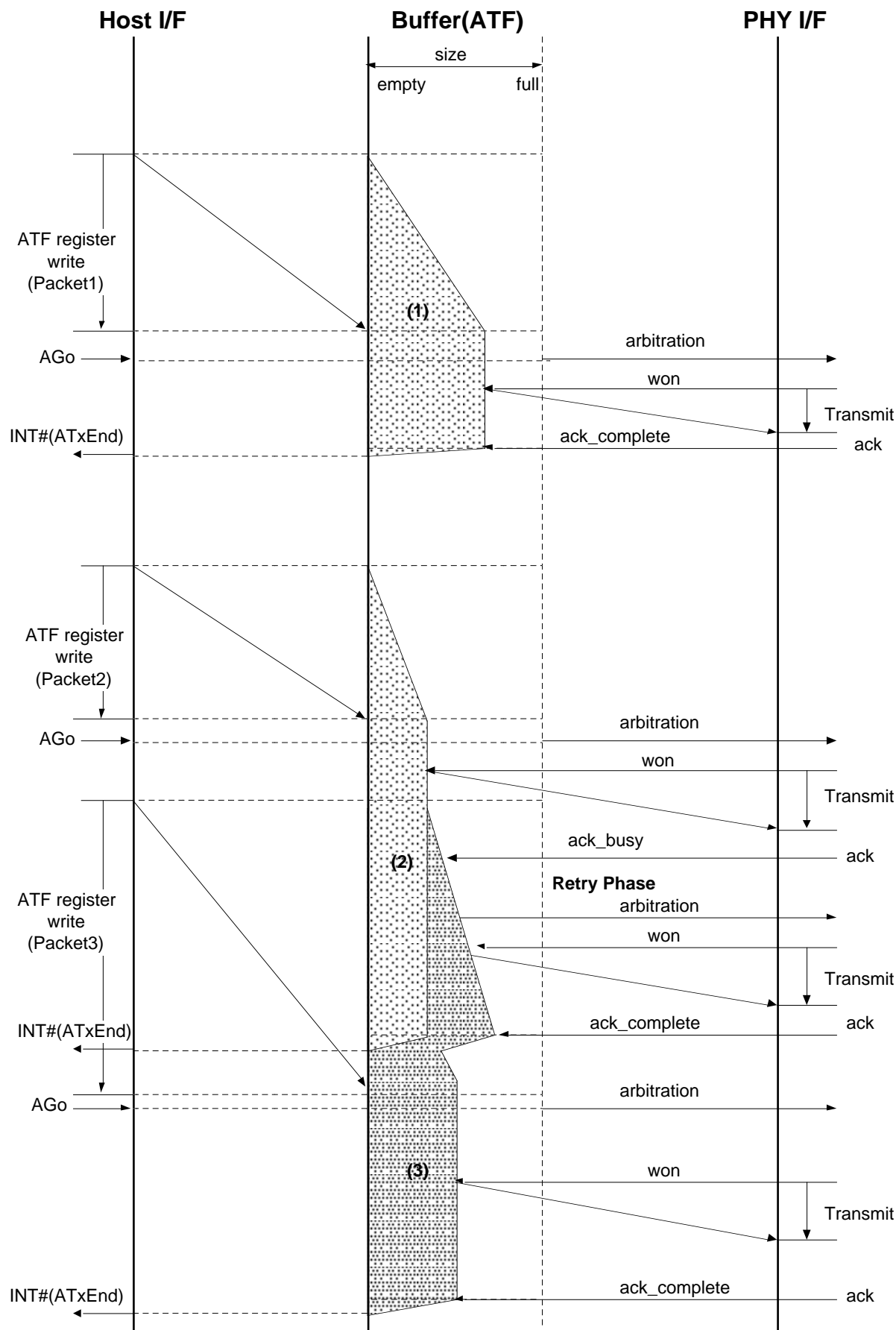


Figure 5-7-1 ATF Transmission Flow -1

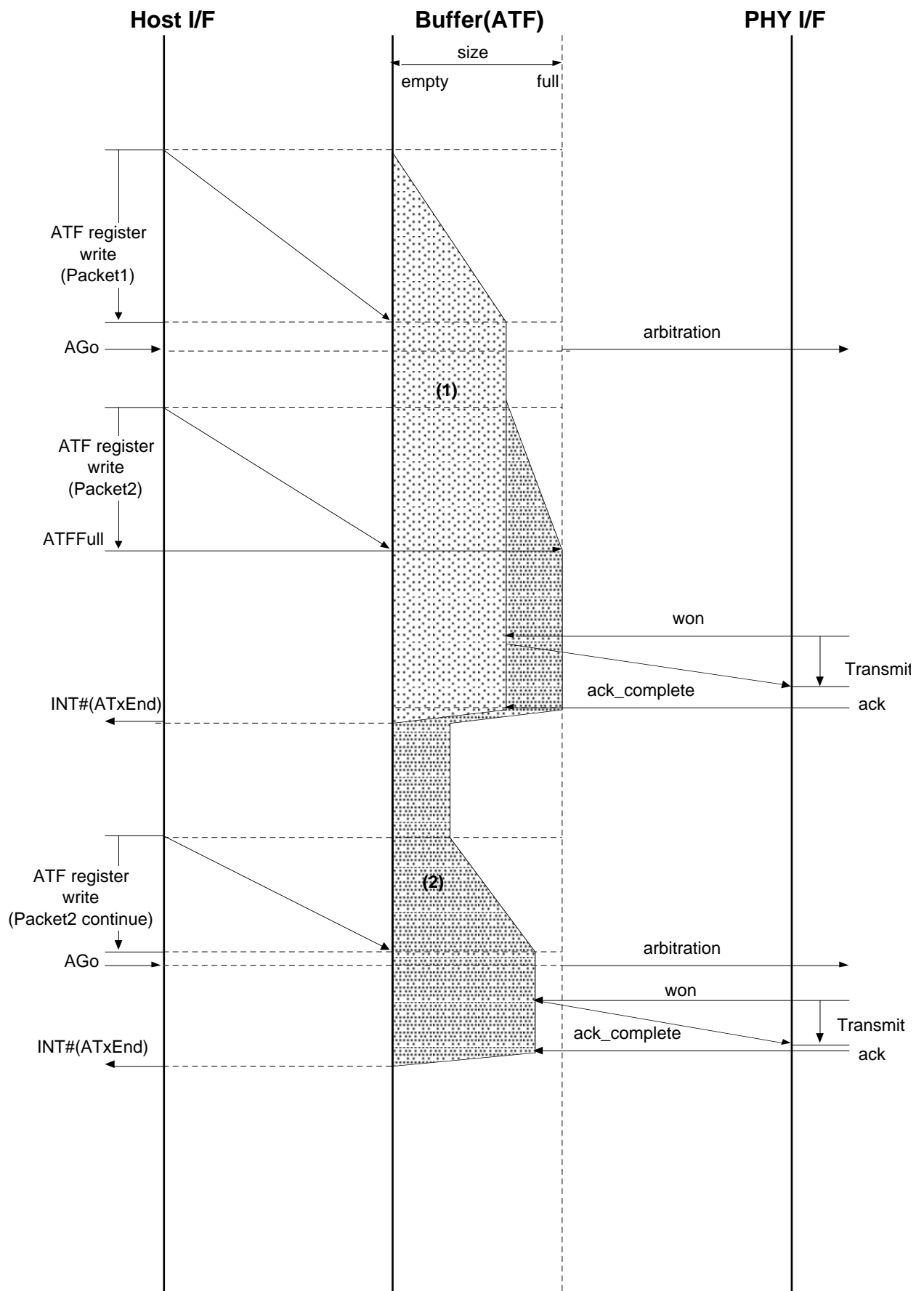


Figure 5-7-2 ATF Transmission Flow -2

5-7-2 Asynchronous Reception
Host I/F

Buffer(ARF)

PHY I/F

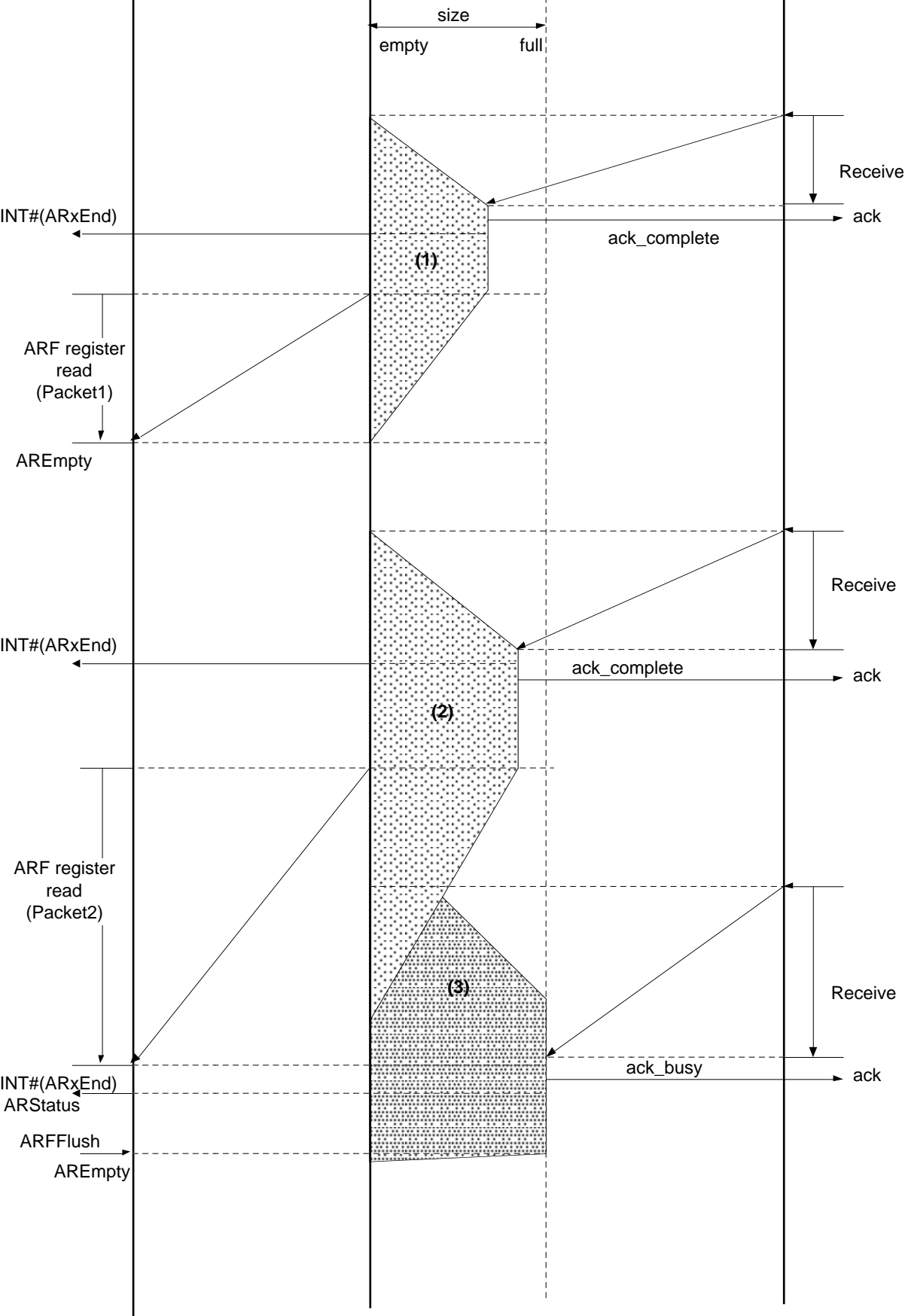


Figure 5-7-3 ARF Reception Flow -1

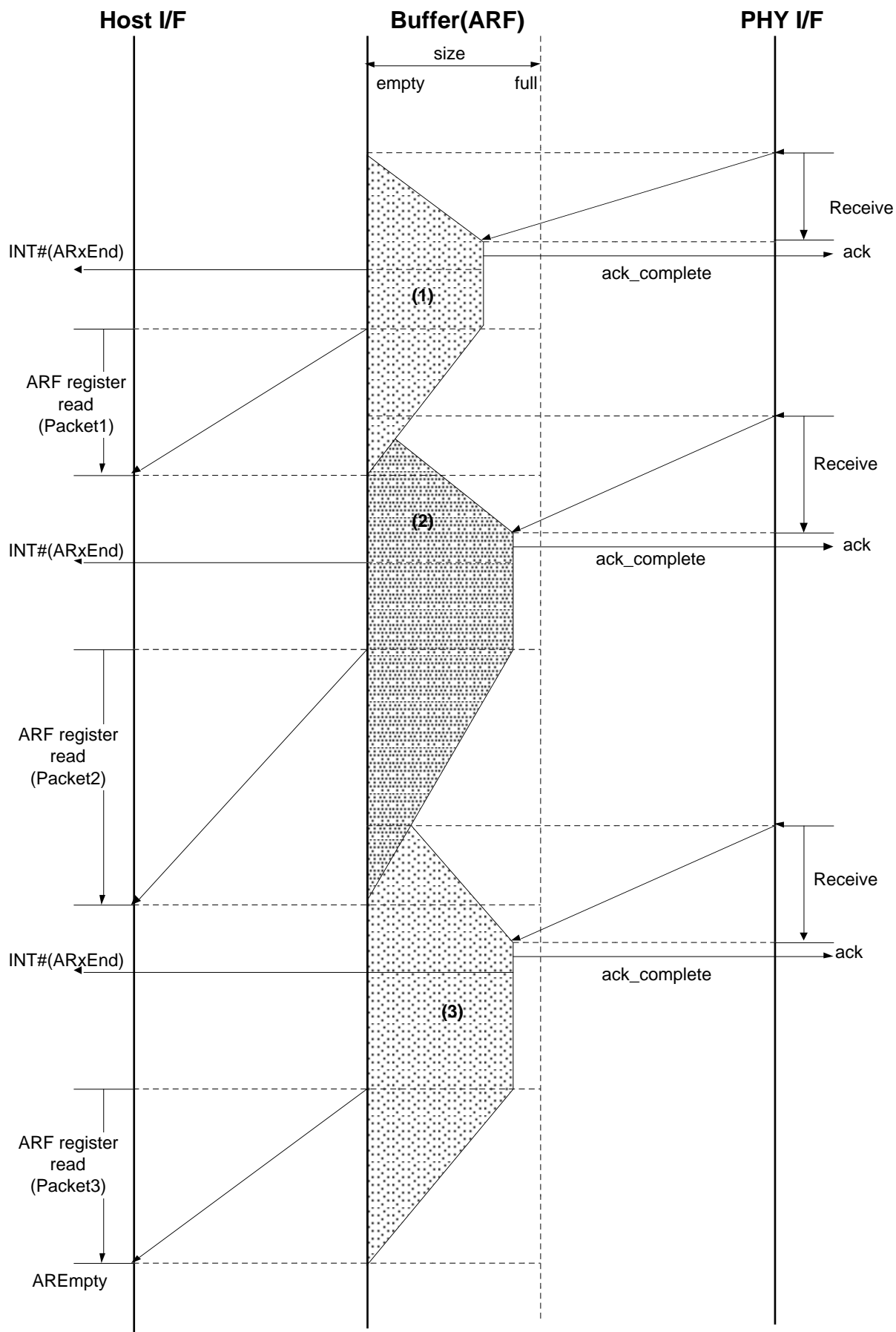


Figure 5-7-4 ARF Reception Flow -2

5-7-3 Isochronous Transmission
Host I/F

Buffer(ITF)

PHY I/F

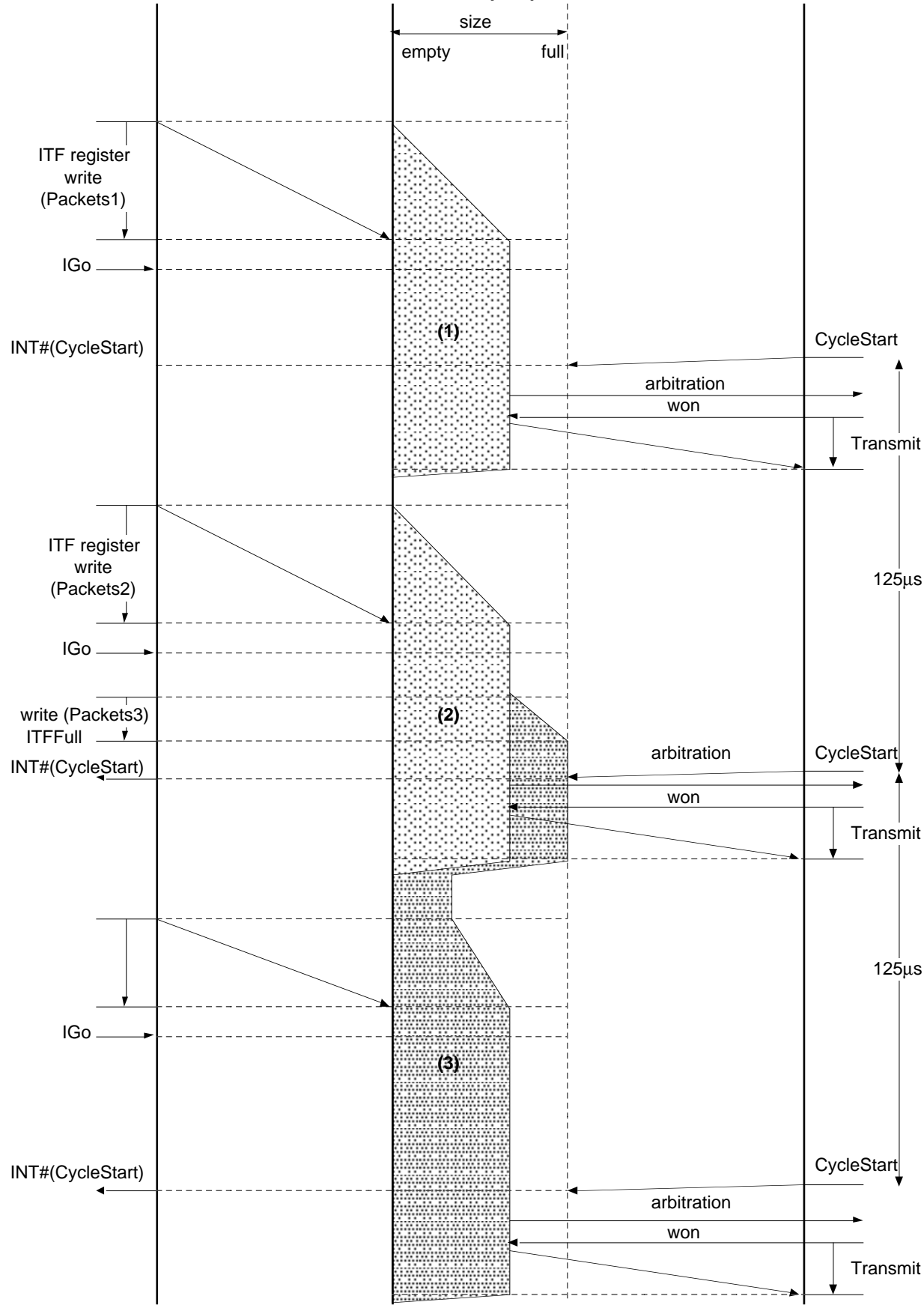


Figure 5-7-5 ITF Transmission Flow

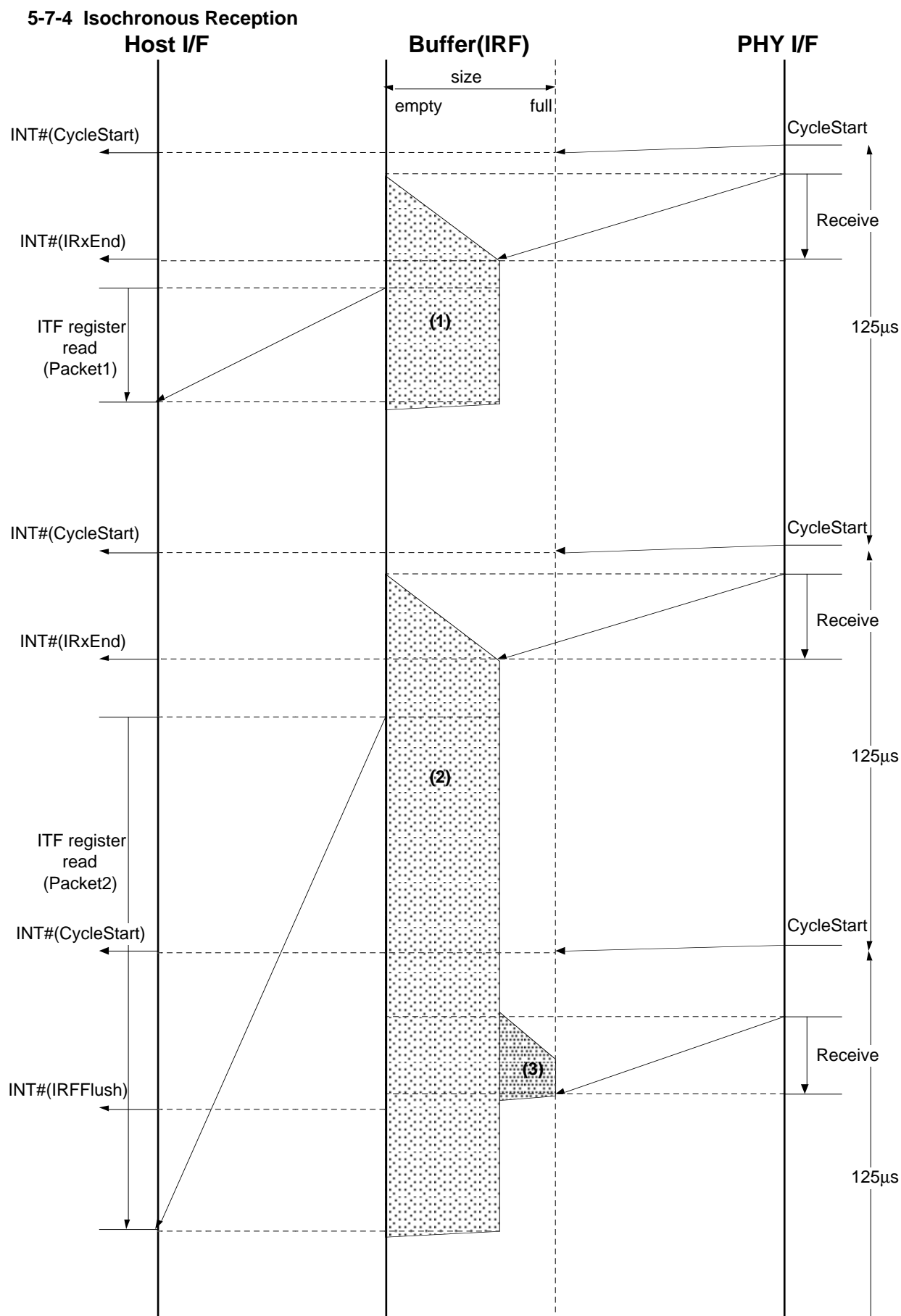


Figure 5-7-5 IRF Reception Flow

6 Electrical Characteristics

6-1 Absolute Rating

(VSS = 0V)

Symbol	Parameter	Rating	Units
VDD	Supply Voltage	VSS - 0.3 ~ VSS + 7.0	V
VIN	Input Voltage	VSS - 0.3 ~ VDD + 0.3	V
VOUT	Output Voltage	VSS - 0.3~ VDD +0.3	V
IIN	Input Current	±10	mA
TSTG	Storage Temp.	- 40 ~ + 125	°C

6-2 Recommended Operating Condition

Symbol	Parameter	Rating	Units
VDD	Power Voltage	4.75~ 5.25	V
VIN	Input Voltage	0 ~ VDD	V
VOUT	Output Voltage	0 ~ VDD	V
TA	Storage Temp.	0~ + 70	°C

6-3 DC Characteristics

(VSS = 0V)

Symbol	Item	Pin	Test Condition	MIN	TYP	MAX	Unit
VIH	High Level Input Voltage	SCLK,CTL,D		3.5			V
		else		2.0			
VIL	Low Level Input Voltage	SCLK,CTL,D				1.5	V
		else				0.8	
IIH	High Level Input Current	TLINK, TLINKSEP,TRFUL, TRAFUL,TRFAVL, TEST0,TEST1	VIN=VDD	10		200	μ A
		else		-10		10	
IIL	Low Level Input Current	CQMODE,LREQMOD E	VIN=VSS	-200		-10	μ A
		else		-10		10	
VOH	High Level Output Voltage	LPS,LREQ,CTL,D	IOH=-12mA	2.4			V
		CYCLEOUT	IOH=-24mA				
		else	IOH=-4mA				
VOL	Low Level Output Voltage	LPS,LREQ,CTL,D	IOL=12mA			0.4	V
		CYCLEOUT	IOL=24mA				
		else	IOL=4mA				
IOZ	Output Disable Current		VOUT=VDD or VSS	-10		10	μ A
IDD	Dinamic Current	VDD	VDD=5.0V		190		mA

6-4 AC Characteristics

Symbol	Item	MIN	TYP	MAX	Unit	
T _{CSS}	CS#, DACK# Setup Time	5			nS	
T _{CSWH}	CS#, DACK# Hold Time (WRITE)	0			nS	
T _{CSRH}	CS#, DACK# Hold Time (READ)	0			nS	
T _{ADS}	HA, UWE#, UBE# Setup Time	10			nS	
T _{ADH}	HA, UWE#, UBE# Hold Time	5			nS	
T _{RW}	READ WRITE Puls Width	42			nS	
T _{RWC}	READ/WRITE Cycle Time	120			nS	
T _{DTD}	Read Data Output Delay Time	4		30	nS	※1
T _{DTH}	READ DATA Output Hold Time	5		30	nS	※1
T _{WRDS}	WRITE DATA Setup Time	10			nS	
T _{WRDH}	WRITE DATA Hold Time	2			nS	
T _{RSW}	Reset Puls Width	160			nS	
T _{CYCD}	CYCLEOUT Output Delay	4		17	nS	※2

※1 : Load Capacitor 50pF

※2 : Load Capacitor 20pF

Table 6-4-1 Host Interface AC Characteristics

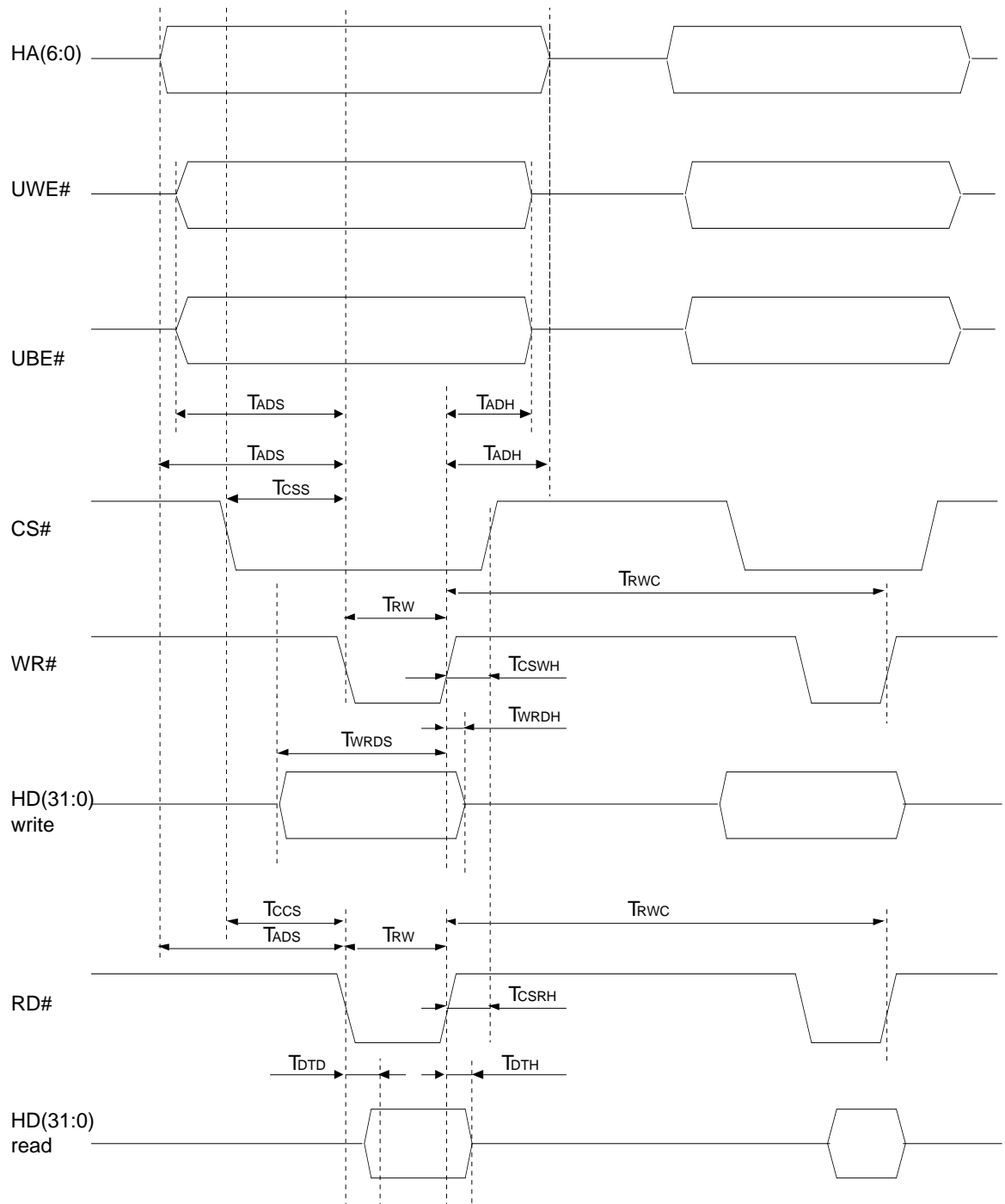


Figure 6-4-1 Host Interface AC Characteristics (Read/Write)

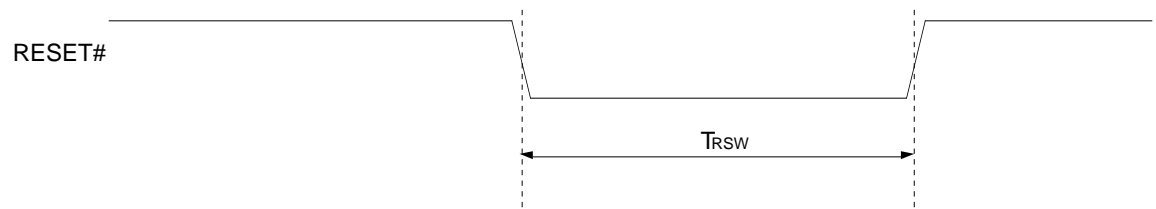


Figure 6-4-2 Host Interface AC Characteristics (Reset)

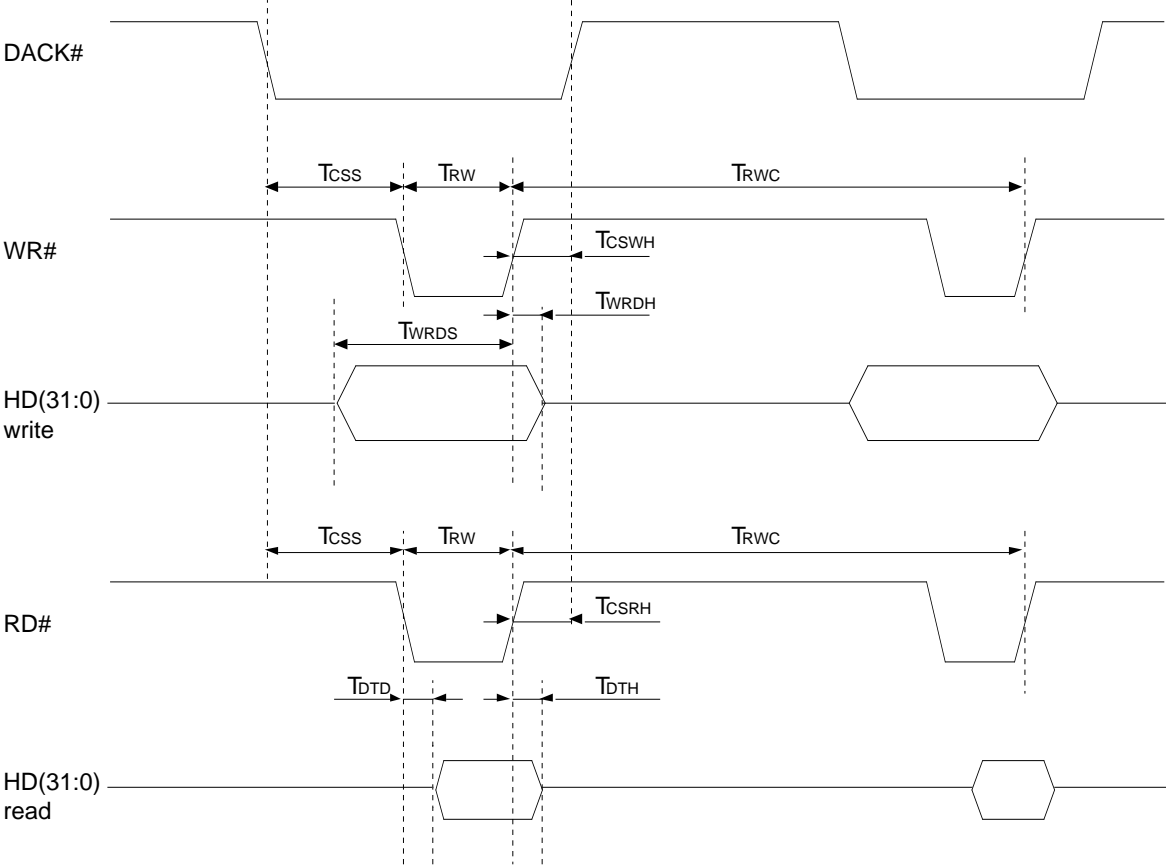


Figure 6-4-3 Host Interface AC Characteristics (DMA)

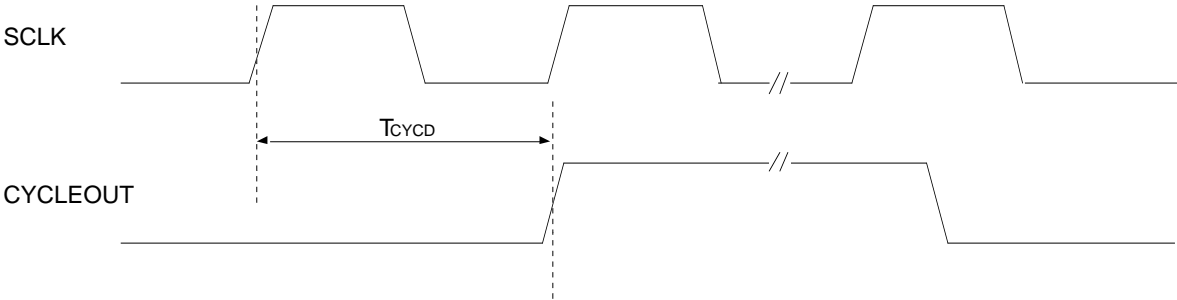


Figure 6-4-4 Host Interface AC Characteristics (CYCLEIN/OUT)

Symbol	Item	MIN	TYP	MAX	Unit
T_{CTD}	Control Output Delay	3		13	nS
T_{PDD}	PHY Data Output Delay	3		13	nS
T_{CTS}	Control Setup	6			nS
T_{CTH}	Control Hold	0			nS
T_{PDS}	PHY Data Setup	6			nS
T_{PDH}	PHY Data Hold	0			nS
T_{LRD}	LREQ Data Output Delay	3		13	nS
T_{SCKC}	SCLK Cycle Time	20			nS
T_{SCKH}	SCLK High Level Time	8		12	nS
T_{SCKL}	SCLK Low Level Time	8		12	nS
T_{LPSC}	LPS Cycle Time	360		570	nS
$T_{LP SH}$	LPS High Level Time	175		290	nS
$T_{LP SL}$	LPS Low Level Time	175		290	nS

(Condition : Load Capacitor 50pF)

Table 6-4-5 PHY AC Characteristics

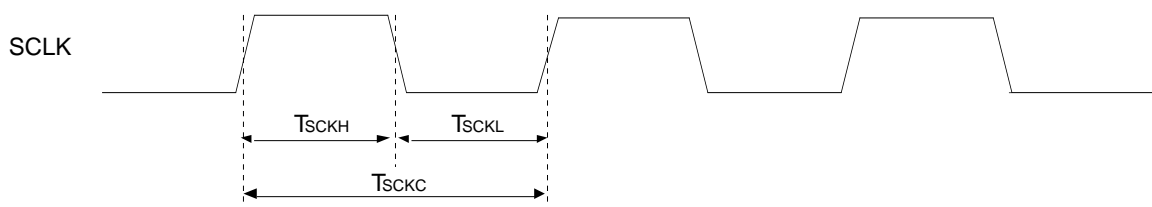


Figure 6-4-6 PHY AC Characteristics(SCLK)

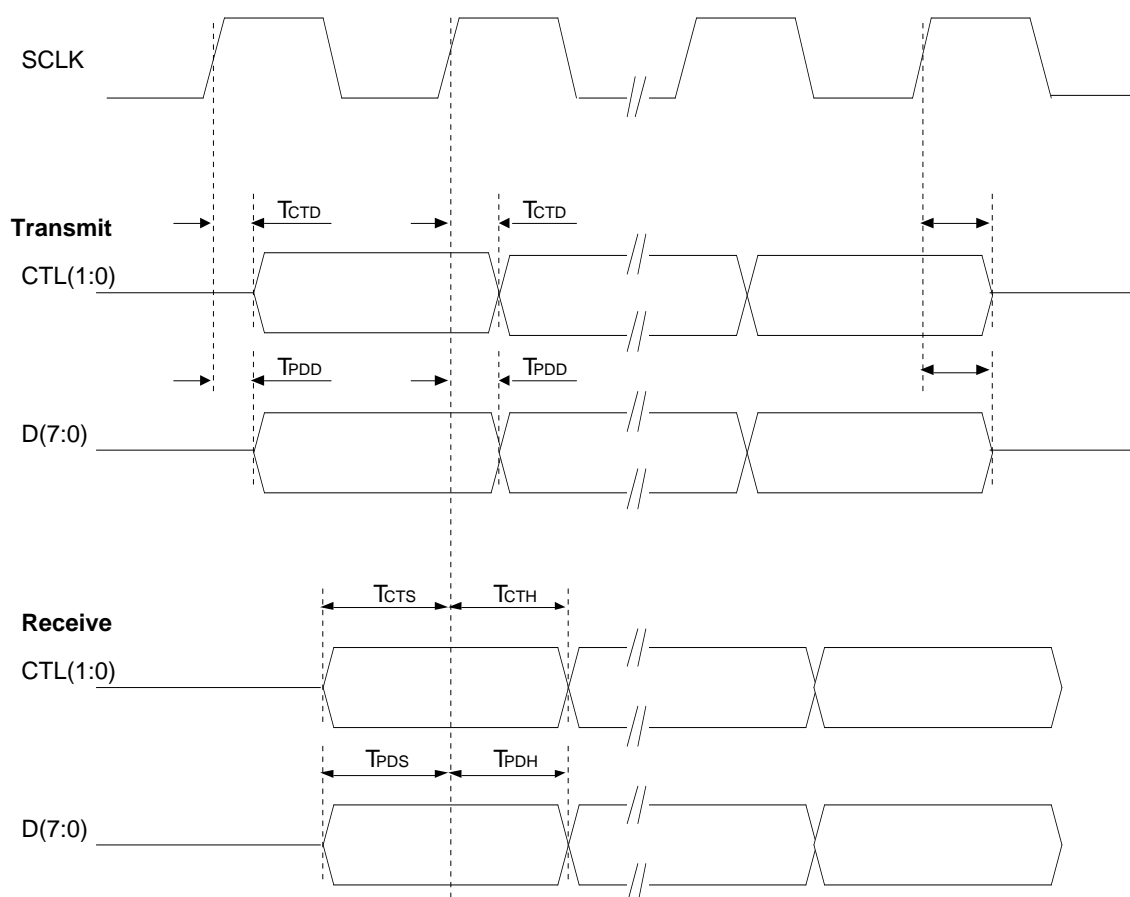


Figure 6-4-7 PHY AC Characteristics(CTL,D)

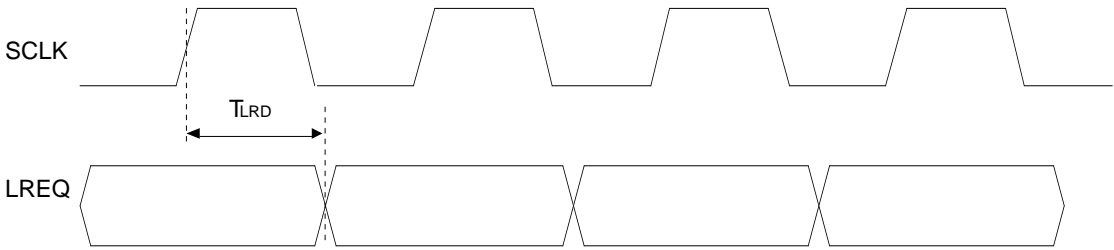


Figure 6-4-8 PHY AC Characteristics(LREQ)

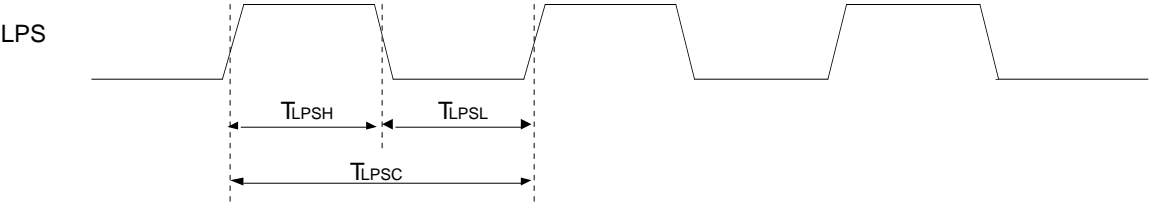
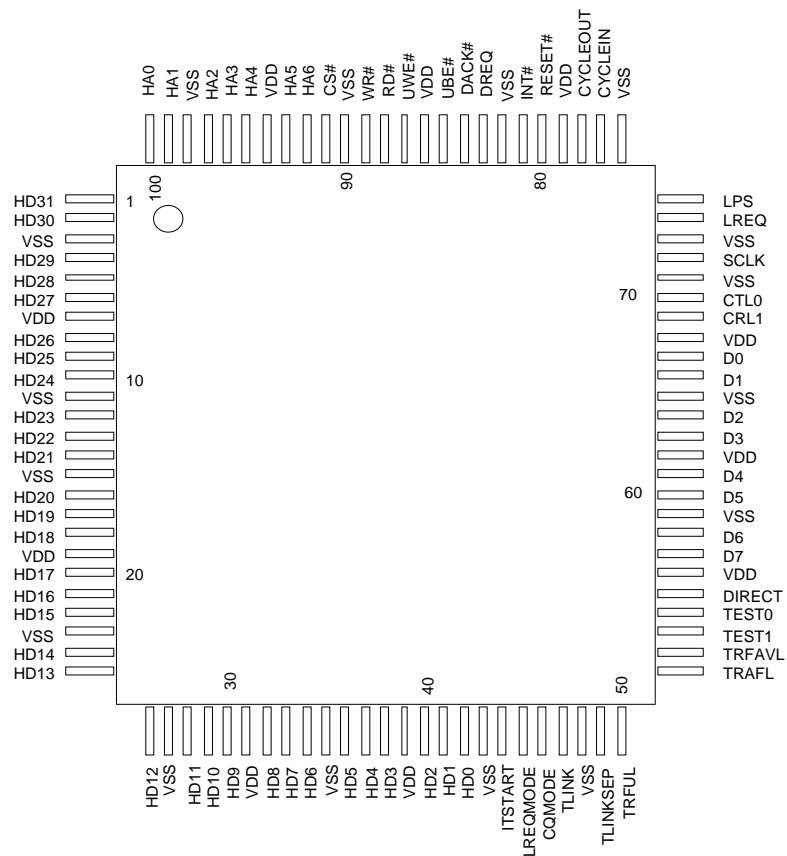


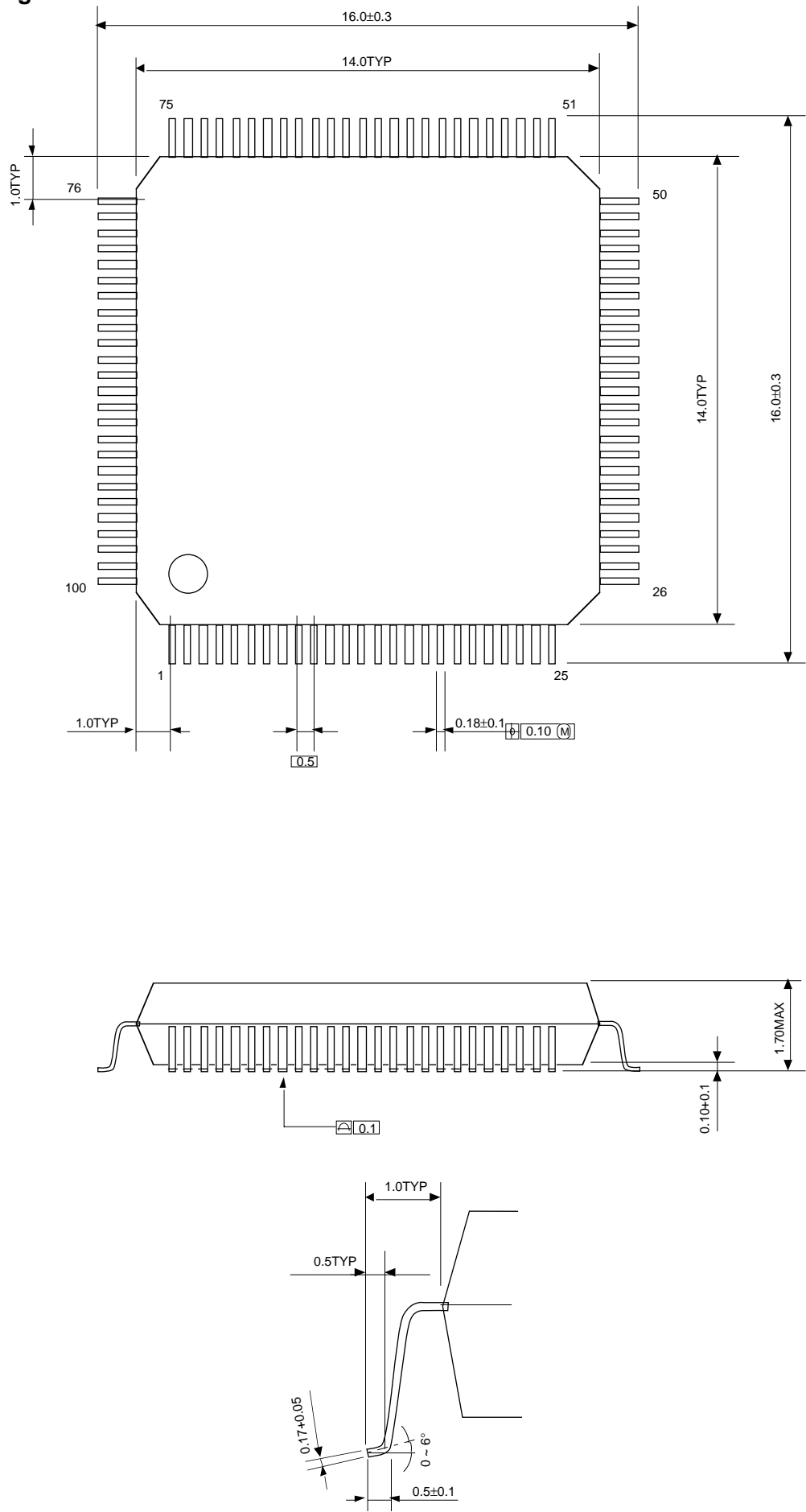
Figure 6-4-9 PHY AC Characteristics(LPS)

7 Pin Assignment and Package Outline

7-1 Pin Assignment



7-2 Package Outline

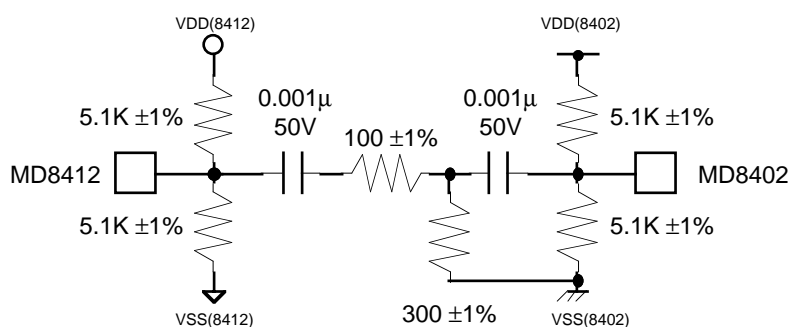


Appendix 1 I/O Status

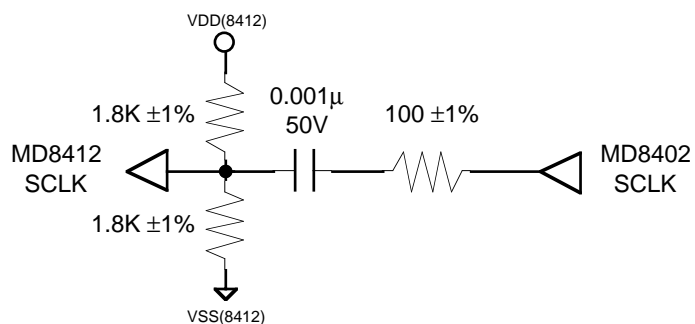
PIN	I/O	PowerOn	RESET#Low	Normal
SCLK	I	Hi-Z	←	←
LREQ	O			
CTL(1:0)	I/O			
D(7:0)	I/O			
HA(6:0)	I	Hi-Z	←	←
HD(31:0)	I/O	When RD# is 'H' Hi-Z	←	←
WR#	I	Hi-Z	←	←
RD#	I	Hi-Z	←	←
CS#	I	Hi-Z	←	←
UWE#	I	Hi-Z	←	←
UBE#	I	Hi-Z	←	←
DREQ	O	N/A	Low	Low/High
DACK#	I	Hi-Z	←	←
INT#	O	N/A	High	Low/High
RESET#	I	Hi-Z	←	←
CYCLEIN	I	Hi-Z	←	←
CYCLEOUT	O			
ITSTART	I	Hi-Z	←	←

Appendix 2 Example circuit for AC connection

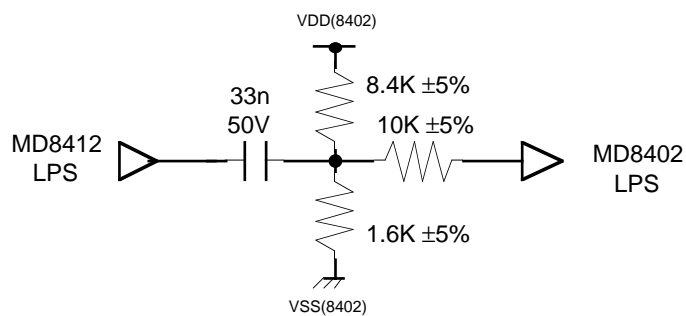
1) LREQ,CTL(0:1),D(0:7)



2) SCLK



3) LPS



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