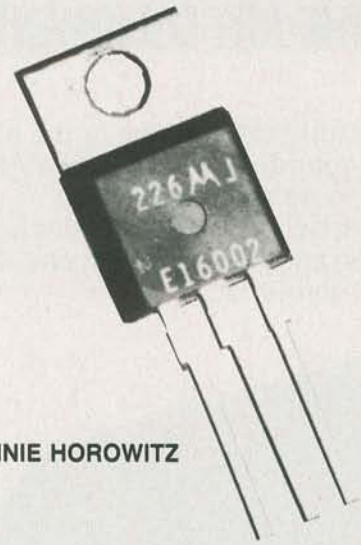
How to Design Analog Circuits —Amplifying AC Signals



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One of the most important uses for the transistor is in an amplifier circuit. This month, we'll look at how a one-stage transistor amplifier works, as well as how to design one.

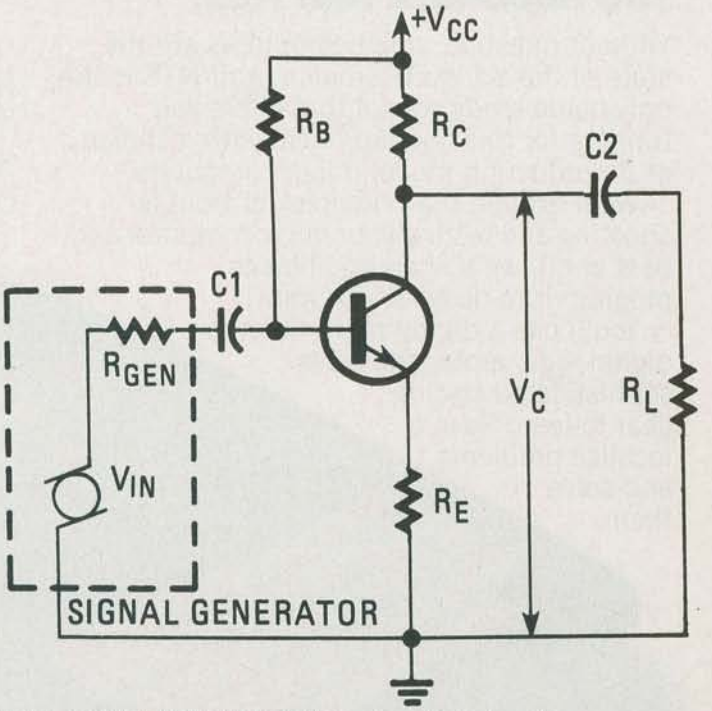

FIG. 1—COMMON-EMITTER AMPLIFIER using a bipolar transistor.

IN THE PREVIOUS PART OF THIS SERIES, WE looked at different bias circuits and analyzed the DC behavior of a one-stage transistor amplifier. But merely biasing a transistor at the quiescent operating point does not produce a functional circuit. The transistor must also be capable of amplifying an AC signal.

When an AC signal is applied to a transistor amplifier stage, many of the transistor parameters, such as gain (β), change from the nominal DC value. Also, for the circuit to be functional, several components must be added to the basic DC circuit. For example, a load resistor must be included so that the output signal can be obtained; and capacitors must be added so that the AC signal does not upset the DC bias voltages. This month, we will analyze the behavior of a one-stage transistor amplifier when an AC signal is applied to it. We will also look at a complete step-by-step design example.

AC bipolar transistor analysis

Last time, we discussed several bias circuits for establishing the collector-to-emitter voltage (V_{CE}) at the quiescent operating point (no-input signal condition). For our analysis of AC operation, we'll use the simplest bias circuit that we described last time, as shown in Fig. 1. The circuit shown in Fig. 1 also includes a sinusoidal voltage source, a load resistor, and two capacitors.

The sinusoidal AC voltage source is V_{in} and since no voltage source is perfect, its internal impedance is not equal to zero. Here, the internal impedance of the generator is shown as R_{gen}.

The signal from the generator is connected to the base of the transistor through capacitor C1. That capacitor prevents the bias current provided by R_B from flowing into the generator and to ground through R_{gen} and thus upsetting the quiescent operating point. At the same time, the value of the capacitor is large enough to allow the AC signal from the generator to pass through it to the transistor.

The AC signal that appears at the base of the transistor is amplified by the transistor. The resulting amplified signal appears across R_C and is applied to the load resistor through capacitor C2. Capacitor C2 prevents the DC voltage at the collector of the transistor from appearing across load resistor R_L while passing the amplified AC signal present at that point in the circuit. Capacitor C2 prevents the DC collector voltage from being affected by the presence of R_L in the circuit.

The voltage across R_C is $I_C \times R_C$, where I_C is the DC collector current. Because of that, the collector voltage is:

$$V_C = V_{CC} - I_C \times R_C$$

If capacitor C2 were not present, R_L would complete a DC current path from V_{CC} through R_C to ground. The additional current, I_L, would add to I_C to determine the total DC current flowing through R_C. The voltage across R_C would be $(I_C + I_L)R_C$. The voltage at the collector (V_C) would drop to $V_{CC} - (I_C + I_L)R_C$.

But what is R_L doing in the circuit? It represents the AC load on the output of the transistor. If this were an audio power amplifier, R_L could represent the im-

pedance of a loudspeaker. If this collector circuit were connected to the input of a second transistor to get additional gain, R_L would be the input impedance of that second transistor circuit.

The circuit around the transistor affects the operation of the transistor just as the various transistor parameters affect the overall circuit performance.

We discussed alpha and beta and described how DC current at the input of a transistor is amplified and appears at the output. The output current is beta times the input current. A similar amplification takes place due to the AC current gain, or AC beta, of the transistor. Although the Greek letter β is usually used to indicate that parameter, some specification sheets use the hybrid parameter, h_{fe}. They both have the same meanings.

The AC beta and DC beta can be derived from the common-emitter curves of the transistor. A typical set of curves is drawn in Fig. 2. Let us assume that a load

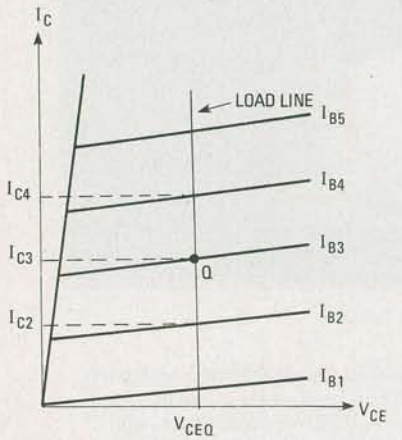

FIG. 2—TYPICAL CHARACTERISTIC CURVES of a bipolar transistor.

line was plotted and that the quiescent operating point, Q, was chosen as shown. At the quiescent operating point, the idling base current is I_{B3}, the idling collector current is I_{C3}, and the collector-to-emitter voltage is V_{CEQ}. Since the DC beta (β_{DC}) is simply the ratio of collector current to base current at any one point on the curves, β_{DC} is equal to I_{C3}/I_{B3}.

The AC beta, β_{AC}, is the ratio of a change in collector current to a change in base current at a specific collector-emitter voltage, V_{CEQ}. We can use that concept to determine the value of β_{AC} from the curves. It is equal to:

$$\beta_{AC} = \frac{I_{C4} - I_{C2}}{I_{B4} - I_{B2}} \quad \frac{\Delta I_C}{\Delta I_B} \qquad (1)$$

Hereafter, as is commonly done throughout our industry, we will refer to the AC beta simply as beta and apply the symbol β to it. For the DC beta, we will retain the symbol β_{DC}.

It is difficult to determine the AC alpha of the transistor from the curves because

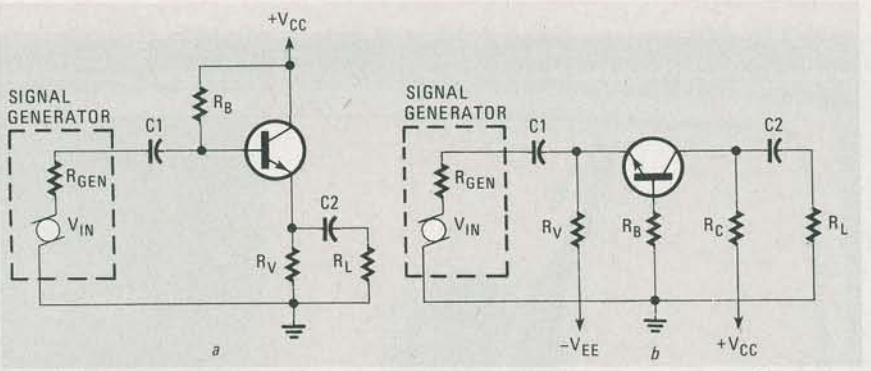

FIG. 3—DIFFERENT CIRCUIT CONFIGURATIONS for the bipolar transistor. The common-collector circuit is shown in *a*. The common-base circuit is shown in *b*.

the section of the curves that we are interested in are almost perfectly horizontal and, as a result, alpha is very close to 1. However, α_{AC} (or α) can be determined from the AC beta using the same equation used for determining β_{DC}.

$$\alpha = \frac{\beta}{1 + \beta} \qquad (2)$$

Another important parameter when analyzing the AC performance of a transistor is the emitter resistance. When we were analyzing the DC performance of a transistor, R_E was an actual resistor connected to the emitter of the transistor and it was the only resistance of significance in the emitter circuit. But when an AC signal passes through the transistor, there is also an internal AC resistance that is in the emitter of the transistor itself. That resistance, r_e, can be determined from the following equation:

$$r_e = \frac{26}{I_C} \qquad (3)$$

In equation 3, I_C is expressed in milliampers and r_e in ohms. When analyzing the AC performance of a common-emitter transistor amplifier, the resistance in the emitter circuit is $r_e + R_E$. When that is reflected as a resistance into the base circuit, the sum is multiplied by the AC beta.

The collector resistance, r_c and r_d, were discussed in the article on bias circuits that appeared in the September issue. The methods for determining those resistances were covered there and those methods remain the same.

As a final parameter to be noted here, we will consider the base resistance, r_b. That is usually an insignificant factor when doing a design. The AC resistance r_b is considered as being in series with the base. It is usually between 500 and 1000 ohms—values that can be ignored in most designs.

AC bipolar-transistor amplifiers

Using the parameters detailed above, we can now define several AC characteristics of the circuit shown in Fig. 1.

The input impedance seen looking into the base circuit itself, is:

$$R_{in} = r_b + \beta(R_E + r_e) \qquad (4)$$

The generator sees that resistance in parallel with R_B because the upper terminal of R_B is connected to $+V_{CC}$ and that terminal is at AC ground through the power supply. (The $+V_{CC}$ terminal is $+V_{CC}$ volts above DC ground. But an ideal voltage source has zero impedance. Because of that, the $+V_{CC}$ point is treated as being at signal or AC ground.)

The output impedance seen looking back into the collector circuit is:

$$R_{out} = \frac{r_d[(R_{gen} + r_b) + \beta(r_e + R_E)]}{R_{gen} + r_b + r_e + R_E} \qquad (5)$$

Note that the impedance of the generator and the base resistance are reflected from the input of the transistor to the output. Both factors therefore appear in equation 5. The load resistance, R_L, sees R_{out} in parallel with R_C. The current gain (A_i) and voltage gain (A_v) for the circuit shown in Fig. 1 are:

$$A_i = \beta \qquad (6)$$

$$A_v = \frac{R_L \| R_C}{R_E + r_e} \qquad (7)$$

where $R_L \| R_C$ is the resistance of R_C and R_L connected in parallel. The power gain, G, is the product of A_i and A_v.

In the common-collector circuit shown in Fig. 3-a, the input impedance of the transistor is calculated using equation 4, but R_E is usually much larger here than when specified for the common-emitter arrangement. The generator still sees R_B in parallel with R_{in}. As for the output resistance R_{out} (the resistance seen when looking back into the transistor), it is the sum of r_e and the total resistance in the base circuit divided by beta. The resistance in the base circuit is the sum of r_b and the parallel combination of r_{gen} and R_B.

The voltage gain of the common-collector circuit itself is approximately equal to 1. The combination of a relatively low input impedance, a high output impedance (as already stated, R_E is usual-

ly specified to be a high resistance) and a voltage gain approximately equal to 1, makes the common collector circuit ideal in buffer amplifier applications. The current and power gains are approximately equal to beta.

The common-base circuit is shown in Fig. 3-b. The input impedance seen by the generator is the parallel combination of R_E and R_{in}, where:

$$R_{in} = r_e + \frac{r_b + R_B}{\beta} \qquad (8)$$

The output resistance seen by the load resistance is the parallel combination of R_C and R_{out}, where:

$$R_{out} = \frac{r_c[\beta(r_e + r_{gen}) + (r_b + R_B)]}{\beta(r_e + r_{gen} + r_b + R_B)} \qquad (9)$$

The current gain of the circuit is equal to α or slightly less than 1. Both the voltage gain and the power gain are equal to:

$$A_v = G = \frac{R_L \| R_C}{r_e} \qquad (10)$$

To find the voltage and power gain of the overall circuit, simply add r_{gen} to r_e in the denominator in equation 10.

A step-by-step design

The equations given in this article can be used to design actual circuits. As an example, let us again consider the circuit shown in Fig. 1. You would start the design of the circuit by knowing the power-supply voltage as well as the beta of the transistor. For this example, let us assume that V_{CC} = 9 volts and that β = 300. Next, determine the load resistance, R_L, that the circuit will be connected to. Let's assume you must feed a 10,000 ohm load. The collector resistor, R_C, should be between 10% and 25% of R_L so that the AC load line will not differ by much from the DC load line. (We will discuss that factor in more detail in a future article on power amplifiers). A good compromise is to make R_C equal to 2700 ohms. The resistance in the collector circuit is 10,000 ohms in parallel with 2700 ohms, or 2100 ohms. If the circuit is to provide a voltage gain of 10, then the ratio of the resistance in the collector circuit to the resistance in the emitter circuit should be 10. Using that information, the emitter resistance should be 2100/10 = 210 ohms. But what portion of the 210 ohms does the r_e in the transistor provide and what portion of the 210 ohms does emitter resistor R_E provide? To determine that, we must know the collector (or emitter) current.

If the power-supply is 9 volts, ideally we want one-half of that or 4.5 volts at the collector. If that were the quiescent collector voltage, the signal could swing, at least ideally, from 0 to 9 volts around the 4.5-volt quiescent setting. To achieve that, 4.5 volts must be across the 2700-ohm collector resistor (R_C). The collector current, I_C, is then equal to 4.5/2700 = 1.67 mA. Plugging that information into equation 3, we find that r_e is equal to 26/1.67 = 15.6 ohms. Since the total maximum resistance in the emitter circuit is 210 ohms, R_E can be as high as 210 − 15.6 ohms or 194.4 ohms, Use a standard 180-ohm resistor for R_E.

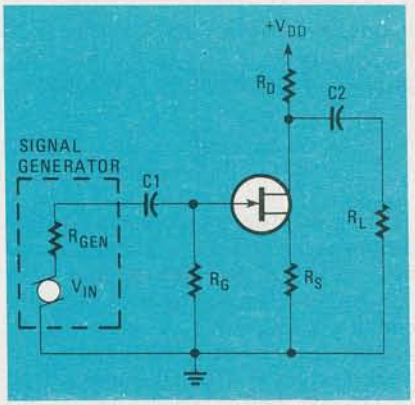

FIG. 4—COMMON-SOURCE AMPLIFIER circuit is shown here.

To get a collector current of 1.67 mA, the base current, I_B, must be 1.67 mA divided by the beta of the transistor. Therefore, I_B = 1.67/300 = 5.6 μA. Base current is provided by the 9-volt supply and flows through R_B, through the base-emitter junction, and then through R_E. Hence the base current, I_B, is equal to $9/(R_B + R_E)$ = 5.6 μA. The base-to-emitter voltage, V_{BE}, is ignored because it is negligible compared to 9 volts. Going through the algebra to determine R_B, we find it is about 1.5 megohms.

Taking that one step further, assume the impedance of the generator, r_{gen}, is 10,000 ohms. That 10,000 ohms forms a voltage divider with the input impedance of the transistor. Using equation 4 and ignoring r_b, the input impedance is the parallel combination of $\beta(R_E + r_e)$ and R_B. Solving for the input impedance: 300(180 + 15.6) in parallel with 1.5 × 10^6 = 56.470 ohms. Due to the voltage divider formed by the generator and the input impedance of the transistor, the voltage that appears at the base of the transistor is equal to:

$$\left(\frac{56{,}470}{56{,}470 + 10{,}000}\right) V_{in} = 0.85\ V_{in}$$

Since the transistor receives only .85V_{in}, the overall voltage gain of the circuit is the voltage gain of the transistor multiplied by 0.85. The voltage gain of the transistor is calculated using equation 7: A_V = 2100/195.6 = 10.74. The voltage gain for the overall circuit is 10.74 × .85, or 9.1. That is slightly below our desired gain of 10. To increase the gain, R_E must be reduced.

Similar procedures can be used to design common-collector and common-base circuits.

FET amplifiers

Few differences exist between the design procedures for a bipolar transistor amplifier and the design procedures for amplifiers using JFET's and MOSFET's. (The MOSFET is also commonly called an IGFET.) Thus, many of the parameters and design procedures that we've discussed so far can be applied to JFET and MOSFET amplifiers. The primary difference involves the polarity of the bias voltage that is applied to the gate of those devices. (The gate is the equivalent of the base terminal of a bipolar transistor.) In the equations used for determining gain and impedance, there are no distinctions between the FET devices and the bipolar transistor.

The three basic circuit configurations

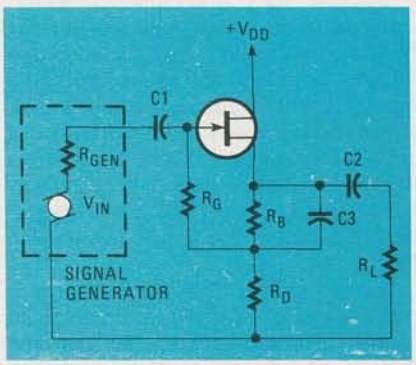

FIG. 5—COMMON-DRAIN FET AMPLIFIER circuit is shown here.

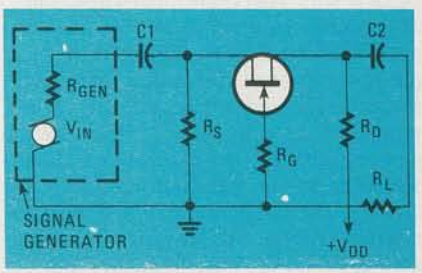

FIG. 6—COMMON-GATE FET AMPLIFIER circuit is mainly used in high-frequency applications.

for the JFET are shown in Figs. 4 through 6. Although the configurations are shown using JFET's, the MOSFET can be substituted instead of the JFET's in those circuits. The common-gate circuit drawn in Fig. 6 is seldom used in audio applications. It is primarily used in high-frequency applications.

Voltage gain as well as the input and output impedances, are the primary concerns of the designer. Because of the high input-impedance of both the JFET and MOSFET devices, the input current is just about zero. Thus, the current gain and the power gain of the device approaches infinity. There are, of course, limits to those gains. Here, the only gain to be considered is voltage gain, A_v. It is related to the transconductance of the FET, g_m. (We will use the term FET to refer to both JFET and MOSFET devices.)

As you may recall, transconductance is

the ratio of a change in drain current to a change in gate voltage. The voltage gain of an FET device in the common-source arrangement is the transconductance multiplied by the AC load impedance connected to the drain of the FET. In Fig. 4, that load impedance is the parallel combination of R_L and R_D. Thus, the equation for calculating the gain of the circuit is:

$$A_v = \frac{g_m (R_D \| R_L)}{1 + g_m R_s} \quad (11)$$

That equation, and the fact that the input and output impedance are R_G and R_D respectively, was noted in the article that appeared in the September 1982 issue. But a complication still exists.

Because of the high input-impedance, capacitance between terminals of the FET become significant. That factor is relatively unimportant when analyzing bipolar transistor circuits because the internal resistance of the bipolar transistor is low. The low internal resistance effectively shorted those capacitances and they had little effect, especially at low operating frequencies. But that is not so with FET's.

As far as the JFET is concerned, capacitances exist between the gate and source, C_{gs}; and between the gate and drain, C_{gd} (sometimes called C_{rss}). When added together, the two capacitances are equal to C_{iss}. That is the input capacitance of a common-source circuit when the output of the transistor is shorted. If the output has a normal load rather than being shorted, the input capacitance is essentially $C_{iss} + g_m R_D C_{gd}$. Because of that capacitance, the gain of the circuit decreases as the operating frequency increases. The frequency at which the gain is down 3 dB (or .707) from its maximum gain is called f_o. That frequency can be calculated using the following equation:

$$f_o = \frac{1}{2\pi R_D (C_{ds} + C_{gd})} \quad (12)$$

It should be noted that the maximum gain is assumed at about $f_o/4$, while it is about 1/2.24 of its maximum gain at $2f_o$, ¼ at $4f_o$, ⅛ at $8f_o$, 1/16 at $16f_o$, and so on.

Note capacitor C_{ds} in equation 12. That is the drain-to-source capacitance. It is negligible in JFET designs, but C_{ds} affects the high-frequency gain significantly in an MOSFET circuit. That is because the drain-to-source resistance (r_{ds}) of the JFET is much lower than the MOSFET. In the JFET, that drain-to-source resistance shunts C_{ds} sufficiently to make it negligible.

You can use equation 12 to calculate the frequency where the gain is down 3 dB from its maximum when the output resistance of the voltage source is insignificant compared to the input resistance of the amplifier. That is frequently true. If, however, the resistance (r_{gen}) is comparable in size to the input impedance of the amplifier, f_o becomes:

$$f_o = \frac{1}{2\pi r_{gen} (C_{iss} + g_m R_D C_{gd})} \quad (13)$$

The general design procedure is to first determine the gain at low frequencies and then calculate f_o by using equation 12 or 13. As an example, let's consider the circuit shown in Fig. 4 where R_D = 12,000 ohms, R_L = 10,000 ohms, R_S = 470 ohms, R_G = 470,000 ohms, and r_{gen} = 470,000 ohms. Let's also assume that the FET has the following parameters: V_p = 3 volts, I_{DSS} = 2 mA, r_{ds} = 5,000 ohms, C_{gs} = 7.5 pF and C_{gd} = 2 pF. Determine the various characteristics of the circuit.

First, we must calculate g_m at the quiescent operating point. To calculate g_m, we must know the drain current. It is:

$$I_D = I_{DSS}\left(1 - \frac{|V_{GS}|}{|V_p|}\right) = 2\times10^{-3}\left(1 - \frac{|V_{GS}|}{3}\right)^2$$

We do not know V_{GS}, but can determine it from the following equation.

$$V_{GS} = I_D R_S = 470\, I_D$$

Substituting V_{GS} into the equation for I_D and solving for I_D, we find it equal to 1.27 mA. Consequently, $V_{GS} = 470 I_D$ = 0.597 volt.

Using that information, we can find g_m:

$$g_m = \frac{2I_{DSS}}{V_p}\left(1 - \frac{|V_{GS}|}{|V_p|}\right) = \frac{2(2\times10^{-3})}{3}\left(1 - \frac{0.597}{3}\right) = 10.68\times10^{-4}$$

Now, we can use equation 11 to determine the AC voltage gain, which calculates out to be 3.88. If a large-value capacitor were across R_S, the shorted resistor would be considered as being at 0 ohms in equation 11. The equation would then be $g_m (R_D \| R_L)$ = 5.82. With the capacitor in the source circuit, the gain has been increased by (5.82 − 3.88) 100/ 3.88 = 50%.

The input impedance seen by the generator is R_C and that is 470,000 ohms. Since the generator and R_G are both 470,000 ohms, half of the generator's voltage appears at the input of the transistor. Because of that, the gain of the overall circuit including the generator, is just one-half of the gain of the transistor circuit with only its load and biasing components.

Because the generator's impedance is significant, the gain is down 3 dB of the maximum at 9783 Hz. That is determined by substituting 4.7×10^5 for r_{gen}, 9×10^{-12} for C_{iss}, 10.68×10^{-4} for g_m, 1.2×10^4 for R_D, and 2×10^{-12} for C_{gd} in equation 13.

Load resistance R_L sees an output impedance equal to R_D or 12,000 ohms, in parallel with the drain-to-source resistance r_{ds}, which is specified as 5000 ohms. That is true only if R_S is shunted by a large capacitor. Otherwise, the resistance increases to R_D in parallel with R_{out}. With R_s = 470 ohms, as stated previously, output impedance R_{out} is equal to:

$$r_{ds} + (1 + g_m r_{ds}) R_S = 7480 \text{ ohms}$$

As for the common-drain circuit, the input impedance is equal to the resistor at the gate input, while the output impedance seen by the load is essentially R_S shunted by $1/g_m$. The gain is approximately equal to 1.

The common-gate circuit has a voltage gain equal to:

$$A_v = \frac{g_m R_D}{1 + g_m R_S} \quad (14)$$

The circuit has a low input impedance that is equal to $R_S + 1/g_m$. The output impedance as seen by the load is approximately equal to R_D. Because of its low input impedance, the significance of the capacitances at the input of the circuit are minimal. Hence, the circuit is used primarily in high frequency applications.

Noise

The amplifiers described so far are used to amplify low-level signals. Because of that, the relationship between the amount of noise present in the amplifier and the level of the input signal is significant. To determine the noise contribution of the circuit, we must first determine the lowest significant frequency reproduced by the amplifier (f_L) and the highest significant frequency reproduced by the amplifier (f_H). Then, a signal with a frequency equal to $\sqrt{f_H f_L}$ is fed to the circuit and its maximum undistorted output voltage is noted. The signal is removed and the remaining output voltage is noise. The ratio of signal voltage to noise voltage, expressed in dB, is:

$$dB = 20 \log_{10} \frac{V_{so}}{V_{no}} = 10 \log_{10} \frac{P_{so}}{P_{no}} \quad (15)$$

Two noise specifications are frequently used in data sheets. Those are the noise factor, F, and the noise figure, NF. They are related by the equation NF = $\log_{10}$ F. F is defined by the equation:

$$F = \frac{P_{si} / P_{ni}}{P_{so} / P_{no}} \quad (16)$$

where P_{si} is the input power, P_{ni} is the noise at the input generated by the circuit feeding the amplifier, P_{so} is power at the output and P_{no} is noise at the output. Low noise-figures and noise factors are most desirable for a transistor used at the input of an audio amplifier.

Curves are available to help you design low-noise circuits. It is a long and tedious task to apply those curves and they usual-

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ly give you no better results than you will get by applying a few rules of thumb. First choose a transistor where F or NF is low. From there on, rules differ for the different types of transistors.

When designing a bipolar transistor circuit, use the smallest practical resistor at the input to the base that is consistent with the functioning of the circuit. As a second rule, keep the idling collector voltage and current at a minimum.

As for FET's, choose a low-noise device with a high g_m. Next, bias the device as close to the I_{DSS} curve as possible to make V_{GS} as close to 0 volt as practical. Finally, do not necessarily use a small input resistor. There is one resistance at the input that will put the noise at a minimum. That value should be determined experimentally through the use of a substitution resistance box across the input circuit.

Increasing gain

We found the gain of a one-stage amplifier to be pretty low. To get more gain, we must connect the output of one transistor to the input of a second transistor. Now the gain of two or more devices determine the overall gain of the circuit. In the next article, we will cover the design procedures for accomplishing that goal. **R-E**