CHAPTER 11: OVERVOLTAGE EFFECTS ON ANALOG INTEGRATED CIRCUITS

◘ BASIC LINEAR DESIGN

CHAPTER 11: OVERVOLTAGE EFFECTS ON ANALOG INTEGRATED CIRCUITS

SECTION 11.1: OVERVOLTAGE EFFECTS

One of the most commonly asked applications questions is: "What happens if external voltages are applied to an analog integrated circuit with the supplies turned off?" This question describes situations that can take on many different forms: from lightning strikes on cables which propagate very high transient voltages into signal conditioning circuits, to walking across a carpet and then touching a printed circuit board full of sensitive precision circuits. Regardless of the situation, the general issue is the effect of overvoltage stress (and, in some cases, abuse) on analog integrated circuits. The discussion which follows will be limited in general to operational amplifiers, because it is these devices that most often interface to the outside world. The principles developed here can and should be applied to all analog integrated circuits which are required to condition or digitize analog waveforms. These devices include (but are not limited to) instrumentation amplifiers, analog comparators, sample-and-hold amplifiers, analog switches and multiplexers, and analog-to-digital converters.

Amplifier Input Stage Overvoltage

In real world signal conditioning, sensors are often used in hostile environments where faults can and do occur. When these faults take place, signal conditioning circuitry can be exposed to large voltages which exceed the power supplies. The likelihood for damage is quite high, even though the components' power supplies may be turned on. Published specifications for operational amplifier absolute maximum ratings state that applied input signal levels should never exceed the power supplies by more than 0.3 V or, in some devices, 0.7 V. Exceeding these levels exposes amplifier input stages to potentially destructive fault currents which flow through internal metal traces and parasitic P-N junctions to the supplies. Without some type of current limiting, unprotected input differential pairs (BJTs or FETs) can be destroyed in a matter of microseconds. There are, however, some devices with built-in circuitry that can provide protection beyond the supply voltages, but in general, absolute maximum ratings must still be observed.

Although more recent vintage operational amplifiers designed for single-supply or rail-to-rail operation are now including information with regard to input stage overvoltage effects, there are very many amplifiers available today without such information provided by the manufacturer. In those cases, the circuit designer using these components must ascertain the input stage current-voltage characteristic of the device in question before

steps can be taken to protect it. All amplifiers will conduct current to the positive/negative supply, provided the applied input voltage exceeds some internal threshold. This threshold is device dependent, and can range from 0.7 V to 30 V, depending on the internal construction of the input stage. Regardless of the threshold level, externally generated fault currents should be limited to no more than ±5 mA.

- **INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS (Usually Specified With Respect to Supply Voltages)**
- **A Common Specification Requires the Input Signal < $|V_s| \pm 0.3$ V**
- **Input Voltage Should be Held Near Zero in the Absence of Supplies**
- **Input Stage Conduction Current Needs to be Limited (Rule of Thumb: ≤ 5 mA)**
- **Avoid Reverse Bias Junction Breakdown in Input Stage Base - Emitter Junctions**
- **Differential and Common-Mode Ratings may Differ**
- **No Two Amplifiers are exactly the Same**
- **Some Op Amps Contain Input Protection (Voltage Clamps, Current Limits, or Both), but Absolute Maximum Ratings Must Still be Observed**

Figure 11.1: *Input Stage Overvoltage*

Many factors contribute to the current-voltage characteristic of an amplifier's input stage: internal differential clamping diodes, current-limiting series resistances, substrate potential connections, and differential input stage topologies (BJTs or FETs). Input protection diodes used as differential input clamps are typically constructed from the base-emitter junctions of NPN transistors. These diodes usually form a parasitic P-N junction to the negative supply when the applied input voltage exceeds the negative supply. Current-limiting series resistances used in the input stages of operational amplifiers can be fabricated from three types of material: N- or P-type diffusions, polysilicon, or thin-films (SiCr, for example). Polysilicon and thin-film resistors are fabricated over thin layers of oxide which provide an insulating barrier to the substrate; as such, they do not exhibit any parasitic P-N junctions to either supply. Diffused resistors, on the other hand, exhibit P-N junctions to the supplies because they are constructed from either P- or N-type diffusion regions. The substrate potential of the amplifier is the most critical component, for it will determine the sensitivity of an amplifier's input current-voltage characteristic to supply voltage.

The configuration of the amplifier's input stage also plays a large role in the current-voltage characteristic of the amplifier. Input differential pairs of operational amplifiers are constructed from either bipolar transistors (NPN or PNP) or field-effect transistors (junction or MOS, N- or P-channel). While the bipolar input differential pairs do not have any direct path to either supply, FET differential pairs do. For example, an N-channel JFET forms a parasitic P-N junction between its backgate and the P-substrate that

energizes when $V_{IN} + 0.7\ V < V_{NEG}$. As mentioned previously, many manufacturers of analog integrated circuits do not provide any details with regard to the behavior of the device's input structure. Either simplified schematics are not provided or, if they are shown, the behavior of the input stage under an overvoltage condition is omitted. Therefore, other measures must be taken in order to identify the conduction paths.

A standard transistor curve tracer can be configured to determine the current-voltage characteristic of any amplifier regardless of input circuit topology. Both amplifier supply pins are connected to ground, and the collector output drive is connected to one of the amplifier's inputs. The curve tracer applies a DC ramp voltage and measures the current flowing through the input stage. In the event that a transistor curve tracer is not available, a DC voltage source and a multimeter can be substituted for the curve tracer. A 10 kΩ resistor should be used between the DC voltage source and the amplifier input for additional protection. Ammeter readings from the multimeter at each applied DC voltage will yield the same result as that produced by the curve tracer. Although either input can be tested (both inputs should), it is recommended that the unused input is left open; otherwise, additional junctions could come into play and would complicate matters further. Evaluations of current feedback amplifier input stages are more difficult because of the lack of symmetry between the inputs. As a result, both inputs should be characterized for their individual current-voltage characteristics.

- **Junctions may be Forward Biased if the Current is Limited**
- **In General a Safe Current Limit is 5mA**
- **Reverse Bias Junction Breakdown is Damaging Regardless of the Current Level**
- **When in Doubt, Protect with External Diodes and Series Resistances**
- **Curve Tracers Can be Used to Check the Overvoltage Characteristics of a Device**
- **Simplified Equivalent Circuits in Data Sheets do not tell the Entire Story!!!**

Figure 11.2: *Overvoltage Effects*

Once the input current-voltage characteristic has been determined for the device in question, the next step is to determine the minimum level of resistance required to limit fault currents to ± 5 mA. Equation 11.1 illustrates the computation for R_S when the input overvoltage level is known:

$$R_S = \frac{V_{IN(MAX)} - V_{SUPPLY}}{5\ mA} \qquad \text{Eq. 11-1}$$

The worst case condition for overvoltage would be when the power supplies are initially turned off or disconnected. In this case, V_{SUPPLY} is equal to zero. For example, if the

input overvoltage could reach 100 V under some type of fault condition, then the external resistor should be no smaller than 20kΩ. Most operational amplifier applications only require protection at one input; however, there are a few configurations (difference amplifiers, for example) where both inputs can be subjected to overvoltage and both must be protected. The need for protection on both inputs is much more common with instrumentation amplifiers.

- **Sometimes Occurs in FET and Bipolar Input (Especially Single-Supply) Op Amps when Input Exceeds Common Mode Range**
- **Does Not Harm Amplifier, but may be Disastrous in Servo Systems!**
- **Not Usually Specified on Data Sheet, so Amplifier Must be Checked**
- **Easily Prevented:**

BiFETs:	**Add Appropriate Input Series Resistance (Determined Empirically, Unless Provided in Data Sheet)**
Bipolars:	**Use Schottky Diode Clamps to the Supply Rails.**

Figure 11.3: BEWARE OF AMPLIFIER OUTPUT PHASE REVERSAL

Amplifier Output Voltage Phase Reversal

Some operational amplifiers exhibit output voltage phase reversal when one or both of their inputs exceeds their input common-mode voltage range. Phase reversal is usually associated with JFET (n- or p-channel) input amplifiers, but some bipolar devices (especially single-supply amplifiers operating as unity-gain followers) may also be susceptible. In the vast majority of applications, output voltage phase reversal does not harm the amplifier nor the circuit in which the amplifier is used. Although a number of operational amplifiers suffer from phase reversal, it is rarely a problem in system design. However, in servo loop applications, this effect can be quite hazardous. Fortunately, this is only a temporary condition. Once the amplifier's inputs return to within its normal operating common-mode range, output voltage phase reversal ceases. It may still be necessary to consult the amplifier manufacturer, since phase reversal information rarely appears on device data sheets.

In BiFET operational amplifiers, phase reversal may be prevented by adding an appropriate resistance in series with the amplifier's input to limit the current. Bipolar

input devices can be protected by using a Schottky diode to clamp the input to within a few hundred millivolts of the negative rail. For a complete description of the output voltage phase reversal effect, please consult Reference 1.

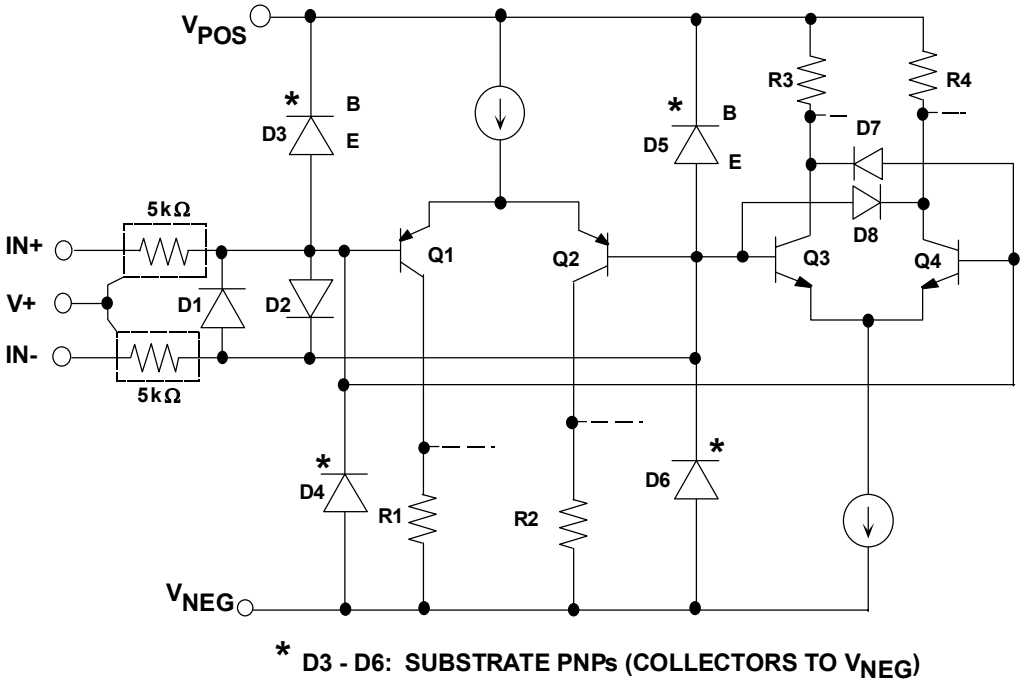


Figure 11.4: *A Closer Look at the OP-X91 Input Stage Reveals Additional Devices*

Rail-to-rail operational amplifiers present a special class of problems to the integrated circuit designer, because these types of devices should not exhibit any abnormal behavior throughout the entire input common-mode range. In fact, it is desirable that devices used in these applications also not exhibit any abnormal behavior if the applied input voltages exceed the power supply range. One of the more recent vintage rail-to-rail input/output operational amplifiers, the OPX91 family (the OP191, the OP291, and the OP491), includes additional components that prevent overvoltage and damage to the device. As shown in Figure 11.4, the input stage of the OPX91 devices use six diodes and two resistors to clamp the input terminals to each other and to the supplies. D1 and D2 are base-emitter NPN diodes which are used to protect the bases of Q 1- Q2 and Q3 - Q4 against avalanche breakdown when the applied differential input voltage to the device exceeds 0.7 V. Diodes D3 - D6 are diodes formed from substrate PNP transistors that clamp the applied input voltages on the OPX91 to the supply rails.

An interesting benefit from using substrate PNPs as clamp diodes is that their collectors are connected to the negative supply; thus, when the applied input voltage exceeds either supply rail, the diodes energize, and the fault currents are diverted directly to the supply and not through or into the device's input stage. There are also 5kΩ resistors in series with each of the inputs to the OPX91 to limit the fault current through D1 and D2 when

the differential input voltage exceeds 0.7 V. Note that these 5 kΩ resistors are p-type diffusions placed inside an n-well, which is then connected to the positive supply. When the applied input voltage exceeds the positive supply, some of the fault current generated is also diverted to V_{POS} and away from the input stage. As a result of these measures, the input overvoltage characteristic of the OPX91 is well behaved as shown in Figure 11.6. Note that the combination of the 5 kΩ resistors and clamp diodes safely limits the input current to less than 2 mA, even when the inputs of the device exceed the supply rails by 10 V.

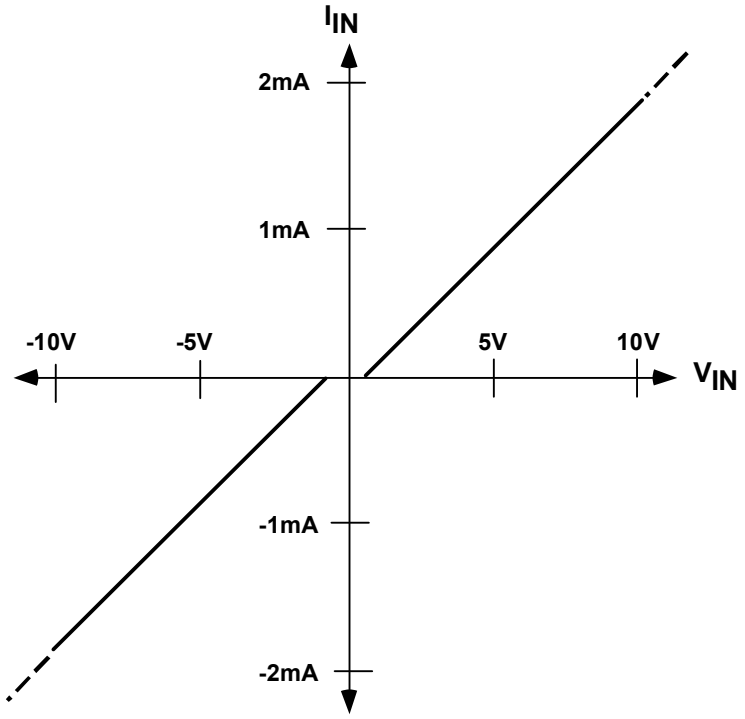


Figure 11.5: *Internal 5 kΩ Resistors Plus Input Clamp Diodes Combine to Protect OP-X91 Devices Against Overvoltage*

As an added safety feature, an additional pair of diodes is used in the input stage across Q3 and Q4 to prevent subsequent stages internal to the OPX91 from collapsing (that is, forced into cutoff). If these stages were forced into cutoff, then the amplifier would undergo output voltage phase reversal when the inputs exceeded the positive input common mode voltage. An illustration of the diodes' effectiveness is shown in Figure 11.6. Here, the OPX91 family can safely handle a 20 Vp-p input signal on ±5 V supplies without exhibiting any sign of output voltage phase reversal or other anomalous behavior. With these amplifiers, no external clamping diodes are required.

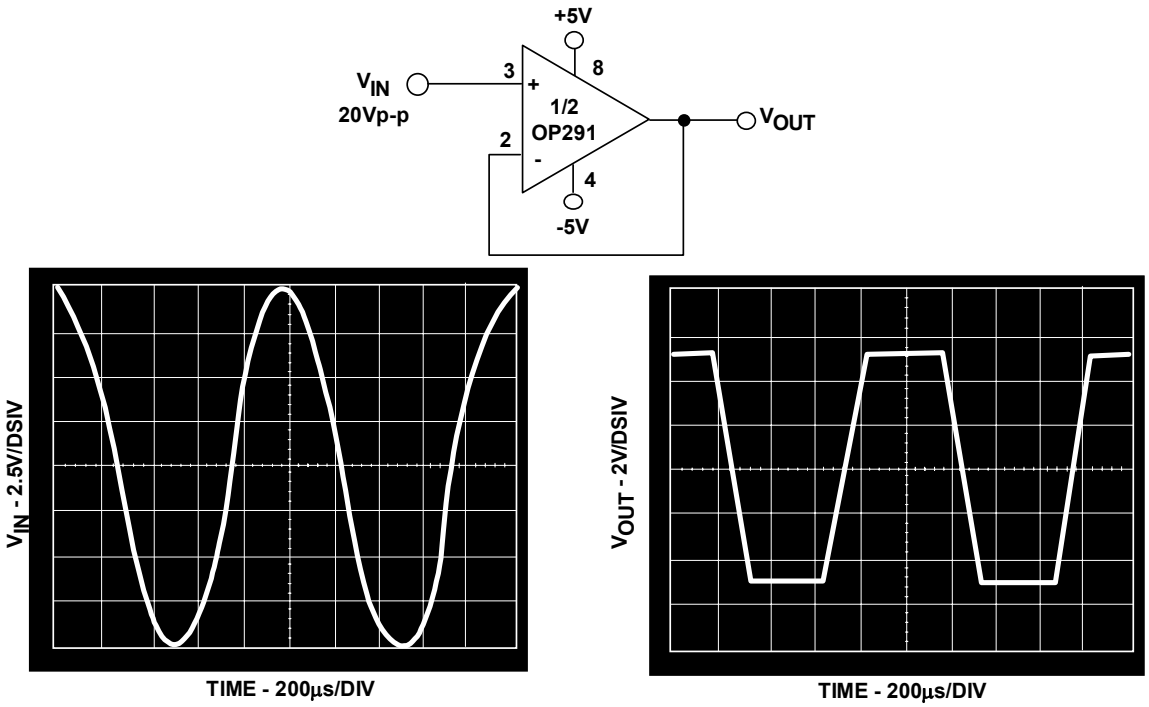
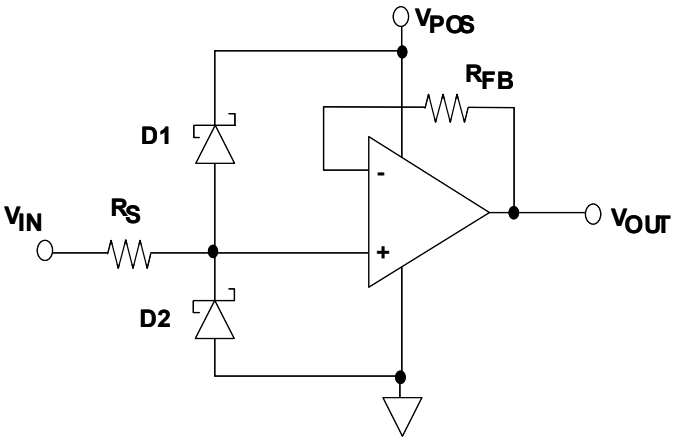


Figure 11.6: *Addition of Two Clamp Diodes Protects OP-X91 Devices Against Output Phase Reversal*



Value for R_S provided by manufacturer or determined empirically

R_{FB} may be required for high bias current devices

D1 and D2 can be Schottky diodes (Check their capacitance and leakage current first)

Figure 11.7: *Generalized External Protection Schemes Against Input Overvoltage Abuse and Output Voltage Phase Reversal in Single Supply Op Amps*

For those amplifiers where external protection is clearly required against both overvoltage abuse and output phase reversal, a common technique is to use a series

resistance, R_S, to limit fault current, and Schottky diodes to clamp the input signal to the supplies, as shown in Figure 11.7.

The external input series resistance, R_S, will be provided by the manufacturer of the amplifier, or determined empirically by the user with the method previously shown in Figure 11.2 and Eq. 11.1. More often than not, the value of this resistor will provide enough protection against output voltage phase reversal, as well as limiting the fault current through the Schottky diodes.

It is evident that whenever resistance is added in series with an amplifier's input, its offset and noise performance will be affected. The effects of this series resistance on circuit noise can be calculated using the following equation.

$$E_{n,total} = \sqrt{\left(e_{n,op\,amp}\right)^2 + \left(e_{n,R_S}\right)^2 + \left(R_S \cdot i_{n,op\,amp}\right)^2} \qquad \text{Eq. 11-2}$$

The thermal noise of the resistor, the voltage noise due to amplifier noise current flowing through the resistor, and the input noise voltage of the amplifier are added together (in root-sum-square manner, since the noise voltages are uncorrelated) to determine the total input noise and may be compared with the input voltage noise in the absence of the protection resistor.

A protection resistor in series with an amplifier input will also produce a voltage drop due to the amplifier bias current flowing through it. This drop appears as an increase in the circuit offset voltage (and, if the bias current changes with temperature, offset drift). In amplifiers where bias currents are approximately equal, a resistor in series with each input will tend to balance the effect and reduce the error. The effects of this additional series resistance on the circuit's overall offset voltage can be calculated:

$$V_{os(total)} = V_{os} + I_b R_S \qquad \text{Eq. 11-3}$$

For the case where $R_{FB} = R_S$ or where the source impedance levels are balanced, then the total circuit offset voltage can be expressed as:

$$V_{os(total)} = V_{os} + I_{os} R_S \qquad \text{Eq. 11-4}$$

To limit the additional noise of R_{FB}, it can be shunted with a capacitor.

When using external clamp diodes to protect operational amplifier inputs, the effects of diode junction capacitance and leakage current should be evaluated in the application. Diode junction capacitance and R_S will add an additional pole in the signal path, and diode leakage currents will double for every 10°C rise in ambient temperature. Therefore, low leakage diodes should be used such that, at the highest ambient temperature for the application, the total diode leakage current is less than one-tenth of the input bias current for the device at that temperature. Another issue with regard to the use of Schottky diodes is the change in their forward voltage drop as a function of temperature. These diodes do

not, in fact, limit the signal to ±0.3 V at all ambient temperatures, but if the Schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is true if over-voltage is only possible at turn-on, when the diodes and the op amp will always be at the same temperature. If the op amp is warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature.

Notes:

SECTION 11.2: ELECTROSATIC DISCHARGE (ESD)

Understanding and Protecting Integrated Circuits from Electrostatic Discharge (ESD)

Integrated circuits can be damaged by the high voltages and high peak currents that can be generated by electrostatic discharge. Precision analog circuits, which often feature very low bias currents, are more susceptible to damage than common digital circuits, because the traditional input-protection structures which protect against ESD damage also increase input leakage.

The keys to eliminating ESD damage are: (1) awareness of the sources of ESD voltages, and (2) understanding the simple handling steps that will discharge potential voltages safely.

- **ESD (Electrostatic Discharge):**
  - **A single fast, high current transfer of electrostatic charge.**
    - **Direct contact between two objects at different potentials.**
    - **A high electrostatic field between two objects when they are in close proximity.**
- **ESD Failure Threshold:**
  - **The highest voltage level at which all pins on a device can be subjected to ESD zaps without failing any 25°C data sheet limits.**

Figure 11.8: *ESD Definitions*

The basic definitions relating to ESD are given in Figure 11.8. Notice that the *ESD Failure Threshold* level relates to any of the IC data sheet limits, and not simply to a *catastrophic failure* of the device. Also, the limits apply to each pin of the IC, not just to the input and output pins.

The generation of static electricity caused by rubbing two substances together is called the *triboelectric effect*. Static charge can be generated either by dissimilar materials (for example, rubber-soled shoes moving across a rug) or by separating similar materials (for example, pulling transparent tape off of a roll).

A wide variety of common human activities can create high electrostatic charge. Some examples are given in Figure 11.9. The values shown will occur with a fairly high relative humidity. Low humidity, such as can occur indoors during cold weather, can generate voltages 10 times (or more) greater than the values shown.

- **Person walks across a typical carpet.**
  - **1000 - 1500V generated**
- **Person walks across a typical vinyl floor.**
  - **150 - 250V generated**
- **Person handles instructions protected by clear plastic covers.**
  - **400 - 600V generated**
- **Person handles polyethylene bags.**
  - **1000 - 1200V generated**
- **Person pours polyurethane foam into a box.**
  - **1200 - 1500V generated**
- **An IC slides down a grounded handler chute.**
  - **50 - 500V generated**
- **An IC slides down an open conductive shipping tube.**
  - **25 - 250V generated**

Note: Above values can occur in a high (≈60%) RH environment. For low RH (≈30%), generated voltages can be >10 times those listed above!

Figure 11.9: *Examples of ESD Generation*

In an effort to standardize the testing and classification of integrated circuits for ESD robustness, ESD models have been developed (Figure 11.10). These models attempt to simulate the source of ESD voltage. The assumptions underlying the three commonly-used models are different, so results are not directly comparable.

- **Three Models:**
  1. **Human Body Model (HBM)**
  2. **Machine Model (MM)**
  3. **Charged Device Model (CDM)**
- **Model Correlation:**
  - **Low - Assumptions are Different**

Figure 11.10: *Modeling Electrostatic Potential*

The most-often encountered ESD model is the Human Body Model (HBM). This model simulates the approximate resistance and capacitance of a human body with a simple RC network. The capacitor is charged through a high voltage power supply (HVPS) and then discharged (using a high voltage switch) through a series resistor. The RC values for different individuals will, of course, vary. However, the HBM has been standardized by MIL-STD-883 Method 3015 Electrostatic Discharge Sensitivity Classification, which specifies R-C combinations of 1.5 kΩ and 100 pF. (R, C, and L values for all three ESD models are shown in Figure 11.12.)

- **Human Body Model (HBM)**

  Simulates the discharge event that occurs when a person charged to either a positive or negative potential touches an IC at a different potential.

  RLC: R = 1.5kΩ, L ≈ 0nH, C =100pF

- **Machine Model (MM)**

  Non-real-world Japanese model based on worst-case HBM.

  RLC: R ≈ 0Ω, L ≈ 500nH, C = 200pF

- **Charged Device Model (CDM)**

  Simulates the discharge that occurs when a pin on an IC, charged to either a positive or negative potential, contacts a conductive surface at a different (usually ground) potential.

  RLC: R = 1 Ω L ≈ 0nH, C = 1 - 20pF

Figure 11.11: *ESD Models Applicable to ICs*

The Machine Model (MM) is a worst-case Human Body Model. Rather than using an *average* value for resistance and capacitance of the human body, the MM assumes a worst-case value of 200 pF and 0Ω. The 0Ω output resistance of the MM is also intended to simulate the discharge from a charged conductive object (for example, a charged DUT socket on an automatic test system) to an IC pin, which is how the Machine Model earned its name. However, the MM does not simulate many known real-world ESD events. Rather, it models the ESD event resulting from a ideal voltage source (in other words, with no resistance in the discharge path). EIAJ Specification ED-4701 Test Method C-111 Condition A and ESD Association Specification S5.2 provide guidelines for MM testing.

The Charged Device Model (CDM) originated at AT&T. This model differs from the HBM and the MM, in that the source of the ESD energy is the IC itself. The CDM assumes that the integrated circuit die, bond wires, and lead frame are charged to some potential (usually positive with respect to ground). One or more of the IC pins then contacts ground, and the stored charge rapidly discharges through the leadframe and

bond wires. Typical examples of triboelectric charging followed by a CDM discharge include:
1. An IC slides down a handler chute and then a corner pin contacts a grounded stop bar.

2. An IC slides down an open conductive shipping tube and then a corner pin contacts a conductive surface.

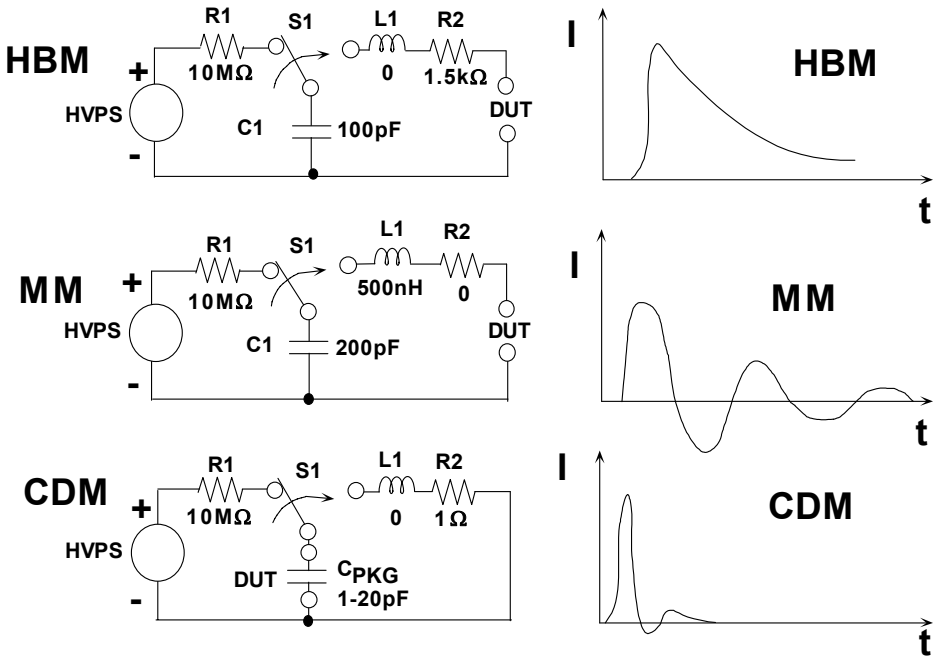


Figure 11.12: Schematic Representations of ESD Models and Typical Discharge Waveforms

The basic concept of the CDM is different than the HBM and MM in two ways. First, the CDM simulates a charged IC discharging to ground, while the HBM and MM both simulate a charged source discharging into the IC. Thus, current flows out of the IC during CDM testing, and into the IC during HBM and MM testing. The second difference is that the capacitor in the CDM is the capacitance of the package, while the HBM and MM use a fixed external capacitor.

Unlike the HBM and MM, CDM ESD thresholds may vary for the same die in different packages. This occurs because the device under test (DUT) capacitance is a function of the package. For example, the capacitance of an 8-pin package is different than the capacitance of a 14-pin package. CDM capacitance values can vary from about 1 to 20 pF. The device capacitance is discharged through a 1 Ω resistor.

Schematic representations of the three models are shown in Figure 11.13. Notice that C1 in the HBM and MM are external capacitors, while C_{PKG} in the CDM is the internal capacitance of the DUT.
The HBM discharge waveform is a predicable unipolar RC pulse, while the MM discharge shows ringing because of the parasitic inductance in the discharge path (typically 500 nH.). Ideally, the CDM waveform is also a single unipolar pulse, but the parasitic inductance in series with the 1 Ω resistor slows the rise time and introduces some ringing.

MODEL:	HBM	MM	SOCKETED CDM
Simulate:	Human Body	Machine	Charged Device
Origin:	US Military, Late 1960s	Japan, 1976	AT&T,1974
Real World?	Yes	Generally	Yes
RC:	1.5 kΩ, 100 pF	0 Ω, 200 pF	1 Ω , 1 – 20 pF
Rise Time	<10 ns (6-9 ns typ)	14 ns*	400 ps**
Ipeak at 400V	0.27 A	5.8 A*	2.1 A**
Energy:	Moderate	High	Low
Package Dependent:	No	No	Yes
Standard:	MIL-STD-883 Method 3015	ESD Association Std. S5.2; EIAJ Std. ED-4701, Method C-111	ESD Association Draft Std. DS5.3

* These values per ESD Association Std. S5.2.
EIAJ Std. ED-4701, Method C-111 includes no waveform specifications.
** These values are for the direct charging (socketed) method.

Figure 11.13: *Comparison of HBM, MM, AND CDM ESD Models*

The significant features of each ESD model are summarized in Figure 11.13. The peak currents shown for each model are based on a test voltage of 400 V. Peak current is lowest for the HBM because of the relatively high discharge resistance. The CDM discharge has low energy because device capacitance is only in the range of 1 pF to 20 pF, but peak current is high. The MM has the highest energy discharge, because it has the highest capacitance value (Power = 0.5 CV^2).

Figure 11.14 compares 400 V discharge waveforms of the CDM, MM, and HBM, with the same current and time scales.

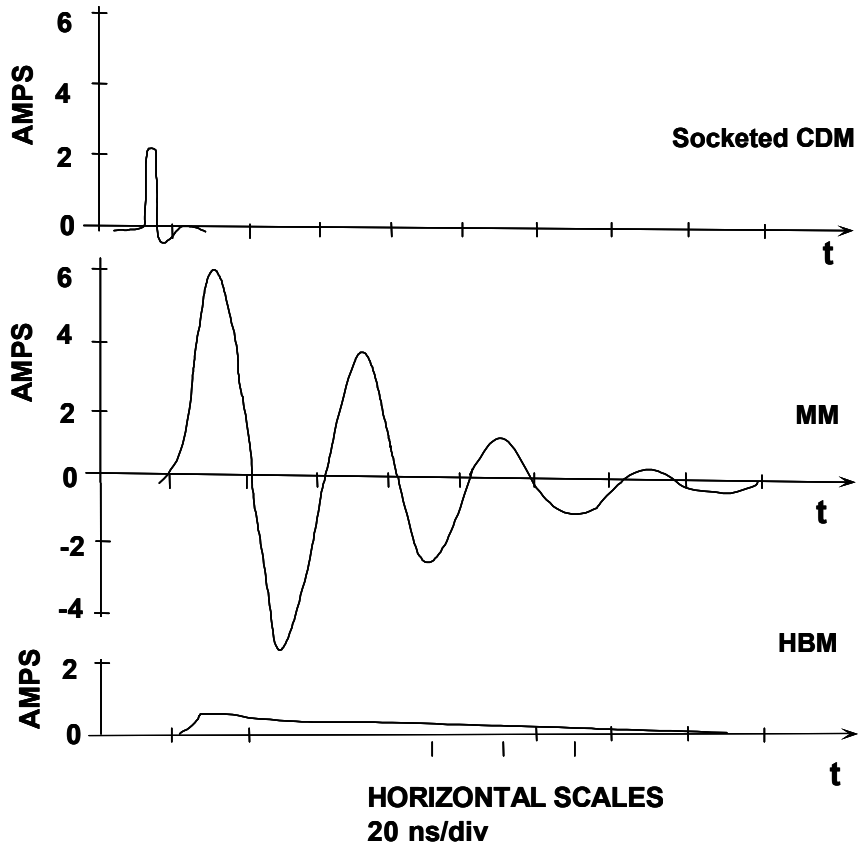


Figure 11.14: *Relative Comparison of 400 V HBM, MM, AND CDM Discharges*

The CDM waveform corresponds to the shortest known real-world ESD event. The waveform has a rise time of <1 ns, with the total duration of the CDM event only about 2 ns. The CDM waveform is essentially unipolar, although some ringing occurs at the end of the pulse that results in small negative-going peaks. The very short duration of the overall CDM event results in an overall discharge of relatively low energy, but peak current is high.

The MM waveform consists of both positive- and negative-going sinusoidal peaks, with a resonance frequency of 10 MHz to 15 MHz. The initial MM peak has a typical rise time of 14 ns, and the total pulse duration is about 150 ns. The multiple high current, moderate duration peaks of the MM result in an overall discharge energy that is by far the highest of the three models for a given test voltage.

The risetime for the unipolar HBM waveform is typically 6 - 9 ns, and the waveform decays exponentially towards 0 V with a fall time of approximately 150 ns. (Method 3015 requires a rise time of <10 ns and a delay time of 150 ns ± 20 ns, with decay time defined as the time for the waveform to drop from 100% to 36.8% of peak current). The peak current for the HBM is 400 V/1500 Ω or 0.267 A, which is much lower than is

produced by 400 V CDM and MM events. However, the relatively long duration of the total HBM event still results in an overall discharge of moderately high energy.
As previously noted, the MM waveform is bipolar while HBM and CDM waveforms are primarily unipolar. However, HBM and CDM testing is done with both positive and negative polarity pulses. Thus all three models stress the IC in both directions.

MIL-STD-883 Method 3015 classifies ICs for ESD failure threshold. The classification limits, shown in Figure 11.15, are derived using the HBM shown in Figure 11.13. Method 3015 also mandates a marking method to denote the ESD classification. All military grade Class 1 and 2 devices have their packages marked with one or two "Δ" symbols, respectively, while class 3 devices (with a failure threshold >4 kV) do not have any ESD marking. Commercial and industrial grade IC packages may not be marked with any ESD classification symbol.

HBM ESD CLASS	FAILURE THRESHOLD	MARKING
1	<2 kV	Δ
2	2 kV – <4 kV	Δ Δ
3	>4 kV	None

Note: Commercial and Industrial ICs are not marked for ESD

Figure 11.15: *Classifying and Marking ICs for ESD Per MIL-883C, METHOD 3015*

Notice that the Class 1 limit includes all devices which do not pass a 2 kV threshold. However, a Class 1 rating does not imply that all devices within that class will pass 1,999 V. In any event, the emphasis must be placed on eliminating ESD exposure, not on attempting to decide how much ESD exposure is 'safe.'

- **ESD Failure Mechanisms:**
  - **Dielectric or junction damage**
  - **Surface charge accumulation**
  - **Conductor fusing.**
- **ESD Damage Can Cause:**
  - **Increased leakage**
  - **Reduced performance**
  - **Functional failures of ICs.**
- **ESD Damage is often Cumulative:**
  - **For example, each ESD "zap" may increase junction damage until, finally, the device fails.**

Figure 11.16: *Understanding ESD Damage*

A detailed discussion of IC failure mechanisms is beyond the scope of this seminar, but some typical ESD effects are shown in Figure 11.17.

- **ESD DAMAGE *CANNOT* BE "CURED"!**

- **Circuits cannot be *tweaked*, *nulled*, *adjusted*, etc., to compensate for ESD damage.**

ESD DAMAGE MUST BE *PREVENTED*!

Figure 11.17: *The Most Important Thing to Remember about ESD Damage*

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered.

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is *prevention*. There is no way to un-do ESD damage, or to compensate for its effects.

Two key elements in protecting circuits from ESD damage are:

- **Recognizing ESD-sensitive products**

- **Always handling ESD-sensitive products at a *grounded* workstation**

Figure 11.18: *Preventing ESD Damage to ICs*

Since ESD damage can not be undone, the only cure is prevention. Luckily, prevention is a simple two-step process. The first step is recognizing ESD-sensitive products, and the second step is understanding how to handle these products.

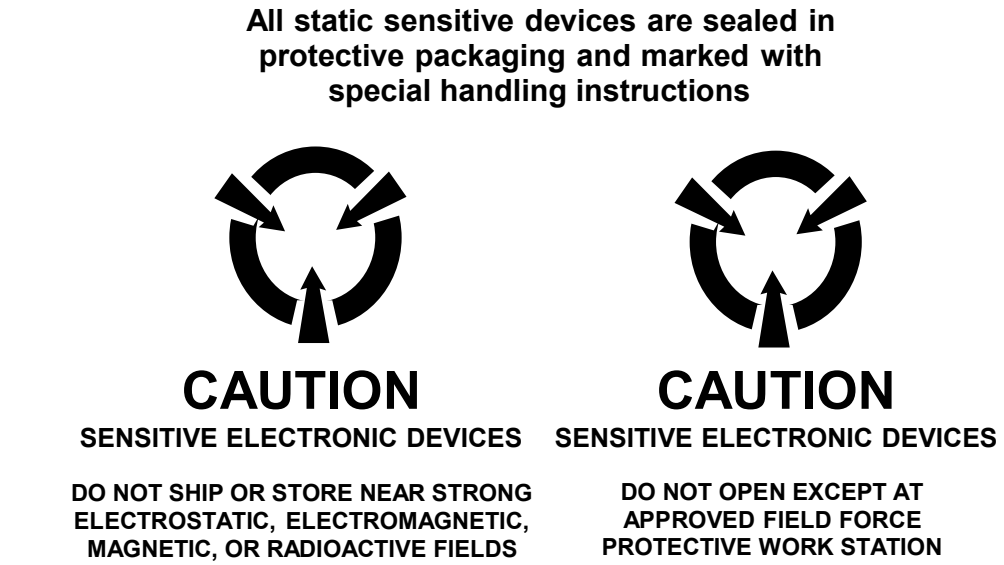
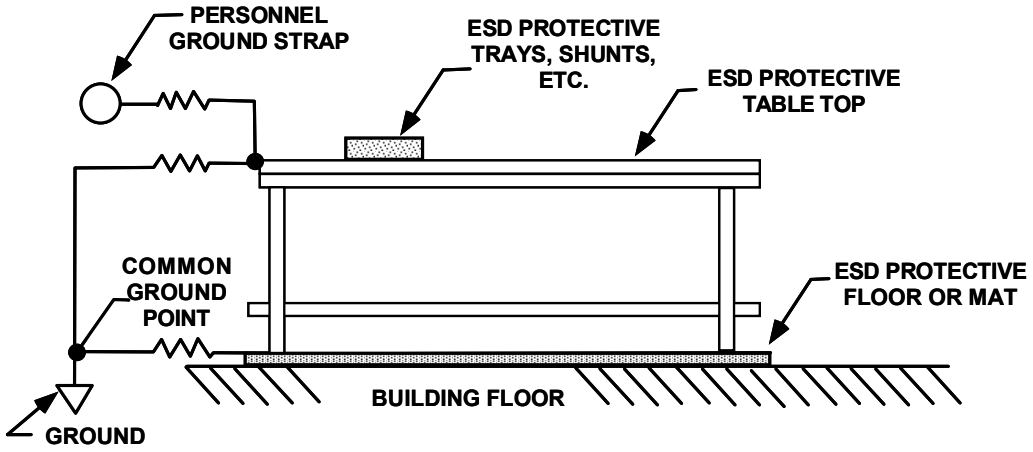


Figure 11.19 *Recognizing ESD Sensitive Devices*

All static sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or in antistatic tubes. Either way, the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as is shown in Figure 11.20, which outlines the appropriate handling procedures.



Note: Conductive table top sheet resistance » 10^6 Ω / □

Figure 11.20: *Workstation for Handling ESD-Sensitive Devices*

Once ESD-sensitive devices are identified, protection is easy. Obviously, keeping ICs in their original protective packaging as long as possible is the first step. The second step is to discharge potential ESD sources before damage to the IC can occur. The HBM capacitance is only 100pF, so discharging a potentially dangerous voltage can be done quickly and safely through a high impedance. Even with a source resistance of 10MΩ, the 100pF will be discharged in less than 100milliseconds.

The key component required for safe ESD handling is a workbench with a static-dissipative surface, as shown in Figure 11.20. This surface is connected to ground through a 1 MΩ resistor, which dissipates static charge while protecting the user from electrical shock hazards caused by ground faults. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with a discharge resistor.

- **Analog Devices is committed to helping our customers prevent ESD damage by:**
  - **Building products with the highest level of ESD protection commensurate with performance requirements**
  - **Protecting products from ESD during shipment**
  - **Helping customers to avoid ESD exposure during manufacture**

Figure 11.21: *Analog Devices Commitment*

Notice that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, the CDM assumes that a high peak current will flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the surface shown in Figure 11.20, however, the peak current is not high enough to damage the device.

A conductive wrist strap is also recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape off of packages, will not cause damage to ICs. Again, a 1 MΩ resistor, from the wrist strap to ground, is required for safety.

When building prototype breadboards or assembling PC boards which contain ESD-sensitive devices, all passive components should be inserted and soldered before the ICs. This procedure minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy (Figure 11.22)

ANALOG DEVICES:

- **Circuit Design and Fabrication -**

  Design and manufacture products with the highest level of ESD protection consistent with required analog and digital performance.

- **Pack and Ship -**

  Pack in static dissipative material. Mark packages with ESD warning.

CUSTOMERS:

- **Incoming Inspection -**

  Inspect at grounded workstation. Minimize handling.

- **Inventory Control -**

  Store in original ESD-safe packaging. Minimize handling.

- **Manufacturing -**

  Deliver to work area in original ESD-safe packaging. Open packages only at grounded workstation. Package subassemblies in static dissipative packaging.

- **Pack and Ship -**

  Pack in static dissipative material if required. Replacement or optional boards may require special attention.

Figure 11.22 *ESD Protection Requires a Partnership Between the IC Supplier and the Customer*

A complete ESD protection plan, however, requires more than building-ESD protection into ICs. Users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures.

Notes:

SECTION 11.3: EMI/RFI CONSIDERATIONS

Electromagnetic interference (EMI) has become a hot topic in the last few years among circuit designers and systems engineers. Although the subject matter and prior art have been in existence for over the last 50 years or so, the advent of portable and high-frequency industrial and consumer electronics has provided a comfortable standard of living for many EMI testing engineers, consultants, and publishers. With the help of EDN Magazine and Kimmel Gerke Associates, this section will highlight general issues of EMC (electromagnetic compatibility) to familiarize the system/circuit designer with this subject and to illustrate proven techniques for protection against EMI.

A Primer on EMI Regulations

The intent of this section is to summarize the different types of electromagnetic compatibility (EMC) regulations imposed on equipment manufacturers, both voluntary and mandatory. Published EMC regulations apply at this time only to equipment and systems, and not to components. Thus, EMI *hardened* equipment does not necessarily imply that each of the components used (integrated circuits, especially) in the equipment must also be EMI *hardened*.

Commercial Equipment

The two driving forces behind commercial EMI regulations are the FCC (Federal Communications Commission) in the U. S. and the VDE (Verband Deutscher Electrotechniker) in Germany. VDE regulations are more restrictive than the FCC's with regard to emissions and radiation. The European Community added immunity to RF, electrostatic discharge, and power-line disturbances to the VDE regulations in 1996. In Japan, commercial EMC regulations are covered under the VCCI (Voluntary Control Council for Interference) standards and, implied by the name, are much looser than their FCC and VDE counterparts.

All commercial EMI regulations primarily focus on *radiated* emissions, specifically to protect nearby radio and television receivers, although both FCC and VDE standards are less stringent with respect to *conducted* interference (by a factor of 10 over radiated levels). The FCC Part 15 and VDE 0871 regulations group commercial equipment into two classes: Class A, for all products intended for business environments; and Class B, for all products used in residential applications. For example, Table 11.1 illustrates the electric-field emission limits of commercial computer equipment for both FCC Part 15 and VDE 0871 compliance.

In addition to the already stringent VDE emission limits, the European Community EMC standards (IEC and IEEE) require mandatory compliance to these additional EMI threats: Immunity to RF fields, electrostatic discharge, and power-line disturbances. All equipment/systems marketed in Europe must exhibit an immunity to RF field strengths of

1-10V/m (IEC standard 801-3), electrostatic discharge (generated by human contact or through material movement) in the range of 10 kV to 15 kV (IEC standard 801-2), and power-line disturbances of 4kV EFTs (extremely fast transients, IEC standard 801-4) and 6 kV lightning surges (IEEE standard C62.41).

Radiated Emission Limits for Commercial Computer Equipment

Frequency (MHz)	Class A (at 3 m)	Class B (at 3 m)
30 to 88	300 μV/m	100 μV/m
88 to 216	500 μV/m	150 μV/m
216 to 1000	700 μV/m	200 μV/m

Table 11.1

Military Equipment

The defining EMC specification for military equipment is MIL-STD-461 which applies to radiated equipment emissions and equipment susceptibility to interference. Radiated emission limits are very typically 10 to 100 times more stringent than the levels shown in Table 11.1. Required limits on immunity to RF fields are typically 200 times more stringent (RF field strengths of 5 to 50 mV/m) than the limits for commercial equipment.

Medical Equipment

Although not yet mandatory, EMC regulations for medical equipment are presently being defined by the FDA (Food and Drug Administration) in the USA and the European Community. The primary focus of these EMC regulations will be on immunity to RF fields, electrostatic discharge, and power-line disturbances, and may very well be more stringent than the limits spelled out in MIL-STD-461. The primary objective of the medical EMC regulations is to guarantee safety to humans.

Automotive Equipment

Perhaps the most difficult and hostile environment in which electrical circuits and systems must operate is that found in the automobile. All of the key EMI threats to electrical systems exist here. In addition, operating temperature extremes, moisture, dirt, and toxic chemicals further exacerbate the problem. To complicate matters further, standard techniques (ferrite beads, feedthrough capacitors, inductors, resistors, shielded cables, wires, and connectors) used in other systems are not generally used in automotive applications because of the cost of the additional components.

Presently, automotive EMC regulations, defined by the very comprehensive SAE Standards J551 and J1113, are not yet mandatory. They are, however, very rigorous. SAE standard J551 applies to vehicle-level EMC specifications, and standard J1113 (functionally similar to MIL-STD-461) applies to all automotive electronic modules. For example, the J1113 specification requires that electronic modules cannot radiate electric fields greater than 300nV/m at a distance of 3 meters. This is roughly 1000 times more stringent than the FCC Part 15 Class-A specification. In many applications, automotive manufacturers are imposing J1113 RF field immunity limits on *each of the active components* used in these modules. Thus, in the very near future, automotive manufacturers will require that IC products comply with existing EMC standards and regulations.

EMC Regulations' Impact on Design

In all these applications and many more, complying with mandatory EMC regulations will require careful design of individual circuits, modules, and systems using established techniques for cable shielding, signal and power-line filtering against both small- and large-scale disturbances, and sound multilayer PCB layouts. The key to success is to incorporate sound EMC principles early in the design phase to avoid time-consuming and expensive redesign efforts.

Passive Components: Your Arsenal Against EMI

Minimizing the effects of EMI requires that the circuit/system designer be completely aware of the primary arsenal in the battle against interference: *passive components*. To successfully use these components, the designer must understand their non-ideal behavior. For example, Figure 11.47 illustrates the *real* behavior of the passive components used in circuit design. At very high frequencies, wires become transmission lines, capacitors become inductors, inductors become capacitors, and resistors behave as resonant circuits.

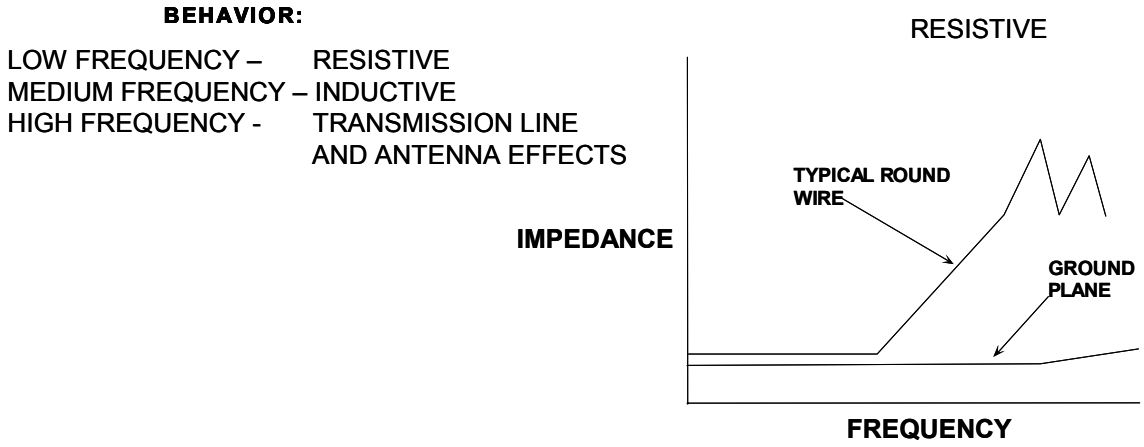


Figure 11.23: *Impedance Comparison: Wire vs. Ground Plane*

A specific case in point is the frequency response of a simple wire compared to that of a ground plane. In many circuits, wires are used as either power or signal returns, and there is no ground plane. A wire will behave as a very low resistance (less than 0.02 Ω/ft for 22-gauge wire) at low frequencies, but because of its parasitic inductance of approximately 20 nH/ft, it becomes inductive at frequencies above 160 kHz. Furthermore, depending on size and routing of the wire and the frequencies involved, it ultimately becomes a transmission line with an uncontrolled impedance. From our knowledge of RF, unterminated transmission lines become antennas with gain, as illustrated in Figure 11.26. On the other hand, large area ground planes are much more well-behaved, and maintain a low impedance over a wide range of frequencies. With a good understanding of the behavior of *real* components, a strategy can now be developed to find solutions to most EMI problems.

With any problem, a strategy should be developed before any effort is expended trying to solve it. This approach is similar to the scientific method: initial circuit misbehavior is noted, theories are postulated, experiments designed to test the theories are conducted, and results are again noted. This process continues until all theories have been tested and expected results achieved and recorded. With respect to EMI, a problem solving framework has been developed. As shown in Figure 11.24, the model suggested by Kimmel-Gerke in [Reference 1] illustrates that all three elements (a *source*, a *receptor* or *victim*, and a *path* between the two) must exist in order to be considered an EMI problem. The sources of electromagnetic interference can take on many forms, and the ever-increasing number of portable instrumentation and personal communications/computation equipment only adds the number of possible sources and receptors.

Interfering signals reach the receptor by *conduction* (the circuit or system interconnections) or *radiation* (parasitic mutual inductance and/or parasitic capacitance). In general, if the frequencies of the interference are less than 30 MHz, the primary means by which interference is coupled is through the *interconnects*. Between 30 MHz and 300 MHz, the primary coupling mechanism is *cable radiation and connector leakage*. At frequencies greater than 300 MHz, the primary mechanism is *slot and board radiation*. There are many cases where the interference is broadband, and the coupling mechanisms are combinations of the above.

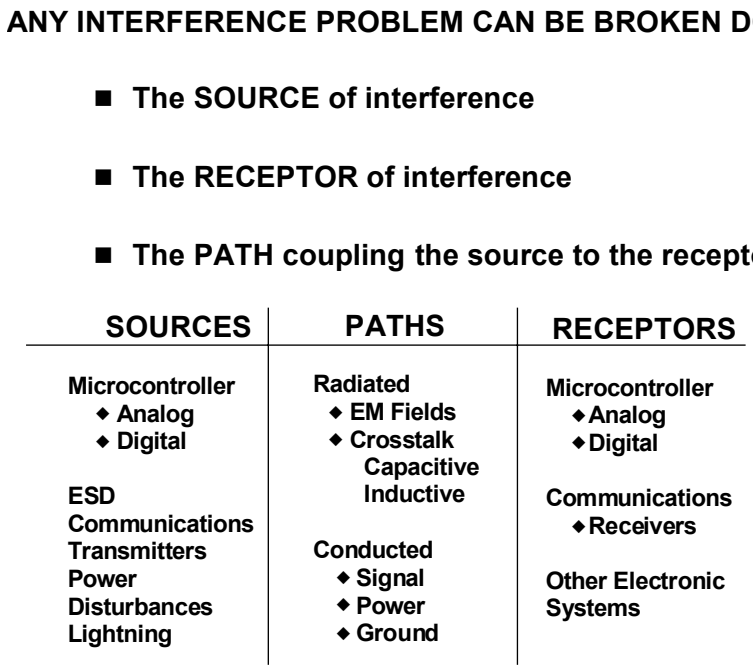


Figure 11.24: *A Diagnostic Framework for EMI*

When all three elements exist together, a framework for solving any EMI problem can be drawn from Figure 11.25. There are three types of interference with which the circuit or system designer must contend. The first type of interference is that generated by and emitted from an instrument; this is known as circuit/system *emission* and can be either *conducted* or *radiated*. An example of this would be the personal computer. Portable and desktop computers must pass the stringent FCC Part 15 specifications prior to general use.

The second type of interference is circuit or system *immunity*. This describes the behavior of an instrument when it is exposed to large electromagnetic fields, primarily electric fields with an intensity in the range of 1 to 10 V/m at a distance of 3 meters. Another term for immunity is *susceptibility*, and it describes circuit/system behavior against radiated or conducted interference.

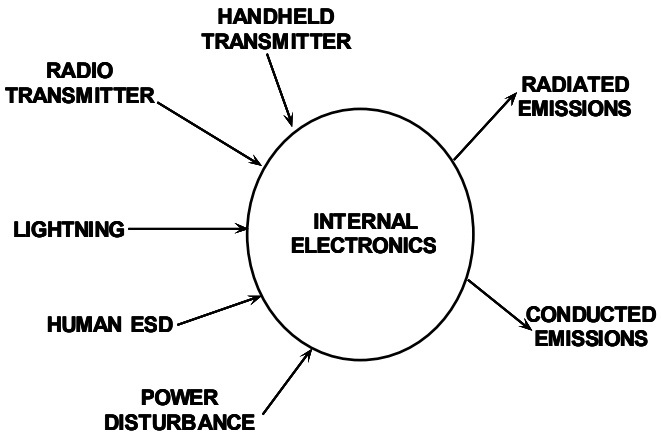


Figure 11.25: *Three Types of Interference: Emissions – Immunity – Internal*

The third type of interference is *internal*. Although not directly shown on the figure, internal interference can be high speed digital circuitry within the equipment which affects sensitive analog (or other digital circuitry), or noisy power supplies which can contaminate both analog and digital circuits. Internal interference often occurs between digital and analog circuits, or between motors or relays and digital circuits. In mixed signal environments, the digital portion of the system often interferes with analog circuitry. In some systems, the internal interference reaches such high levels that even very high speed digital circuitry can affect other low-speed digital circuitry as well as analog circuits.

In addition to the source-path-receptor model for analyzing EMI-related problems, Kimmel Gerke Associates have also introduced the FAT-ID concept [Reference 1]. FAT-ID is an acronym that describes the five key elements inherent in any EMI problem. These five key parameters are: *frequency*, *amplitude*, *time*, *impedance*, and *distance*.

The *frequency* of the offending signal suggests its path. For example, the path of low-frequency interference is often the circuit conductors. As the interference frequency increases, it will take the path of least impedance, usually stray capacitance. In this case, the coupling mechanism is radiation.

Time and frequency in EMI problems are interchangeable. In fact, the physics of EMI have shows that the time response of signals contains all the necessary information to construct the spectral response of the interference. In digital systems, both the signal rise time and pulse repetition rate produce spectral components according to the following relationship:

$$f_{EMI} = \frac{1}{\pi \cdot t_{rise}} \qquad \text{Eq. 11-5}$$

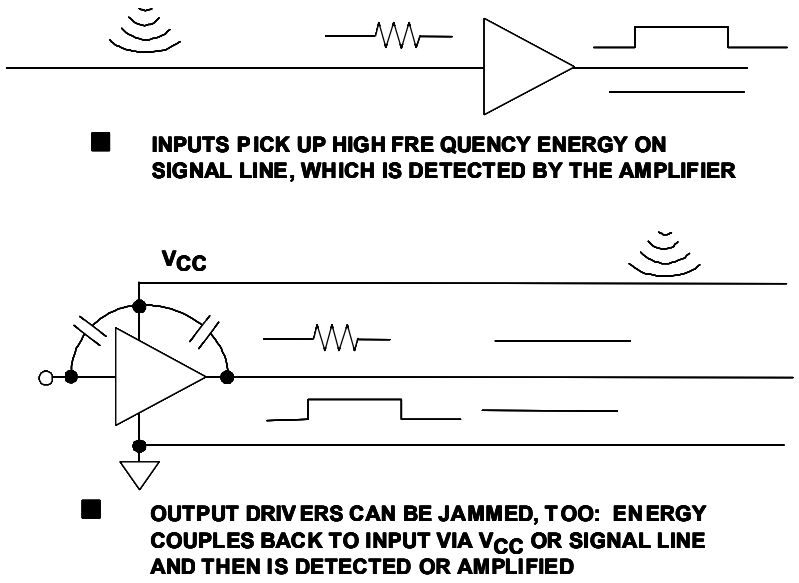


Figure 11.26: *RFI Can Cause Rectification in Sensitive Analog Circuits*

For example, a pulse having a 1 ns rise time is equivalent to an EMI frequency of over 300 MHz. This time-frequency relationship can also be applied to high speed analog circuits, where slew rates in excess of 1000 V/μs and gain-bandwidth products greater than 500 MHz are not uncommon.

When this concept is applied to instruments and systems, EMI emissions are again functions of signal rise time and pulse repetition rates. Spectrum analyzers and high speed oscilloscopes used with voltage and current probes are very useful tools in quantifying the effects of EMI on circuits and systems.

Another important parameter in the analysis of EMI problems is the physical dimensions of cables, wires, and enclosures. Cables can behave as either passive antennas (receptors) or very efficient transmitters (sources) of interference. Their physical length and their shield must be carefully examined where EMI is a concern. As previously mentioned, the behavior of simple conductors is a function of length, cross-sectional area, and frequency. Openings in equipment enclosures can behave as slot antennas, thereby allowing EMI energy to affect the internal electronics.

Radio Frequency Interference (RFI)

The world is rich in radio transmitters: radio and TV stations, mobile radios, computers, electric motors, garage door openers, electric jackhammers, and countless others. All this electrical activity can affect circuit/system performance and, in extreme cases, may render it inoperable. Regardless of the location and magnitude of the interference, circuits/systems must have a minimum level of immunity to radio frequency interference (RFI). The next section will cover two general means by which RFI can disrupt normal instrument operation: the direct effects of RFI sensitive analog circuits, and the effects of RFI on shielded cables.

Two terms are typically used in describing the sensitivity of an electronic system to RF fields. In communications, radio engineers define *immunity* to be an instrument's *susceptibility to the applied RFI power density at the unit*. In more general EMI analysis, the *electric-field intensity* is used to describe RFI stimulus. For comparative purposes, Equation 11-6 can be used to convert electric-field intensity to power density and vice-versa:

$$\vec{E}\left(\frac{V}{m}\right) = 61.4\sqrt{P_T\left(\frac{mW}{cm^2}\right)} \qquad \text{Eq. 11-6}$$

where:

E = Electric Field Strength, in volts per meter, and
P_T = Transmitted power, in milliwatts per cm^2.

From the standpoint of the source-path-receptor model, the *strength of the electric field*, E, surrounding the receptor is a function of *transmitted power*, *antenna gain*, and *distance* from the source of the disturbance. An approximation for the electric-field intensity (for both near- and far-field sources) in these terms is given by Equation 11-7:

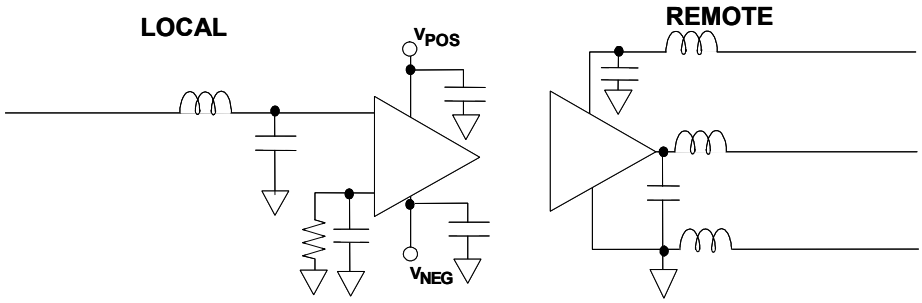
$$\vec{E}\left(\frac{V}{m}\right) = 5.5\left(\frac{\sqrt{P_T \cdot G_A}}{d}\right) \qquad \text{Eq. 11-7}$$

where:

E = Electric field intensity, in V/m;
P_T = Transmitted power, in mW/cm^2;
G_A = Antenna gain (numerical); and
d = distance from source, in meters

For example, a 1 W hand-held radio at a distance of 1 meter can generate an electric-field of 5.5 V/m, whereas a 10 kW radio transmission station located 1 km away generates a field smaller than 0.6 V/m.

Analog circuits are generally more sensitive to RF fields than digital circuits because analog circuits, operating at high gains, must be able to resolve signals in the microvolt/millivolt region. Digital circuits, on the other hand, are more immune to RF fields because of their larger signal swings and noise margins. As shown in Figure 11.27, RF fields can use inductive and/or capacitive coupling paths to generate noise currents and voltages which are amplified by high impedance analog instrumentation. In many cases, out-of-band noise signals are detected and rectified by these circuits. The result of the RFI rectification is usually unexplained offset voltage shifts in the circuit or in the system.



Decouple all voltage supplies to analog chip with high-frequency capacitors

Use high-frequency filters on all lines that leave the board

Use high-frequency filters on the voltage reference if it is not grounded

Figure 11.27: *Keeping RFI Away from Analog Circuits*

There are techniques that can be used to protect analog circuits against interference from RF fields (see Figure 11.28). The three general points of RFI coupling are *signal inputs*, *signal outputs*, and *power supplies*. At a minimum, all power supply pin connections on analog and digital ICs should be decoupled with 0.1 µF ceramic capacitors. As was shown in Reference 3, low-pass filters, whose cutoff frequencies are set no higher than 10 to 100 times the signal bandwidth, can be used at the inputs and the outputs of signal conditioning circuitry to filter noise.

Care must be taken to ensure that the low-pass filters (LPFs) are effective at the highest RF interference frequency expected. As illustrated in Figure 11.28, real low-pass filters may exhibit *leakage* at high frequencies. Their inductors can lose their effectiveness due to parasitic capacitance, and capacitors can lose their effectiveness due to parasitic inductance. A rule of thumb is that a conventional low-pass filter (made up of a single capacitor and inductor) can begin to *leak* when the applied signal frequency is 100 to 1000 higher than the filter's cutoff frequency. For example, a 10 kHz LPF would not be considered very efficient at filtering frequencies above 1 MHz.

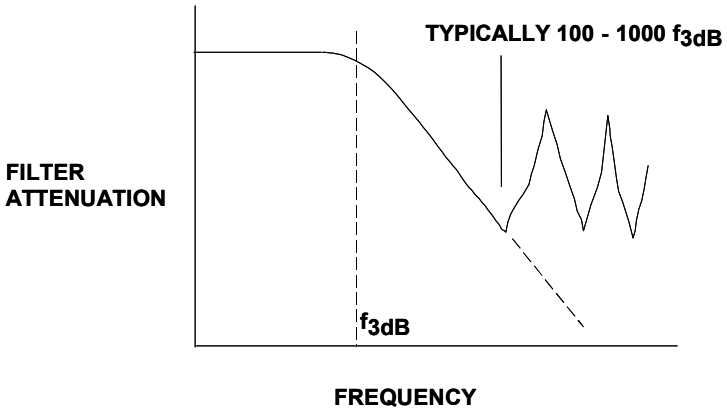


Figure 11.28: *Single Low Power Low Pass Filter Loses Effectiveness at 100 – 1000 f_{3dB}*

Rather than use one LPF stage, it is recommended that the interference frequency bands be separated into *low-band*, *mid-band*, and *high-band*, and then use individual filters for each band. Kimmel Gerke Associates use the stereo speaker analogy of *woofer-midrange-tweeter* for RFI low-pass filter design illustrated in Figure 11.29. In this approach, low frequencies are grouped from 10 kHz to 1 MHz, mid-band frequencies are grouped from 1 MHz to 100 MHz, and high frequencies grouped from 100 MHz to 1 GHz. In the case of a shielded cable input/output, the high frequency section should be located close to the shield to prevent high-frequency leakage at the shield boundary. This is commonly referred to as *feed-through* protection. For applications where shields are not required at the inputs/outputs, then the preferred method is to locate the high frequency filter section as close the analog circuit as possible. This is to prevent the possibility of pickup from other parts of the circuit.

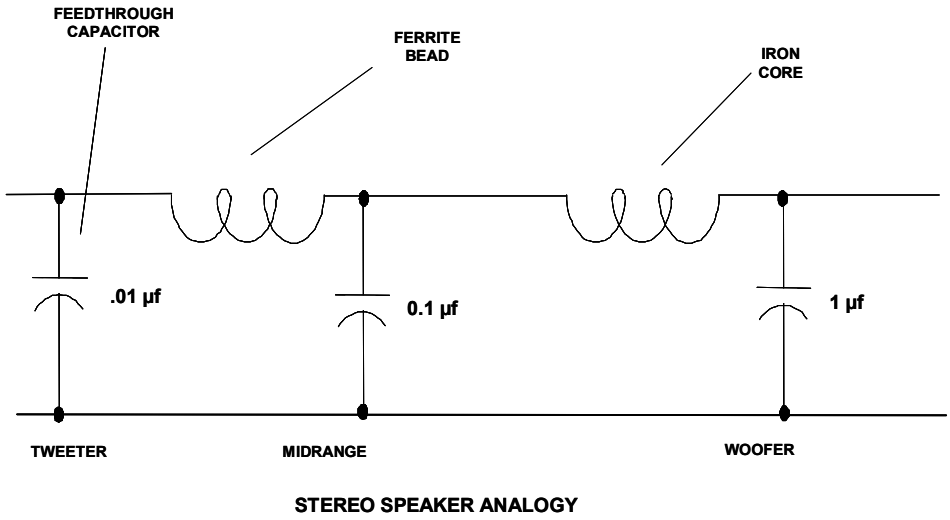


Figure 11.29: *Multistage Filters Are More Effective*

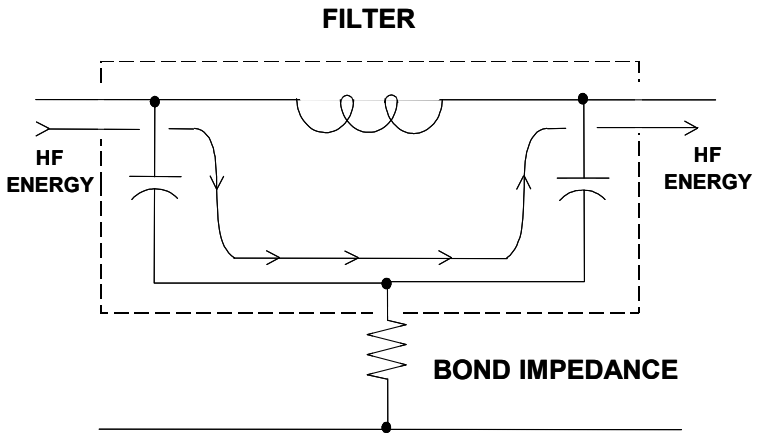


Figure 11.30: *Non-Zero (Inductive and/or Resistive) Filter*

Ground Reduces Effectiveness

Another cause of filter failure is illustrated in Figure 11.31. If there is any impedance in the ground connection (for example, a long wire or narrow trace connected to the ground plane), then the high frequency noise uses this impedance path to bypass the filter completely. Filter grounds must be broadband and tied to low impedance points or planes for optimum performance. High frequency capacitor leads should be kept as short as possible, and low inductance surface-mounted ceramic chip capacitors are preferable.

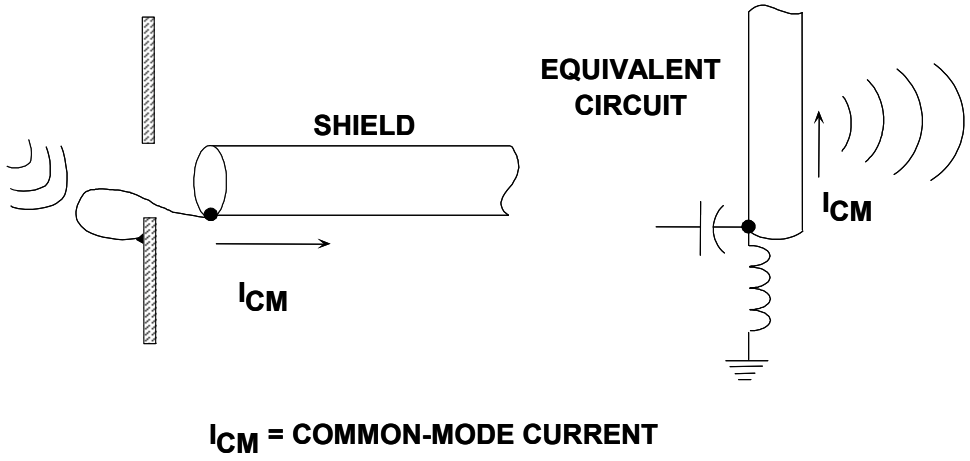


Figure 11.31: *"Shielded" Cable Can Carry High Frequency Current and Behaves as an Antenna*

In the first part of this discussion on RF immunity, circuit level techniques were discussed. In this next section, the second strategic concept for RF immunity will be discussed: *all cables behave as antennas*. As shown in Figure 11.31, pigtail terminations on cables very often cause systems to fail radiated emissions tests because high frequency noise has coupled into the cable shield, generally through stray capacitance. If the length of the cable is considered *electrically long* (a concept to be explained later) at the interference frequency, then it can behave as a very efficient quarter-wave antenna. The cable pigtail forms a matching network, as shown in the figure, to radiate the noise which coupled into the shield. In general, pigtails are only recommended for applications below 10 kHz, such as 50 Hz/60 Hz interference protection. For applications where the interference is greater than 10 kHz, shielded connectors, electrically and physically connected to the chassis, should be used. In applications where shielding is not used, filters on input/output signal and power lines work well. Small ferrites and capacitors should be used to filter high frequencies, provided that: (1) the capacitors have short leads and are tied directly to the chassis ground, and (2) the filters are physically located close to the connectors to prevent noise pickup.

- **Radio-Frequency Interference is a Serious Threat**
  - **Equipment causes interference to nearby radio and television**
  - **Equipment upset by nearby transmitters**
- **RF-Failure Modes**
  - **Digital circuits prime source of emissions**
  - **Analog circuits more vulnerable to RF than digital circuits**
- **Two Strategic Concepts**
  - **Treat all cables as antennas**
  - **Determine the most critical circuits**
- **RF Circuit Protection**
  - **Filters and multilayer boards**
  - **Multistage filters often needed**
- **RF Shielding**
  - **Slots and seams cause the most problems**
- **RF Cable Protection**
  - **High-quality shields and connectors needed for RF protection**

Figure 11.32: *Summary of Radio Frequency Interference and Protection Techniques*

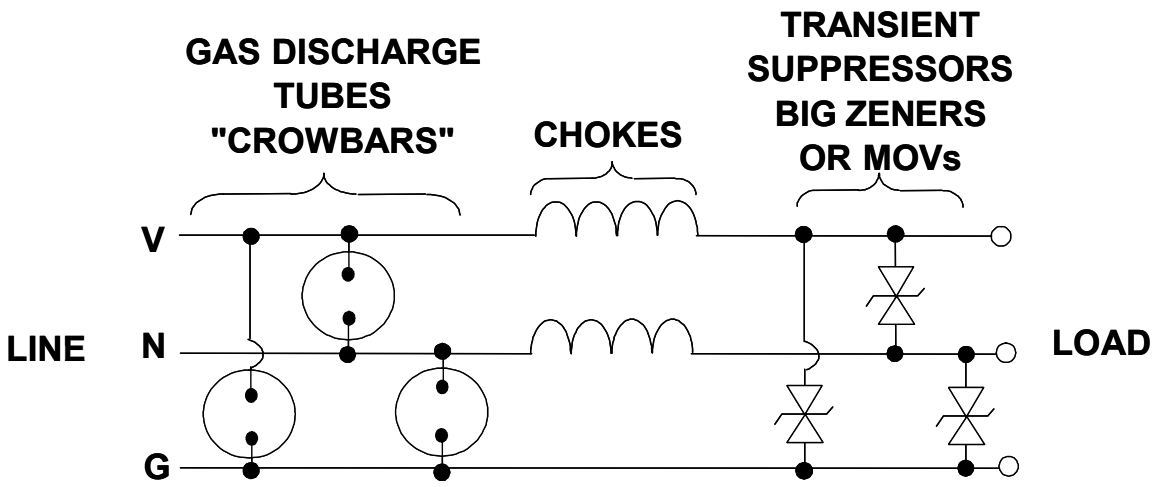


Figure 11.33: *Power Line Disturbances Can Generate EMI*

The key issues and techniques described in this section on solving RFI related problems are summarized in Figure 11.32. Some of the issues were not discussed in detail, but are equally important. For a complete treatment of this issue, the interested reader should consult References 1 and 2. The main thrust of this section was to provide the reader with a problem-solving strategy against RFI and to illustrate solutions to commonly encountered RFI problems.

Solutions for Power-Line Disturbances

The goal of this next section is not to describe in detail all the circuit/system failure mechanisms which can result from power-line disturbances or faults. Nor is it the intent of this section to describe methods by which power-line disturbances can be prevented. Instead, this section will describe techniques that allow circuits and systems to accommodate *transient* power-line disturbances.

Figure 11.34 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10 kV and as fast as 10 ns. Gas discharge tubes (crowbars) and large geometry zener diodes (clamps) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.

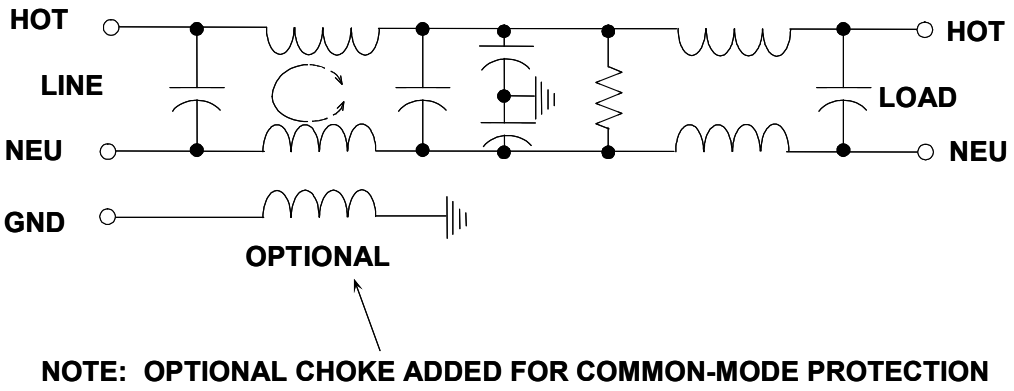


Figure 11.34: *Schematic for a Commercial Power Line Filter*

Commercial EMI filters, as illustrated in Figure 11.34, can be used to filter less catastrophic transients or high frequency interference. These EMI filters provide both common-mode and differential mode filtering. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of this choke cannot be too large, however, because its resistance may affect power-line fault clearing.

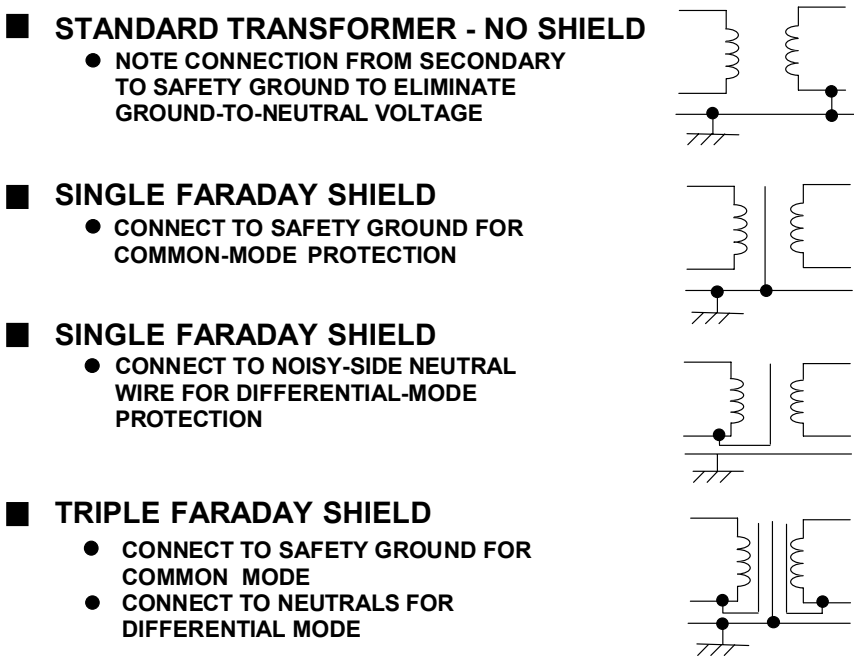


Figure 11.35: *Faraday Shields in Isolation Transformers Provide Increasing Levels of Protection*

Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1 MHz), or for transients with rise and fall times greater than 300 ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10 ns) or those caused by high-amplitude electrostatic discharge (1 ns to 3 ns). As illustrated in Figure 11.36, isolation transformers can be designed for various levels of differential- or common-mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.

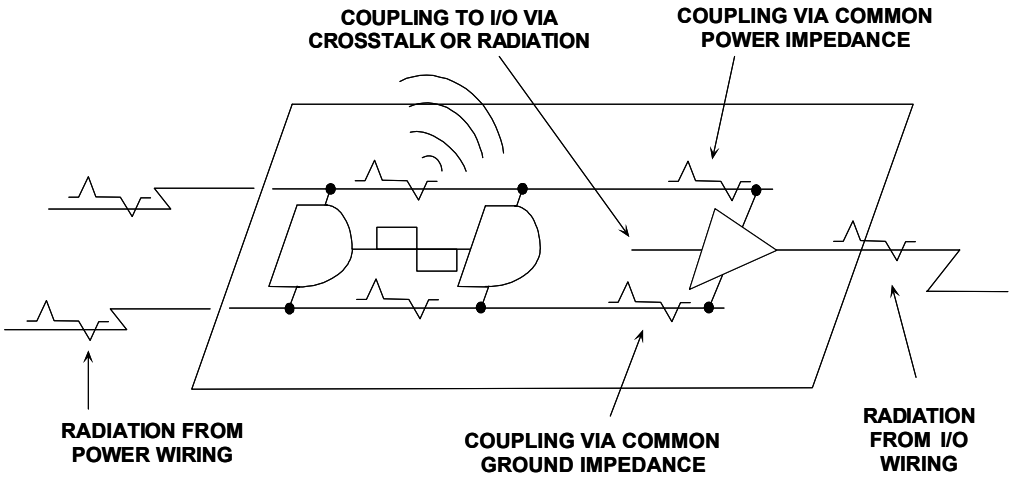


Figure 11.36: *Methods by Which High Frequency Energy Couples and Radiates Into Circuitry Via Placements*

Printed Circuit Board Design for EMI Protection

This section will summarize general points regarding the most critical portion of the design phase: the printed circuit board layout. It is at this stage where the performance of the system is most often compromised. This is not only true for signal-path performance, but also for the system's susceptibility to electromagnetic interference and the amount of electromagnetic energy radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

Figure 11.37 is a real-world printed circuit board layout which shows all the paths through which high-frequency noise can couple/radiate into/out of the circuit. Although the diagram shows digital circuitry, the same points are applicable to precision analog, high speed analog, or mixed analog/digital circuits. Identifying critical circuits and paths helps in designing the PCB layout for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

A key point in minimizing noise problems in a design is to *choose devices no faster than actually required by the application*. Many designers assume that faster is better: fast logic is better than slow, high bandwidth amplifiers are clearly better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed is not required by the system. Unfortunately, faster is not better, but worse where EMI is concerned.

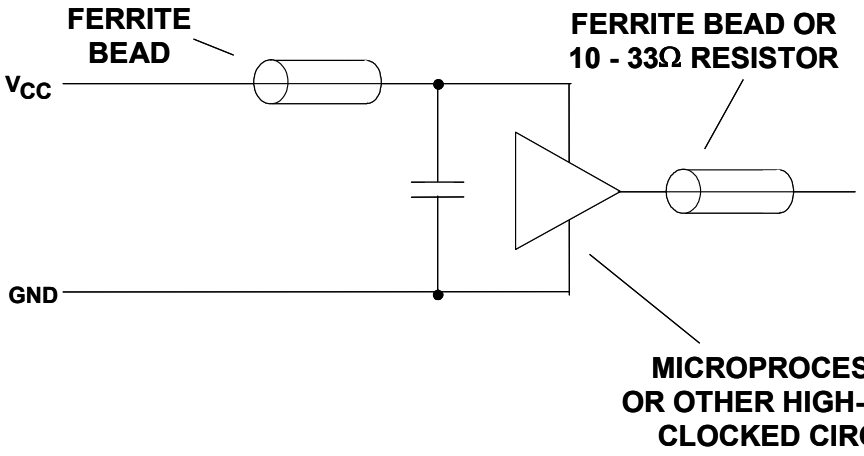


Figure 11.37: *Power Supply Filtering and Signal Line Snubbing Greatly Reduces EMI Emissions*

Many fast DACs and ADCs have digital inputs and outputs with rise and fall times in the nanosecond region. Because of their wide bandwidth, the sampling clock and the digital inputs and can respond to any form of high frequency noise, even glitches as narrow as 1 ns to 3 ns. These high speed data converters and amplifiers are easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. Adding a small ferrite bead just before the decoupling capacitor as shown in Figure 11.38 is very effective in filtering high frequency noise on the supply lines. For those circuits that require bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce the emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference

(I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution, and critical paths routed by hand.

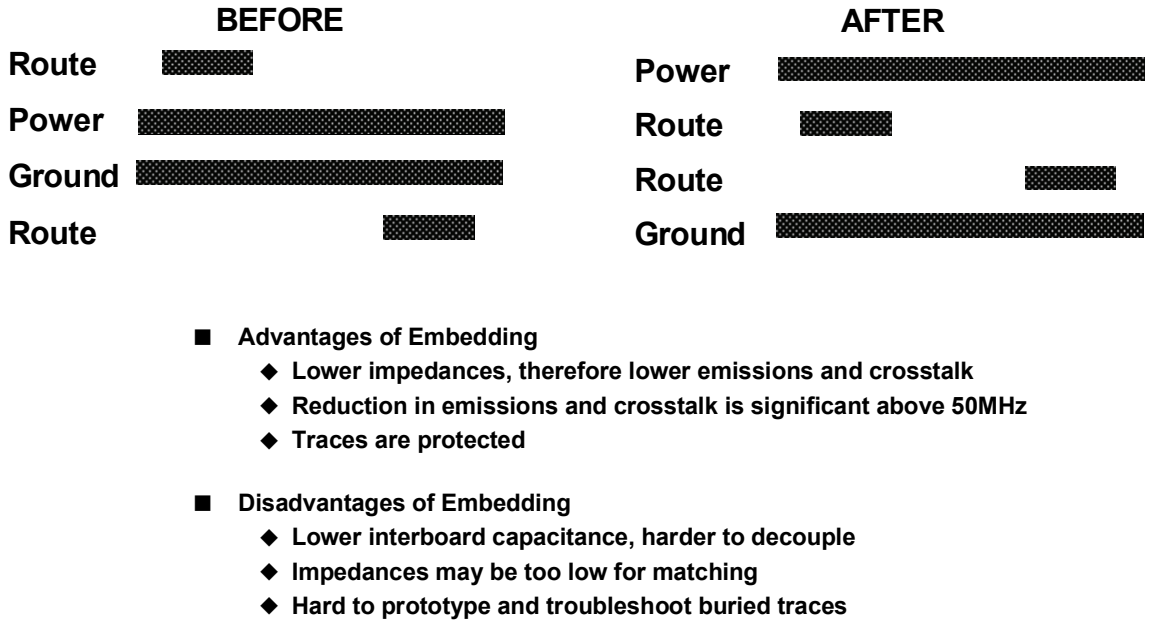


Figure 11.38: *"To Embed or Not To Embed" That Is the Question*

Properly designed multilayer printed circuit boards can reduce EMI emissions and increase immunity to RF fields by a factor of 10 or more compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc.

The preferred multilayer board arrangement is to embed the signal traces between the power and ground planes, as shown in Figure 11.39. These low impedance planes form very high frequency *stripline* transmission lines with the signal traces. The return current path for a high frequency signal on a trace is located directly above and below the trace on the ground/power planes. The high frequency signal is thus contained inside the PCB, thereby minimizing emissions. The embedded signal trace approach has an obvious disadvantage: debugging circuit traces that are hidden from plain view is difficult.

DIGITAL IC FAMILY	t_r, t_f (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50
HC	18	36	90

t_r = rise time of signal in ns
t_f = fall time of signal in ns

■ **For analog signals @ f_{max}, calculate $t_r = t_f = 0.35 / f_{max}$**

Figure 11.39: *Line Termination Should Be Used When the Length of the PCB Trace Exceeds 2 inches/ns*

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high speed logic with rise/fall time of 5 ns should be terminated in their characteristic impedance and if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 11.38 for a number of logic families

This same 2 inch/nanosecond rule should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime, t_r, can be calculated using the equation $t_r = 0.35/f_{max}$. The maximum PCB track length is then calculated by multiplying the rise time by 2 inch/nanosecond. For example, a maximum output

frequency of 100 MHz corresponds to a rise time of 3.5 ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

"ALL EMI PROBLEMS BEGIN AND END AT A CIRCUIT"

- **Identify critical, sensitive circuits**
- **Where appropriate, choose ICs no faster than needed**
- **Consider and implement sound PCB design**
- **Spend time on the initial layout (by hand, if necessary)**
- **Power supply decoupling (digital and analog circuits)**
- **High-speed digital and high-accuracy analog don't mix**
- **Beware of connectors for input / output circuits**
- **Test, evaluate, and correct early and often**

Figure 11.40: *Circuit Board Design and EMI*

Equation 9.4 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_o(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98d}{0.89w + t}\right] \qquad \text{Eq. 11-8}$$

where:

ε_r = dielectric constant of printed circuit board material;
d = thickness of the board between metal layers, in mils;
w = width of metal trace, in mils; and
t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq. 9.5:

$$t_{pd}(ns/ft) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 11-9}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 (ε_r = 4.7) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88 Ω and 1.7 ns/ft (7 "/ns), respectively. Transmission lines can be effectively terminated in several ways depending on the application..

Figure 11.41 is a summary of techniques that should be applied to printed circuit board layouts to minimize the effects of electromagnetic interference, both emissions and immunity.

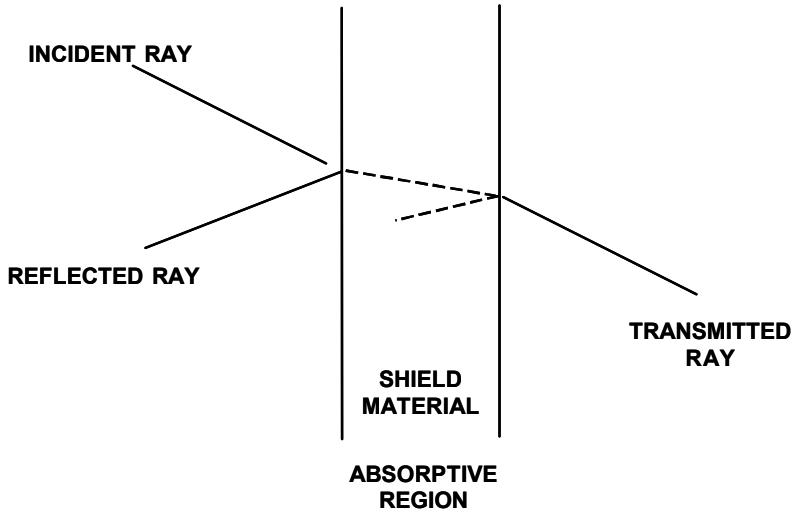


Figure 11.41 *Reflection and Absorption Are the Two Principal Shielding Mechanisms*

A Review of Shielding Concepts

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1, 3, and 4 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or π/2λ. If the distance between the circuit and the source of the interference is larger than this quantity, then the

circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350 MHz. The wavelength of a 350 MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350 MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by Z_O = 377 Ω. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377 Ω. If the source is low current and high voltage (for example, a rod antenna or a high speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377 Ω.

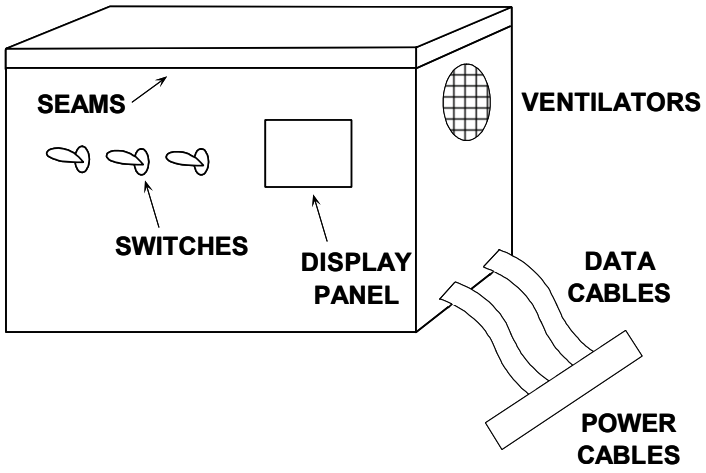


Figure 11.42: *Any Opening in an Enclosure Can Act as an EMI Waveguide by Compromising Shielding Effectiveness*

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. Both concepts are illustrated in Figure 11.42. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is

independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(\mathrm{dB}) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \qquad \text{Eq. 11.10}$$

where

σ_r = relative conductivity of the shielding material, in Siemens per meter;
μ_r = relative permeability of the shielding material, in Henries per meter;
f = frequency of the interference, and
r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(\mathrm{dB}) = 14.6 + 10\log_{10}\left[\frac{f r^2 \sigma_r}{\mu_r}\right] \qquad \text{Eq. 11.11}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(\mathrm{dB}) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \qquad \text{Eq. 11.12}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(\mathrm{dB}) = 3.34\ t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 11.13}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9 dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.
Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_S, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane

waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low frequency magnetic fields. In these applications, high permeability materials that exhibit low reluctance provide the best protection. These low reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Table 11.2.

Impedance and Skin Depths for Various Shielding Materials

Material	**Conductivity σ_r**	**Permeability μ_r**	**Shield Impedance $\lvert Z_S \rvert$**	**Skin depth δ (inch)**
Cu	1	1	$3.68E-7 \cdot \sqrt{f}$	$\frac{2.6}{\sqrt{f}}$
Al	1	0.61	$4.71E-7 \cdot \sqrt{f}$	$\frac{3.3}{\sqrt{f}}$
Steel	0.1	1000	$3.68E-5 \cdot \sqrt{f}$	$\frac{0.26}{\sqrt{f}}$
μ Metal	0.03	20,000	$3E-4 \cdot \sqrt{f}$	$\frac{0.11}{\sqrt{f}}$

Table 9.2

Where:

$$\sigma_o = 5.82 \times 10^7 \text{ S/m}$$
$$\mu_o = 4\pi \times 10^{-7} \text{ H/m}$$
$$\varepsilon_o = 8.85 \times 10^{-12} \text{ F/m}$$

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation (see Figure 11.43). Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

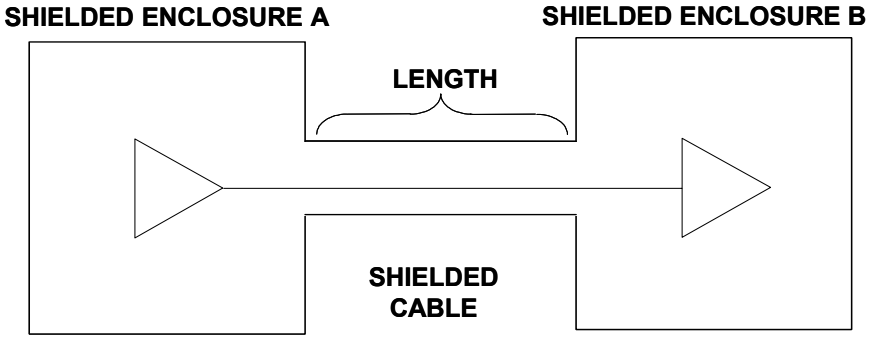
The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 9.10 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness}\,(\text{dB}) = 20\log_{10}\left(\frac{\lambda}{2\cdot L}\right) \qquad \text{Eq. 11.14}$$

where:

λ = wavelength of the interference and
L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0 dB shielding effectiveness). A rule of thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20 dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure are preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.



FULLY SHIELDED ENCLOSURES CONNECTED BY FULLY SHIELDED CABLE KEEP ALL INTERNAL CIRCUITS AND SIGNAL LINES INSIDE THE SHIELD.
- **TRANSITION REGION: 1/20 WAVELENGTH**

Figure 11.43 *Length of Shielded Cables Determines as "Electrically Long" or "Electronically Short" Applications*

General Points on Cables and Shields

Although covered in more detail later, the improper use of cables and their shields is a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 1, 2, 4, and 5. As illustrated in Figure 11.44 effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness.

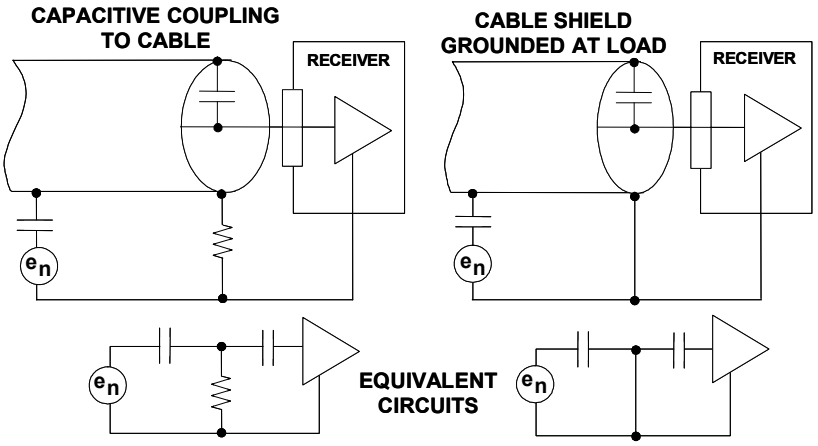


Figure 11.44: *Connect the Shield at One Point at the Load to Protect Against Low Frequency (50 Hz/60 Hz) Threats*

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50 Hz/60 Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable. To protect circuits against low frequency electric-field pickup, only one end of the shield should be returned to a low impedance point. A generalized example of this mechanism is illustrated in Figure 11.45.

- **Diagnose before you fix**
- **Ask yourself:**
  - **What are the symptoms?**
  - **What are the causes?**
  - **What are the constraints?**
  - **How will you know you have fixed it?**
- **Use available models for EMI to identify source - path - victim**
- **Start at low frequency and work up to high frequency**
- **EMI doctor's bag of tricks:**
  - **Aluminum foil**
  - **Conductive tape**
  - **Bulk ferrites**
  - **Power line filters**
  - **Signal filters**
  - **Resistors, capacitors, inductors, ferrites**
  - **Physical separation**

Figure 11.45: *EMI Troubleshooting Philosophy*

In this example, the shield is grounded at the receiver. An exception to this approach (which will be highlighted again later) is the case where line-level (>1 V rms) audio signals are transmitted over long distances using twisted pair, shielded cables. In these applications, the shield again offers protection against low-frequency interference, and an accepted approach is to ground the shield at the driver end (LF and HF ground) and ground it at the receiver with a capacitor (HF ground only).

In those applications where the length of the cable is *electrically long*, or protection against high frequency interference is required, then the preferred method is to connect the cable shield to low impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10 MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low frequency (<1 MHz), electric-field interference, grounding the shield at one end is acceptable. For high frequency interference (>1 MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure. Low-frequency ground loops can be eliminated by replacing one of the DC shield connections to ground with a low inductance 0.01 μF capacitor. This capacitor prevents low frequency ground loops and shunts high frequency interference to ground.

EMI Trouble Shooting Philosophy

System EMI problems often occur after the equipment has been designed and is operating in the field. More often than not, the original designer of the instrument has retired and is living in Tahiti, so the responsibility of repairing it belongs to someone else who may not be familiar with the product. Figure 11.46 summarizes the EMI problem solving techniques discussed in this section and should be useful in these situations.

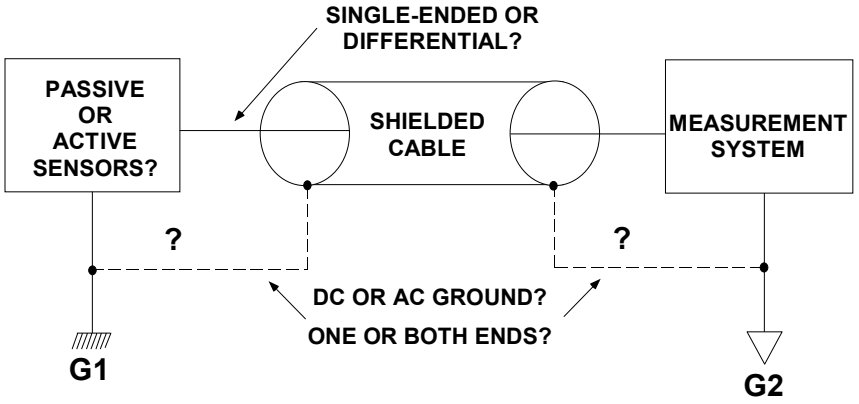


Figure 11.46: Precision Sensors and Cable Shielding

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