HIGH PERFORMANCE SAMPLE AND HOLD

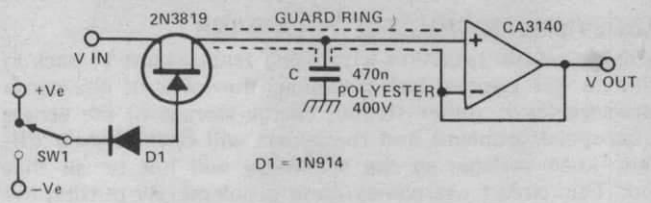
It is often necessary to have a circuit that will sample an analogue voltage and then remember it for a long time without any significant degradation of that voltage. This is known as a sample and hold circuit and one of its uses is to store the voltage from the keyboard connected to an electronic music synthesiser. The voltage is then used to control the pitch of a voltage controlled oscillator and so it is very important to have a high performance sample and hold. A drift of less than one semitone, (80 mV), in ten minutes is required. A sample and hold is simply an electronic switch, a storage capacitor and a high input impedance voltage follower. In the circuit shown, when switch SW1 is positive the FET is turned on, and has a resistance of about 400R. Thus the input voltage charges up the capacitor through the FET. When SW1 is negative, the FET is turned off, (pinched off), and can have a resistance of thousands of megohms. To get a long storage time the op-amp must have a very low input bias current. For the CA3140, this current is about 10 pico amps, i.e., 10^{-11} amps. Therefore the rate at which the capacitor will be discharged by this current can be worked out from the equation, $C(dv/dt) = i$
where dv/dt is the rate of change of voltage on the capacitor.

Therefore:

$$\frac{dv}{dt} = \frac{i}{C} = \frac{10^{-11}}{0.47 \times 10^{-6}} \quad 22\ uV/s$$

This is a very low drift rate, much better than we need. However, the actual drift rate will probably be in excess of this, due to surface leakage on the printed circuit board, leakage through the FET, and internal leakage in the capacitor. It is advisable to use a high voltage, non-polarised capacitor in this circuit to keep the leakage currents to a minimum. Also, to stop surface leakage a simple PCB trick can be used, that of making a guard ring around the sensitive components.

Normally any potential stored on the capacitor may leak to ground across the surface of the PCB, but if we make the surrounding surface a conducting track held at the same potential as that of the capacitor then the potential difference is virtually always zero, and hence the surface leakage is greatly reduced.



PRINTED CIRCUIT BOARD LAYOUT