Sample-and-hold amplifier holds the difference of two inputs

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

You can fulfill a requirement for sampling the difference of two signals in two classic ways. You can subtract the two input signals with an instrumentation amplifier whose output connects to an input of a classic sample-and-hold amplifier. Despite the positive feature of needing no external resistors for a gain-of-one differencing instrumentation amplifier, this approach suffers from high relative output distortion when the inputs are of the same polarity and close in magnitude. In such a case, the difference of two input signals is close to 0V, and the amplifier is therefore more vulnerable to residual dynamic imperfections of the sample-and-hold amp. The other approach is to separately sample the two input voltages in two sample-and-hold amps and subtract the outputs of these amps in an instrumentation amp. Here, the relative error of output signal with similar input waveforms is lower than in the first approach.

If you like all-in-one solutions, you can use the circuit configuration in **Figure 1**. This circuit simultaneously tracks both input voltages, V_{INA} and V_{INB}, at an active-high level of the internal logic-control signal, which enables the A_1, B_1, and A_2 voltage followers. V_{INA} thus appears on capacitor C_2, which is ground-referenced. Capacitor C_1, which is temporarily grounded at its upper node, Pin 9 of IC_1, tracks the V_{INB} voltage. After a settling interval when all of the internal logic-control signals go inactive low, the Q_{SB} logic-control signal goes high. The voltage of $V_{C2}(TS)=V_{INA}(TS)$ shifts the potential at the lower node of capacitor C_1 because of the enabled B_3 follower. Upon the sample command, Q_S is high, and the upper node of C_1 is grounded within the tracking interval. Storage capacitor C_3 therefore charges through the B_2 follower to a voltage of $V_{C2}(TS)-V_{C1}(TS)=V_{INA}(TS)-V_{INB}(TS)$. The A_3 follower serves as an impedance converter.

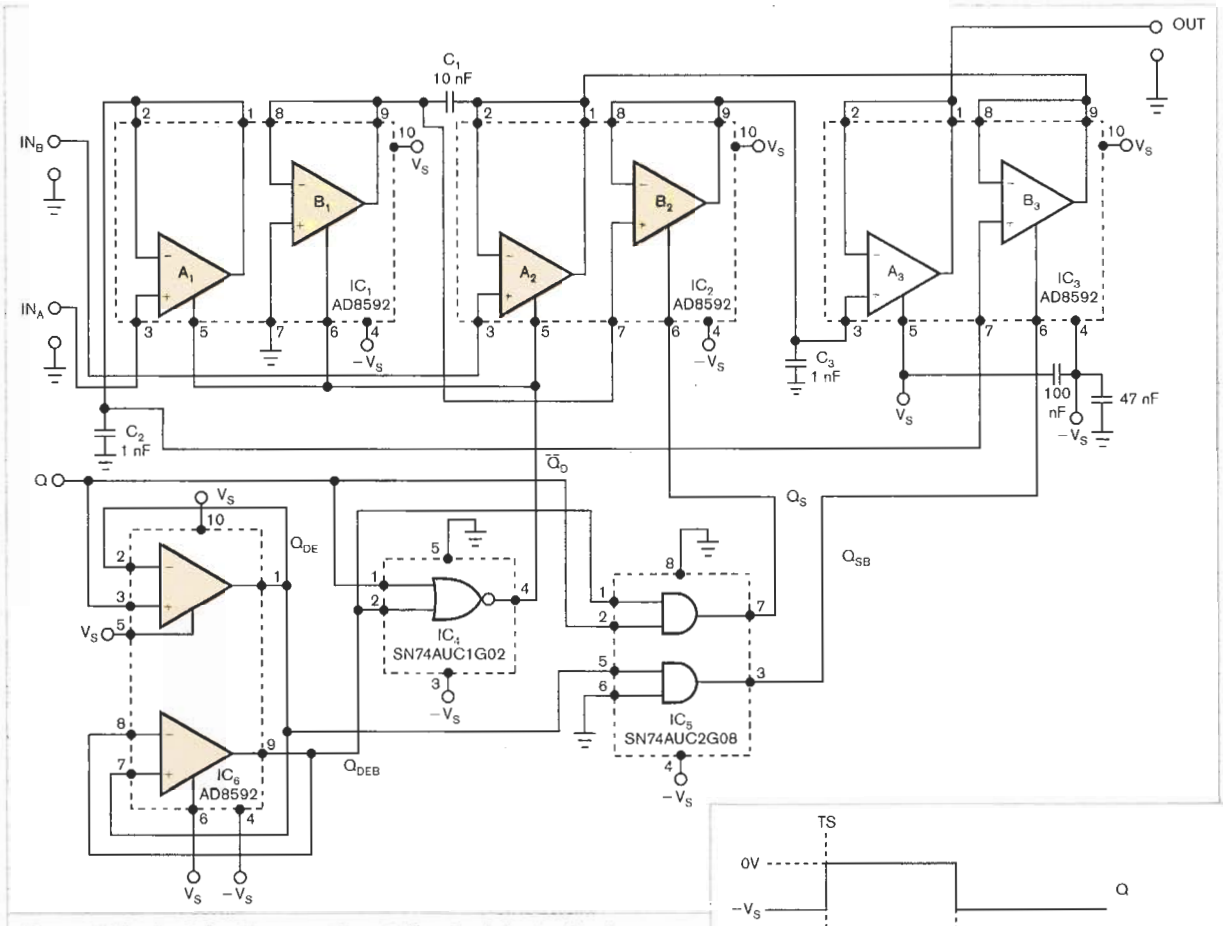
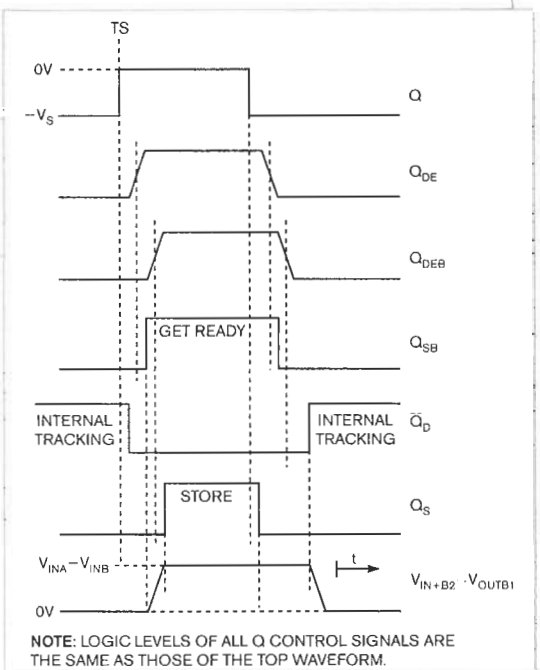


Figure 1 The basis for the operation of this circuit is the simultaneous tracking of the V_{INA} and V_{INB} input voltages on capacitors C_1 and C_2 and a stacking of these capacitors within the sample interval on capacitor C_3.



NOTE: LOGIC LEVELS OF ALL Q CONTROL SIGNALS ARE THE SAME AS THOSE OF THE TOP WAVEFORM.

Figure 2 The bottom waveform shows that, at the upper node of capacitor C_1, 0V appears within the tracking interval, and it rises to the value of a difference between both input voltages within the get-ready interval when Q_{SB} is high. The difference of input voltages of $V_{INA}(TS)-V_{INB}(TS)$ resides within the store interval when Q_S is high.

The voltage gains of both the A and the B channels are slightly lower than ideal. This slight gain decrease has approximately the same value for both channels: $\delta_{GAINA}=\delta_{GAINB}\sim(C_{OUTB1}/C_1)$. The equality of gain decrements on both channels stems from the fact that the upper node of the storage capacitor, C_1, connects at the instant that Q_{SB} goes high to the output capacitor, C_{OUTB1}, of the disabled follower, B_1. Follower B_1 always discharges to 0V within the tracking interval without regard to the voltages at the A and B inputs. For Analog Devices' (www.analog.com) AD8592 op amps, the output capacitance, C_{OUT}, in the disabled state is approximately 26.2 pF.

Note, however, that if V_{INA} and V_{INB} are of opposite polarity and of equal magnitude, almost reaching the value of $V_S/2$, the output voltage approaches either the positive- or the negative-supply rail. In this case, the relative output error is about twice that given in the previous **equation**. The op amps' capacitance rises as the output voltage approaches any of the supply rails, reaching the value of 55 pF. This increasing output capacitance arises from one of the complementary power transistors in the AD8592's output stage as its drain-to-source voltage approaches 0V at the output voltage close to the positive-supply rail. The increasing drain-to-source capacitance with decreasing drain-to-source voltage is an inherent

property of MOSFET transistors. The same situation holds true for the bottom power transistor of the AD8592's output stage, when the output voltage approaches the negative-supply rail.

The turn-on time of the AD8592 is much longer than the turn-off time. Although the device's data sheet does not directly specify these times, you can see from the internal structure of the IC that the on/off control enters almost all of the IC's stages (**Reference 1**). Thus, turn-off is fast because the turn-off of the output stage occurs without regard for the states of the preceding stages. Within one period of operation of the circuit in **Figure 1**, a sequence of two turn-ons (T_{ON}) plus four intentionally added delays (T_{DE}) determines the shortest sampling period: $T_{MIN} \sim T_{ONBJ} + 4T_{DE} + T_{ONA1B1A2}$. Here, $T_{ONA1B1A2}$ is the largest from among the values of turn-on times of followers A_1, B_1, and A_2, which depend on the actual values of V_{INA} and V_{INB}. The maximum sampling frequency is then $1/2(T_{ON}+2T_{DE})$.

If you assume that the maximum turn-on time can reach the value of the overvoltage-recovery time of approximately 3 µsec and that the delay time is approximately 0.35 µsec, then it follows that the maximum sampling frequency is approximately 135 kHz. The duty-factor of the external logic-control signal, Q, for sampling frequencies near the value of the maximum sampling frequency should be about 0.5 **(Figure 2)**.EDN

REFERENCE

"AD8592-Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier," Analog Devices Inc, 1999, www.analog.com/zh/prod/0,,759_786_AD8592,00.html.