Inexpensive peak detector requires few components

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Requiring no rectifier diodes, the positive peak-detector circuits in **figures 1** and **2** exploit the open-drain output of a Texas Instruments TLC372 fast comparator, IC_1. Both versions of the detector are simple and inexpensive and provide a buffered, low-impedance output at V_{OUT}. In addition, the TLC372's high typical input impedance of $10^{12}\Omega$ eliminates any need for an input buffer stage. As **Figure 1** shows, the detector's output voltage at the output of op amp IC_{2A} applies a feedback signal for the comparator and acts as a reference level for comparison with the input signal's amplitude. Upon first application of input signal V_{IN}, the voltage on the hold capacitor, C_1, is 0V, and V_{OUT} is also 0V.

When the input signal goes more positive than the output voltage, the comparator's internal output MOSFET turns on and sinks current through R_1. Provided that R_2 is relatively large, charging current flows into C_1 from IC_{2A}'s output. Over several cycles of the input signal, the charge on C_1 builds up, and V_{OUT} rises to the point at which it slightly exceeds the peak level of V_{IN}. For as long as V_{OUT} is slightly greater than V_{IN}, IC_1's output MOSFET remains off, and C_1 receives no additional packets of charge.

As a consequence, the charge stored on C_1 starts to dissipate as the capacitor discharges through R_2 and through the bias-current path into IC_{2A}'s inverting input. V_{OUT} gradually falls until it is just below the peak level of V_{IN}. The next positive peak of V_{IN} trips comparator IC_1, which pulls current through R_1, "topping up" the charge on C_1. This process produces a dc level at V_{OUT} that closely approximates the positive peak level of the input waveform. The values of R_1, R_2, and C_1 determine the ripple voltage present on V_{OUT}.

IC_{2A}'s inverting input is held at virtual ground potential, so whenever IC_1's output MOSFET turns on, the voltage across R_1 approximately equals the negative-supply-rail voltage, $-V_S$. Therefore, using a small value of R_1 injects a relatively large pulse of current into C_1, thus allowing the circuit to respond quickly to a sudden increase in input-signal amplitude—that is, a "fast-attack" response. However, if the value of R_1 is too small, the positive-going ripple on V_{OUT} becomes excessive and can lead to bursts of oscillation around peak values of V_{IN}.

For a given value of R_2, the value of C_1 determines the circuit's "delay time."

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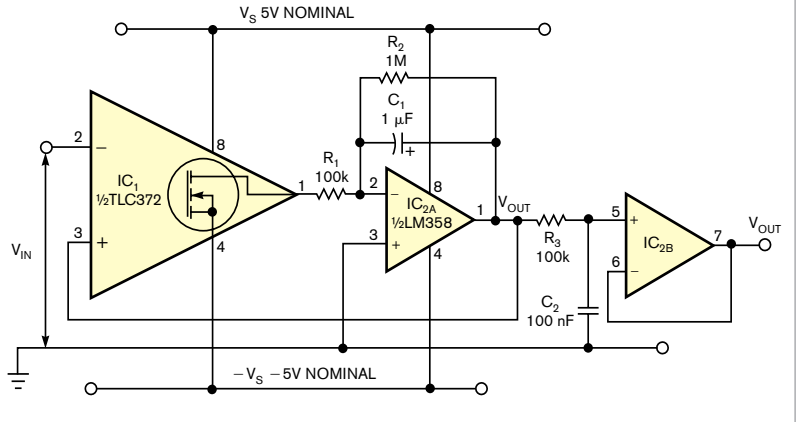

Figure 1 The dual-power-supply-voltage version of this positive peak detector requires only two active devices: a comparator and a dual operational amplifier.

A relatively large value of capacitance minimizes the negative-going ripple on V_{OUT}, which can be useful when dealing with low frequencies, low-duty-cycle pulse trains, or both. However, making C_1 too large renders the detector sluggish when responding to a sudden decrease in input-signal amplitude. Note that C_1 also affects the attack time; for example, doubling the capacitance doubles the time the circuit takes to acquire the peak level of V_{IN}.

Because the comparator's feedback path includes op amp IC_{2A}, offsets and errors that IC_{2A} presents have no effect on the circuit's accuracy. At low to moderate frequencies, only the comparator's input offset errors contribute to the detector's overall accuracy. At high frequencies, the comparator's response time becomes a significant factor, leading to a reduction in V_{OUT} that worsens as the frequency increases. Despite these limitations, the circuit performs well over several decades of frequency from approximately 50 Hz to 500 kHz. **Figure 2** and **Table 1** show the test circuit's sine-wave-frequency response by plotting the error in V_{OUT} for three peak levels of V_{IN}.

The oscilloscope photo shows the circuit's response to a 500-mV peak sine wave at 400 kHz, in which the output voltage, at 488 mV, lies just below the positive peaks (**Figure 3**). In addition to exhibiting good sine-wave response, the test circuit produces good results with rectangular signals of duty cycles as low as 5%. Note that the virtual ground at IC_{2A}'s inverting input restricts V_{OUT} to positive voltages only. Therefore, the circuit can respond only to true positive peaks—that is, peaks that go above 0V. If the input signal goes entirely below 0V, V_{OUT} simply levels off at 0V.

Although not essential to the circuit's operation, the lowpass filter and buffer formed by R_3, C_2, and IC_{2B} can minimize any switching noise that appears on V_{OUT}. However, offset errors inherent to op amp IC_{2B} affect the filter's output voltage.

Figure 4 shows a single-supply version of the circuit, in which R_A and R_B set a reference voltage, V_{REF}, at IC_{2A}'s

TABLE 1 SINE-WAVE-FREQUENCY RESPONSE

Frequency (Hz)	Error V_{IN}=2.5V peak (%)	Error V_{IN}=250 mV peak (%)	Error V_{IN}=25 mV peak (%)
200	−0.4	0.8	10
2000	−0.4	1.2	10
20,000	0	0.4	6.4
200,000	0	−2.4	−7.6
400,000	0	−4	−22
500,000	−2.4	−4.8	−28.4
600,000	−12	−6	−34

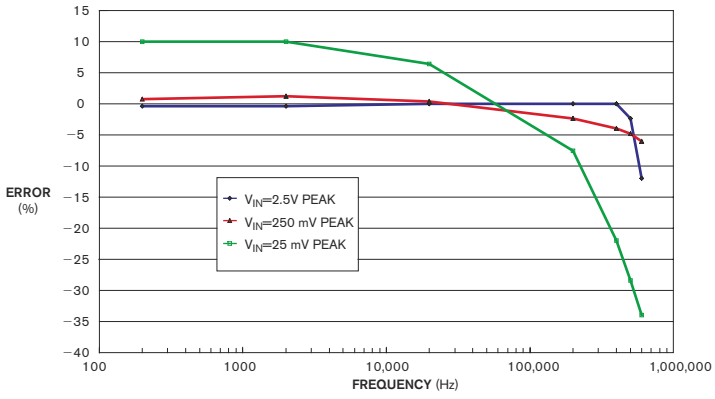

Figure 2 Plotting the difference between peak signal levels and output voltage for three peak levels illustrates the detector's frequency response.

Figure 3 An oscilloscope photo displays input versus output voltages for a 400-kHz, 500-mV sine wave.

noninverting input, such that IC_{2A} maintains a virtual potential equal to V_{REF} at the inverting input. Thus, when V_{IN} goes more positive than V_{OUT}, the comparator's output MOSFET turns on, pulling the output down to 0V and impressing a potential equal to V_{REF} across R_1. This action, in turn, injects a current pulse equal to V_{REF}/R_1 into C_1. In most respects, the circuit behaves in the same manner as the circuit in **Figure 1**. As in the dual-rail version, V_{OUT} cannot go below the potential at the op amp's noninverting input. Therefore, even though V_{IN} need not center on a potential equal to V_{REF}, V_{IN}'s positive peaks must exceed V_{REF} for the circuit to work properly.

To select a value for V_{REF}, examine the input and output common-mode-voltage ranges of both op amp IC_{2A} and comparator IC_1 and the maximum peak-to-peak swing of the input signal. For example, setting the positive power-supply voltage, V_S, to 10V and setting $R_A=R_B$ sets $V_{REF}=5V$. The detector accommodates an input signal that swings from 0V to approximately 8V and thus detects positive peak voltages of 5 to 8V. Remember to select R_1 according to the value chosen for V_{REF}. EDN

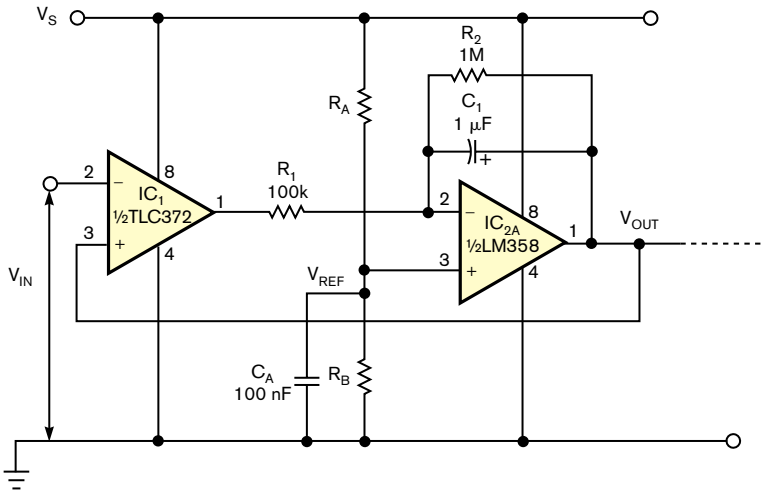

Figure 4 For operation from a single power supply, this version of the peak detector sets a reference voltage via resistors R_A and R_B.