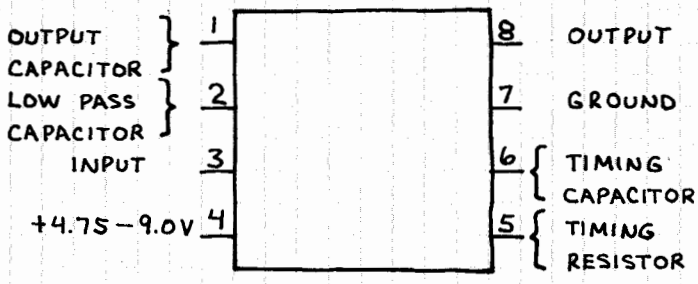
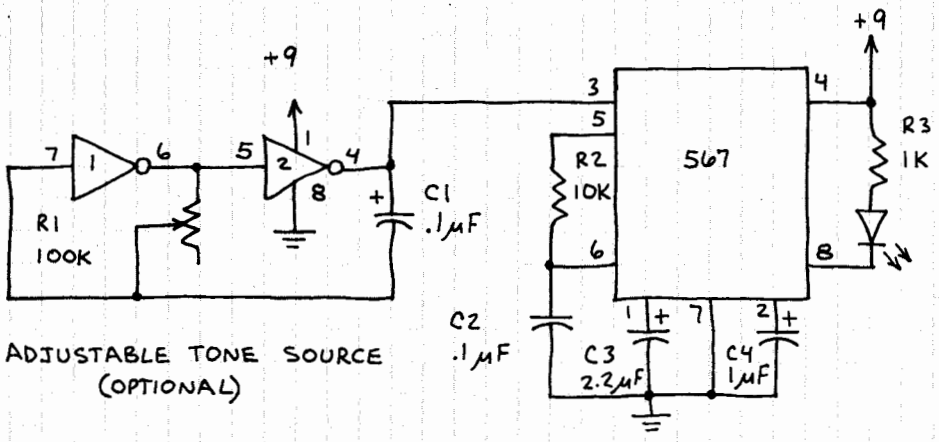
TONE DECODER
567

CONTAINS A PHASE-LOCKED LOOP. PIN 8 GOES LOW WHEN THE INPUT FREQUENCY MATCHES THE CHIP'S CENTER FREQUENCY (f_o). THE LATTER FREQUENCY IS SET BY THE TIMING RESISTOR AND CAPACITOR (R AND C) AND IS $(1.1) \div (RC)$. R SHOULD BE BETWEEN 2K-20K. THE 567 CAN BE ADJUSTED TO DETECT ANY INPUT BETWEEN 0.01 Hz TO 500KHz. NOTE: 1 SECOND OR MORE MAY BE REQUIRED FOR THE 567 TO LOCK ON TO LOW FREQUENCY INPUTS! SEE THIS CHIP'S SPECIFICATIONS FOR MORE INFORMATION.



THE VALUE IN MICROFARADS OF THE LOW PASS CAPACITOR SHOULD BE n / f_o WHERE n RANGES BETWEEN 1300 (FOR UP TO 14% f_o DETECTION BANDWIDTH) TO 62,000 (UP TO 2% f_o DETECTION BANDWIDTH). THE OUTPUT CAPACITOR SHOULD HAVE ABOUT TWICE THE CAPACITANCE OF THE LOW PASS FILTER CAPACITOR.

BASIC TONE DETECTOR CIRCUIT



ADJUSTABLE TONE SOURCE (OPTIONAL)

THIS CIRCUIT IS HANDY FOR LEARNING TONE DECODER BASICS. THE 567 PORTION CAN BE USED IN MANY DIFFERENT APPLICATIONS (SEE BELOW). THE PREDICTED f_o IS 1.1 KHz. THE TEST CIRCUIT f_o WAS 1.3KHz.