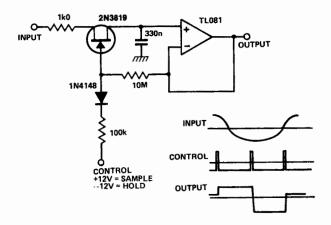
49

FET Sample And Hold

Control = +12 V; sample Control = -12 V; hold

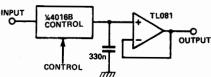


Use a printed circuit guard ring (connected to the output voltage) around the hold capacitor

50

4016 Sample And Hold

Control = $+V_{CC}$; sample Control = $-V_{CC}$; hold $-V_{CC}$ < signal voltage < $+V_{CC}$ $+V_{CC}$ - $(-V_{CC}) \le 15 \text{ V}$



Use a printed circuit guard ring (connected to the output voltage) around the hold capacitor