Pulse height modulator

This circuit reduces the spike feedthrough in series f.e.t. gates by always limiting the gate voltage swing to between the source voltage and the pinch-off voltage. Referring to Fig. 1, if the input voltage (V_i) is

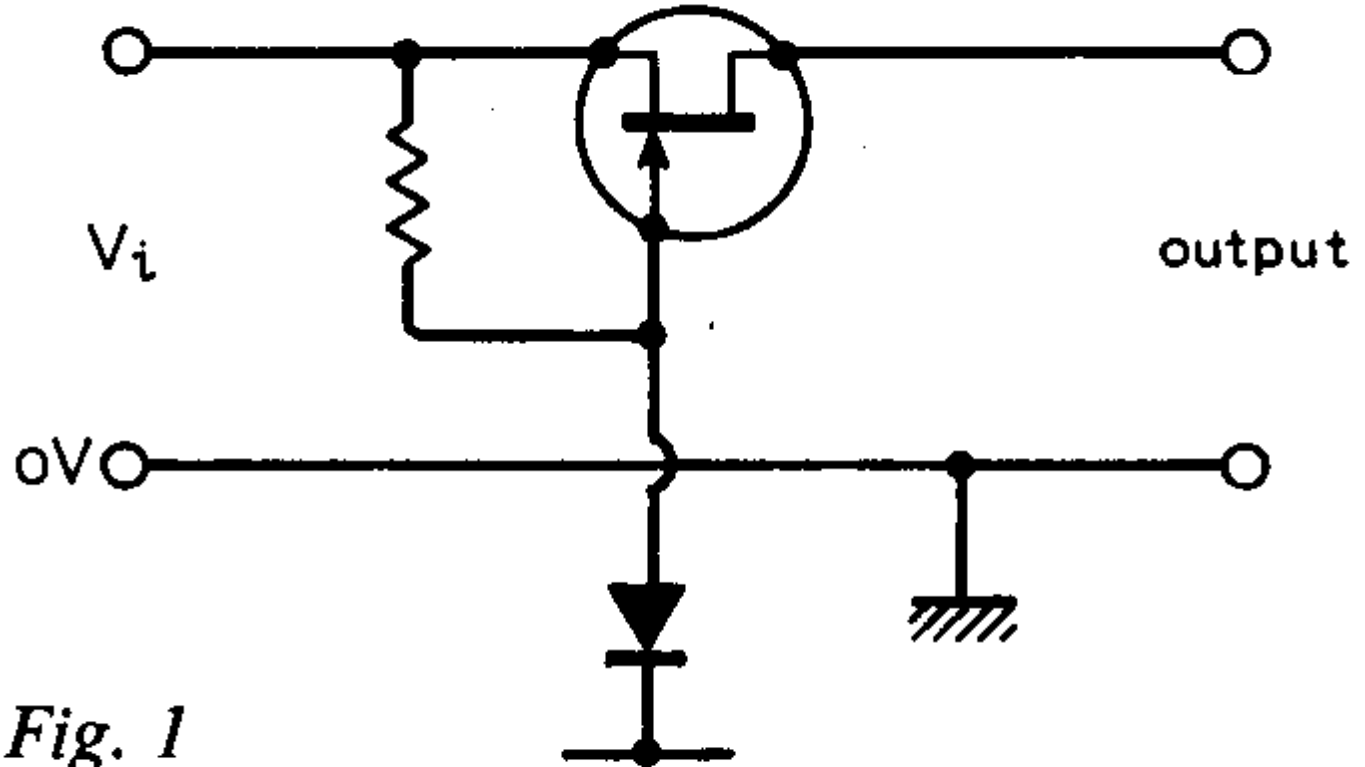
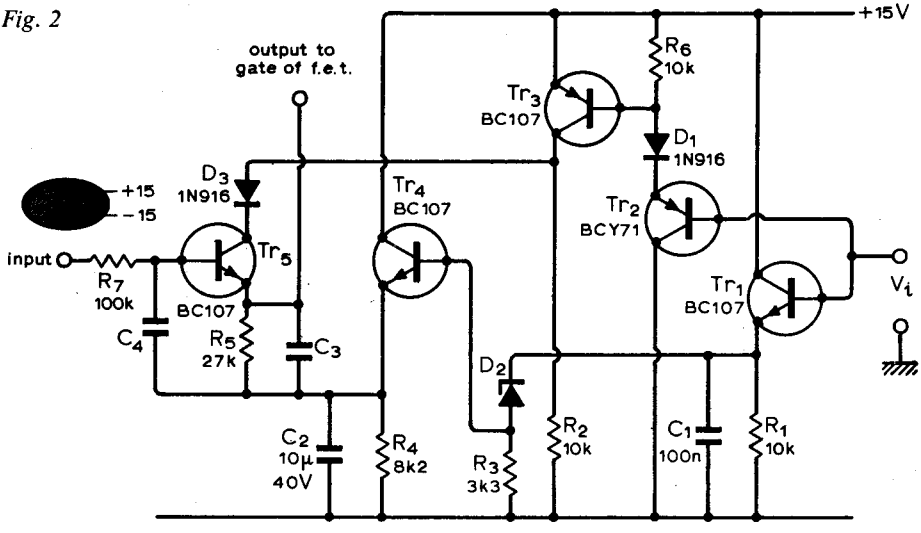


Fig. 1

varied between 0 and 13V, say from an op-amp, then the f.e.t. gate would have to be swung from $+13$V to $-V_p$ volts (V_p is pinch-off voltage). Fig. 2 shows one version of a circuit used to limit the voltage swing on the f.e.t. gate to approximately $V_i - V_p$. Input voltage is monitored by the emitter followers Tr_1 and Tr_2 and Tr_1 emitter is maintained at $V_i - V_{be} \approx V_i - 0.7$V. Zener diode D_2 is matched as nearly as possible to the *measured* V_p of the particular f.e.t. in use. If $V_p < 1$V a forward-biased diode (e.g. 1N916) may be used. The emitter of Tr_4 is therefore established at $V_i - V_p - 1.4$V. Tr_2, Tr_3 and D_1 establish the upper limit of the voltage swing to $\approx V_i$. The switching waveform, a ± 15V squarewave with

Fig. 2


+15V
output to gate of f.e.t.
R6 10k
Tr3 BC107
D1 1N916
D3 1N916
+15
−15
Tr4 BC107
Tr2 BCY71
input
R7 100k
Tr5 BC107
Tr1 BC107
Vi
C4
R5 27k
C3
D2
C2 10μ 40V
R4 8k2
R3 3k3
R2 10k
C1 100n
R1 10k

fast rise and fall times, drives the base of Tr_5. Clearly from Fig. 2 the output waveform cannot go below $V_i - V_p - 1.4V$ or above V_i.

Capacitors C_3 and C_4 are optional. Capacitor C_4 increases the rise time of the output signal and C_3 increases the fall time. Very slow turn off times can be obtained by suitable adjustment of C_3 thereby giving further spike reduction. Resistor R_7 should be kept high because for low values of V_p and high values of V_i the emitter-base junction of Tr_5 will become reverse biased. Alternatively a diode can be placed between the emitter and R_5.

The modulator was tried with a number of different types of f.e.ts and always reduced the spike amplitude when compared to the spike produced by a full $\pm 15V$ swing on the gate. By using a slow fall time the spike amplitude for this edge could easily be reduced by an order of magnitude. The circuit may need slight modification to suit individual requirements but works well with a slowly changing analogue signal and with switching rise/fall time of the order of 1μs.

M. D. G. Dabbs,
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