Digital-analog interface acts as counter/modulator

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Some control system applications require counting a variable number of events at various times and providing an activating signal accordingly. This need can be fulfilled by a divide-by-N counter, where N is dynamically variable. Adding the pulse-position modulation scheme borrowed from power and communication systems forms a simple digital circuit with a digital-analog interface that functions as a dynamically variable divide-by-N counter and pulse-position modulator. Additionally, cascading these units results in a dynamic divide-by-N, divide-by-M, and complex ppm circuit.

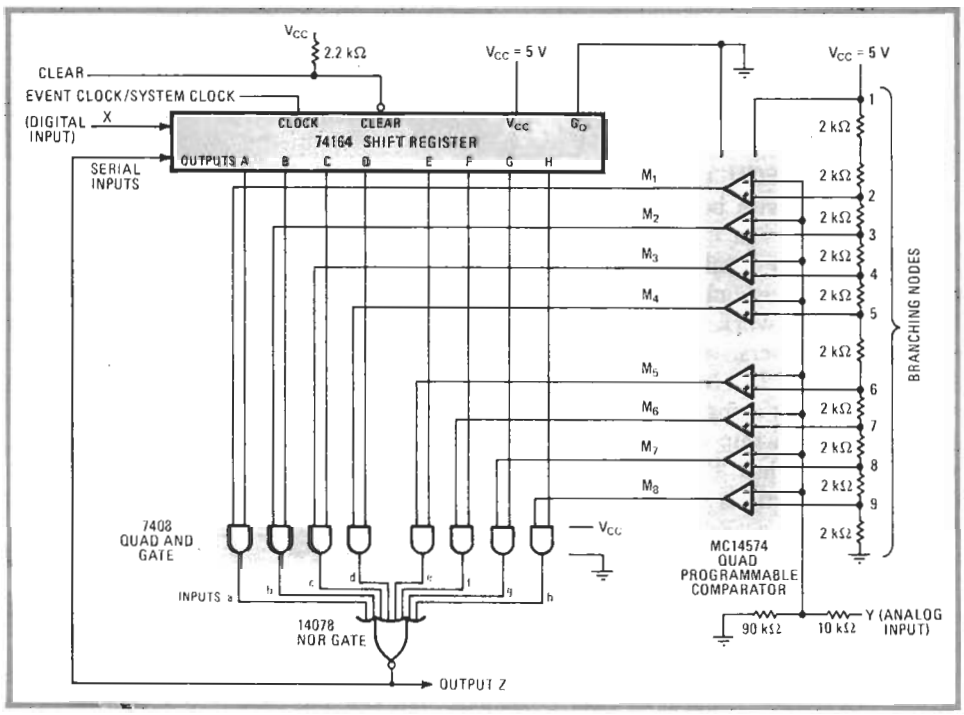
In Fig. 1, a simple shift-register-based counter is constructed as a variable divide-by-N counter. Assuming digital input X is at a high level (logic 1) and analog input Y is connected to the ground node, the digital control word M1 . . . M8 is 1 1 1 1 1 1 1 1. The Z output of the 14078 NOR gate is high whenever inputs a through h are all zero. This Z output is clocked into the shift register, in the form of a walking 1 through the states A through H. It takes eight clocks to shift out the walking 1 and present an all-zero condition at the A through H outputs of the shift register, which is transmitted to the a through h inputs of the NOR gate.

If the control word M1 . . . M8 is made 1 1 1 1 1 1 1 0, the shift register must shift 1 bit through 7 states (A through G) to present an all-zero condition at the a through h inputs of the NOR gate. This provides the divide-by-8 action. Following the same sequence of operations, the system behavior is summarized:

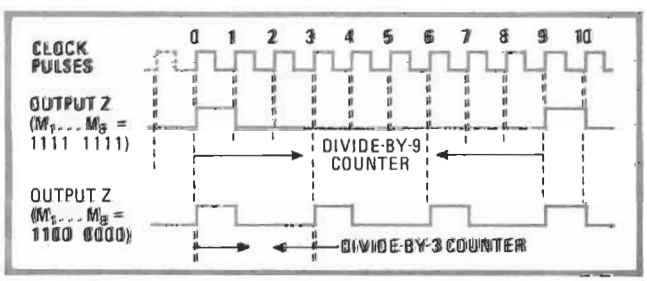
Divide-by-9	if control word $M_1 \ldots M_8$	= 1 1 1 1 1 1 1 1
Divide-by-8	"	= 1 1 1 1 1 1 1 0
Divide-by-7	"	= 1 1 1 1 1 1 0 0
Divide-by-6	"	= 1 1 1 1 1 0 0 0
Divide-by-5	"	= 1 1 1 1 0 0 0 0
Divide-by-4	"	= 1 1 1 0 0 0 0 0
Divide-by-3	"	= 1 1 0 0 0 0 0 0
Divide-by-2	"	= 1 0 0 0 0 0 0 0

The desired control word is obtained by connecting analog node Y to the appropriate node. For divide by 9, the analog node is connected to branching node 9, and so forth. Figure 2 shows the waveforms.

If the Y analog input is connected to an analog input voltage with an amplitude between 0 and 4 volts, the system will behave as a continuously variable divide-by-N counter (N can range from 2 to 9). The Z output of the system will manifest pulse-position modulation properties with maximum separation between Z pulses for the lowest voltages (divide-by-9 action) and minimum separation for the highest voltages (divide-by-2 action). Several of these systems can be cascaded to operate as a variable modulo counter with a divisor range from 4 to 81. Some of the prime numbers, such as 17, 23, 29, and so on, may not be realizable when using the specified shift registers, but larger registers can overcome this limitation. □



1. Variable counter. Using a voltage-divider network as the input to the MC14574 programmable comparator determines the analog levels necessary to create the control word that determines the divide-by-N action. The threshold at each node differs by .5 V.



2. Divide-by-N waveforms. With the shift register initially cleared and a control word consisting of all 1s, the Z output of the NOR gate, in this case a logical 1, is fed to the shift register upon presence of a clock pulse. The Z output goes high every ninth clock pulse, providing divide-by-9 action.