Special Sample and Hold Techniques

National Semiconductor
Application Note 294

Although standard devices (e.g., the LF398) fill most sample and hold requirements, situations often arise which call for special capabilities. Extended hold times, rapid acquisition and reduced hold step are areas which require special circuit techniques to achieve good results. The most common requirement is for extended hold time. The circuit of *Figure 1* addresses this issue.

EXTENDED HOLD TIME SAMPLE AND HOLD

In this circuit, extended hole time is achieved by "stacking" two sample and hold circuits in a chain. In addition, rapid acquisition time is retained by use of a feed-forward path. When a sample command is applied to the circuit (trace A, *Figure 2*), A1 acquires the input very rapidly because its 0.002 μF hold capacitor can charge very quickly. The sample command is also used to trigger the DM74C221 one-shot (trace B, *Figure 2*), which turns on the FET switch, S1. In this fashion, A1's output is fed immediately to the A3 output buffer. During the time the one-shot is high, A2 acquires the value of A1's output. When the one-shot drops low, S1 opens, disconnecting A1's output from A3's input. At this point A2's output is allowed to bias A3's input and the circuit output does not change from A1's initial sampled value. Trace C details what happens when S1 opens. A small glitch, due to charge transfer through the FET, appears but the steady state output value does not change. This circuit will acquire a 10V step in 10 μs to 0.01% with a droop rate of just 30 μV/second.

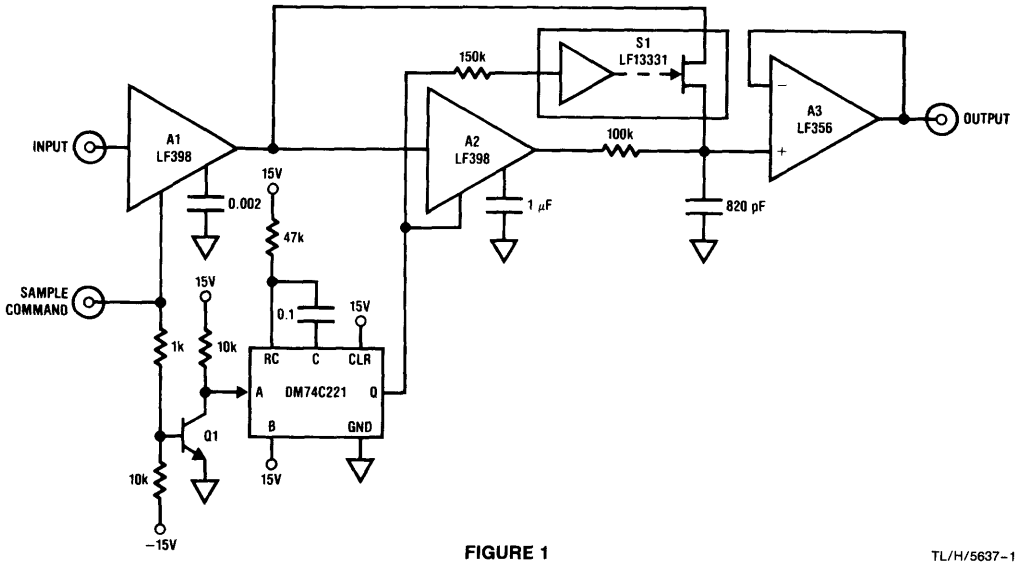

FIGURE 1

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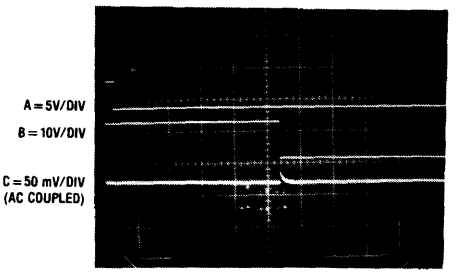

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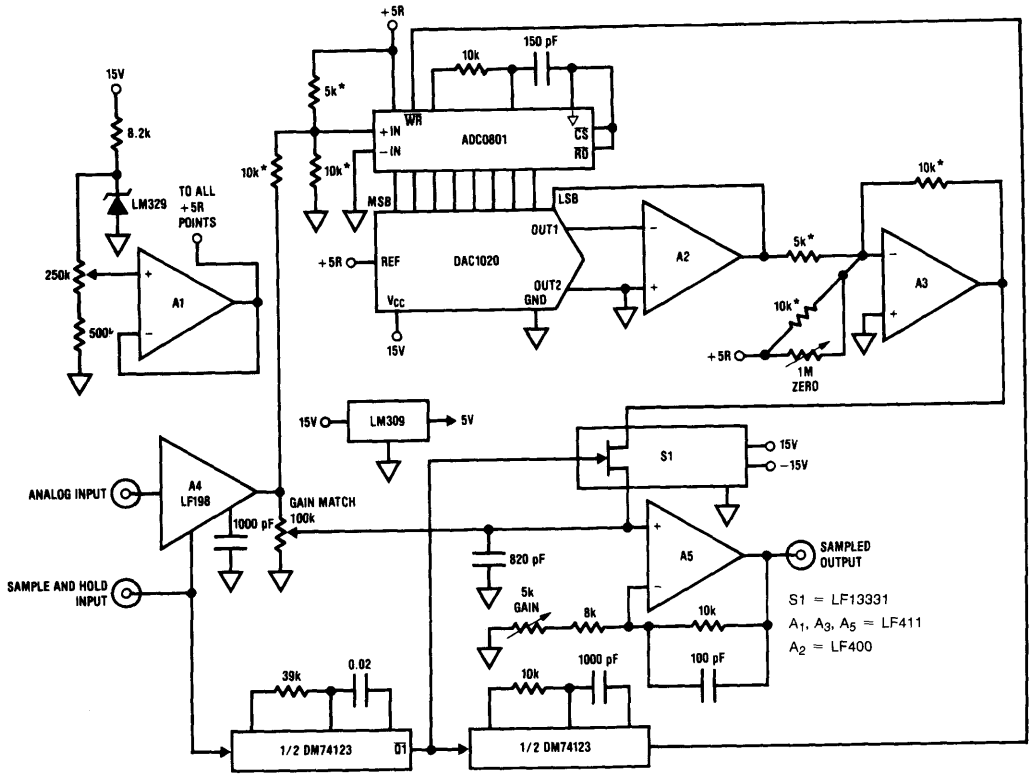
FIGURE 2



*Ratio match 0.1%

FIGURE 3

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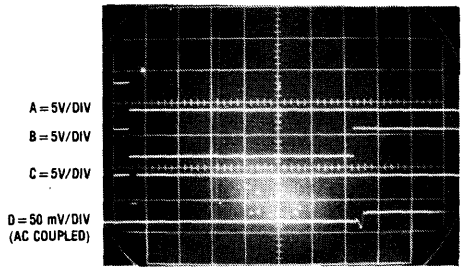
INFINITE HOLD SAMPLE AND HOLD

Figure 3 details a circuit which extends the hold time to infinity with an acquisition time of 10 μs. Once a signal has been acquired, this circuit will hold its output with no droop for as long as is desired. If this arrangement, A4's divided down output is fed directly to the circuit output via A5 as soon as a sample command (trace A, *Figure 4)* is applied. The sample command is also used to trigger the DM74123 one-shots. The first one-shot (trace B, *Figure 4)* is used to bias the FET switch OFF during the time it is low. The second one-shot (trace C, *Figure 4)* delivers a pulse to the ADC0801 A/D converter which then performs an A/D conversion on A4's output. The DAC1020, in combination with A2 and A3, converts the A/D output back to a voltage. The A/D/A process requires about 100 μs. When the one-shot (trace B) times out, its output goes high, closing the FET switch. This action effectively connects A3's output to A5 while disconnecting A4's output. In this manner, the circuit output will remain at the DC level that was originally determined by A4's sampling action. Because the sampled value is stored digitally, no droop error can occur. The precision resistors noted in the circuit provide offsetting capability for the unipolar A/D output so that a −10V to +10V input range can be accommodated. To calibrate this circuit, apply 10V to the input and drive the sample command input with a pulse generator. Adjust the gain match potentiometer so that minimum "hop" occurs at the circuit output when S1 closes. Next, ground the input and adjust the zero potentiometer for 0V output. Finally, apply 10V to the input and adjust the gain trim for a precise 10V circuit output. Once adjusted, this circuit will hold a sampled input to within the 8-bit quantization level of the A/D converter over a full range of +10V to −10V. Trace D, *Figure 4* shows the circuit output in great detail. The small glitch is due to parasitic capacitance in the FET switch, while the level shift is caused by quantization in the A/D. An A/D with higher resolution could be used to minimize this effect.



A, B, C HORIZONTAL = 20 μs/DIV
D HORIZONTAL = 2 μs/DIV

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FIGURE 4

HIGH SPEED SAMPLE AND HOLD

Another requirement encountered in sample and hold work is high speed. Although conventional sample and hold circuits can be built for very fast acquisition times, they are difficult and expensive. If the input waveform is repetitive, the circuit of *Figure 5* can be employed. In this circuit a very fast comparator and a digital latch are placed in front of a differential integrator. Feedback is used to close a loop around all these elements. Each time an input pulse is applied, the DM7475 latch is opened for 100 ns. If the summing junction error at the LM361 is positive, A1 will pull current out of the junction. If the error is negative, the inverse will occur. After some number of input pulses, A1's output will settle at a DC level which is equivalent to the value of the level sampled during the 100 ns window. Note that the delay time of one-shot A is variable, allowing the sample pulse from one-shot B to be placed at any desired point on the input waveform. *Figure 6a* shows the circuit waveforms. Trace A is the circuit input. After the variable delay provided by one-shot A, one-shot B generates the sample pulse (trace B). In this case the delay has been adjusted so that sampling occurs at the mid-point of the input waveform, although any point may be sampled by adjusting the delay appropriately.

Figure 6b shows the circuit at work sampling a 1 MHz sine wave input. The optional comparator (C2) shown in dashed lines is used to convert the sine wave input into a TTL compatible signal for the DM74123 one-shot. Trace A is the sine wave input while trace B represents the output of C2. Trace C is the delay generated by one-shot A and trace D is the sample width window out of one-shot B. Note that this pulse can be positioned at any point on the high speed sine wave with the resultant voltage level appearing at A1's output.

REDUCED HOLD STEP SAMPLE AND HOLD

Another area where special techniques may offer improvement is minimization of hold step. When a standard sample and hold switches from sample to hold, a large amplitude high speed spike may occur. This is called hold step and is usually due to capacitive feedthrough in the FET switches

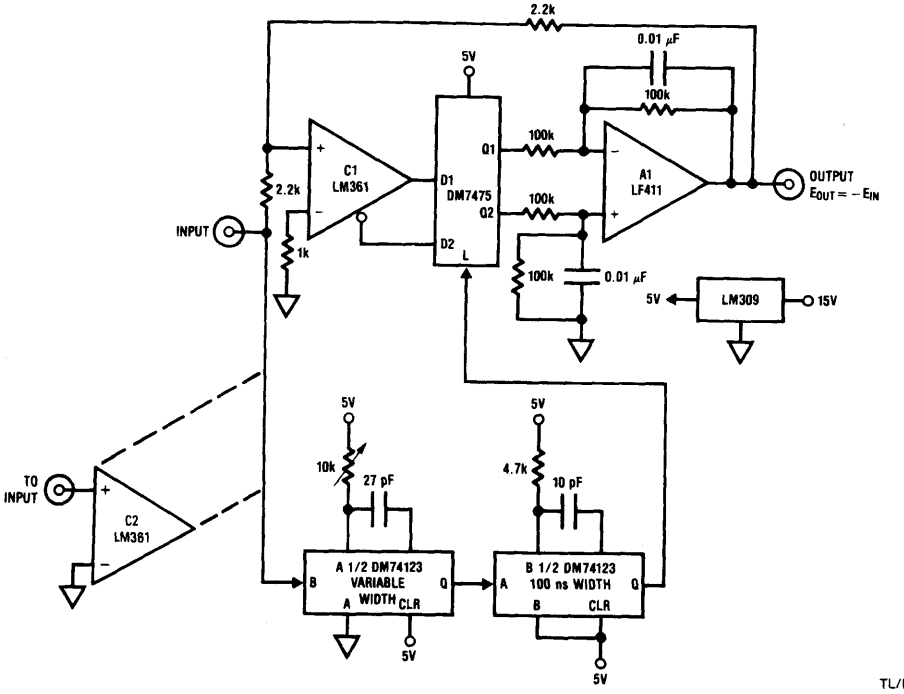

FIGURE 5

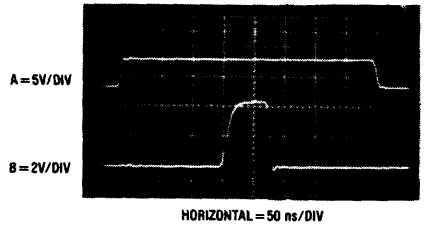

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FIGURE 6a

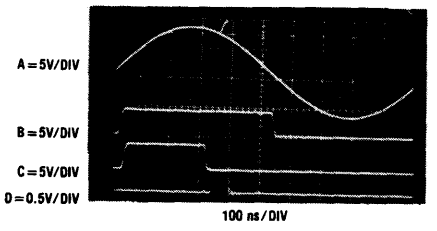

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FIGURE 6b

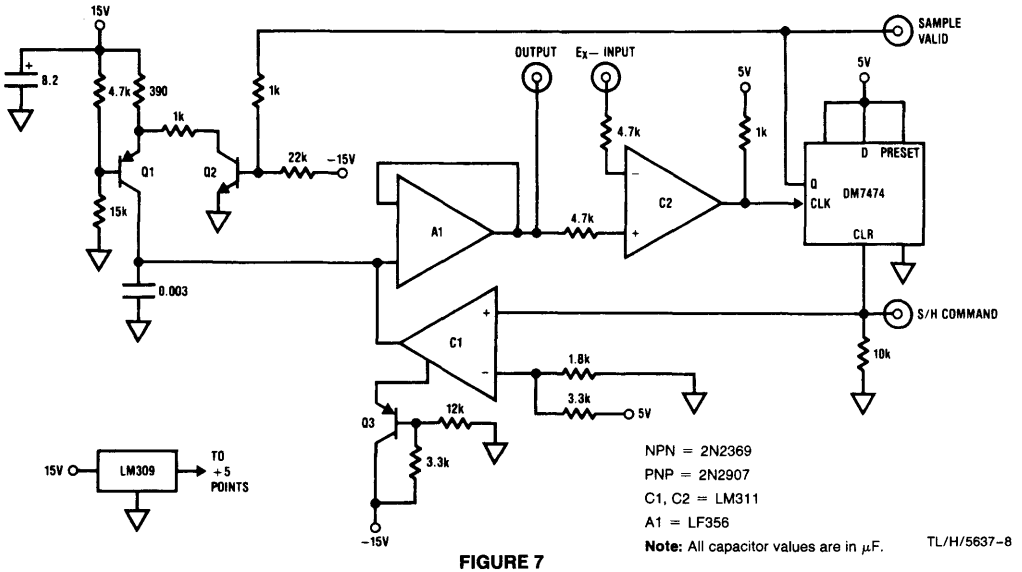

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FIGURE 7

used in the circuit. The circuit of *Figure 7* greatly reduces hold step by using an unusual approach to the sample and hold function. In this circuit sampling is started when the sample and hold command input goes low (trace A,*Figure 8*). This action also sets the DM7474 flip-flop low (trace B, *Figure 8*). At the same time, C1's output clamps at Q3's emitter potential of −12V (trace C, *Figure 8*). When the sample pulse returns high, C1's output floats high and the 0.003 μF capacitor is linearly charged by current source Q1. This ramp is followed by A1, which feeds C2. When the ramp potential equals the circuit's input voltage, C2's output (trace D, *Figure 8*) goes high, setting the flip-flop high. This turns on Q2, very quickly cutting off the Q1 current source. This causes the ramp to stop and sit at the same potential at the circuit's input. The hold step generated when the circuit goes into hold mode (e.g., when the flip-flop output goes high) is quite small. Trace E, a greatly enlarged version of trace C, details this. Note the hold step is less than 10 mV high and only 30 ns in duration. Acquisition time for this circuit is directly dependent on the input value, at a rate of 5 μs/V.

REFERENCE

One IC Makes Precision Analog Sampler, S. Dendinger; EDN May 20, 1977.

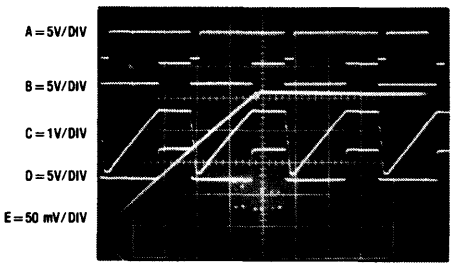

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FIGURE 8