Prevent emitter-follower oscillation

by understanding its causes. You can minimize problems by adding an inexpensive resistor or ferrite bead.

You can use graphical analysis and minor circuit changes to prevent oscillation in emitter-follower output stages. For most applications a simplified analysis can pinpoint the causes of oscillation and help you avoid loss of system performance and possible damage to transistors and other components.[1,2,3]

Oscillations occur at 50 kHz and higher

When emitter-follower circuits break into oscillation, they usually do so at some frequency between 50 kHz and 500 MHz. The frequency, of course, depends on the transistor's f_T and its source and load impedances (Fig. 1).

Because the influential transistor characteristics—notably f_T and C_{ob}—vary with voltage and current, the emitter-follower oscillations sometimes occur in only part of the signal range—coming and going as the signal waveform rises and falls.

Let's first analyze the emitter-follower stability, using a one-pole model for the transistor's current gain, $\beta(f)$. This model will show how interactions among the source and load impedances and the transistor can result in oscillation because of the transistor's negative input resistance at some frequencies.

In analyzing the oscillation problem, different authors use different mathematical techniques to model the circuit. Basically any analysis proceeds as follows:

- At high frequencies, an R-C emitter load is transformed by $\beta(f)$ to appear at the transistor base as a negative resistance in series with a capacitor. (Both the resistance and the capacitance are frequency-dependent.)
- When an inductive source impedance is placed at the base, it results in oscillation if the external resistance of the base circuit is small enough. Then the total resistance in the loop is zero or negative at the frequency at which $X_L = X_C$.

Michael Chessman, Project Engineer, and **Nathan Sokal**, Director of Engineering, Design Automation Inc., 809 Massachusetts Ave., Lexington, MA 02173.

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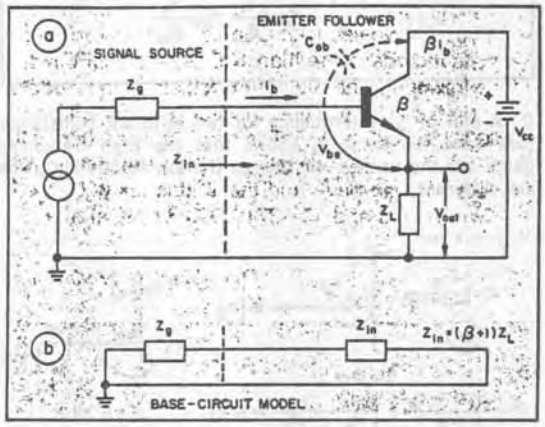


1. The emitter-follower transistor circuit (a) provides large current gain, β, but can be unstable at certain frequencies. A simplified base model (b) allows easy determination of the conditions for stability.

The usual solution to this instability is to overwhelm the apparent negative resistance with an external positive resistor at the base, so that the sum of the resistances is positive. For example, if we assume Z_L to be a parallel R-C load, we must do three things to prevent oscillation:

(1.) Determine the resulting emitter-follower input impedance, Z_{in}, and show that the real part, $Re[Z_{in}]$, can be negative.

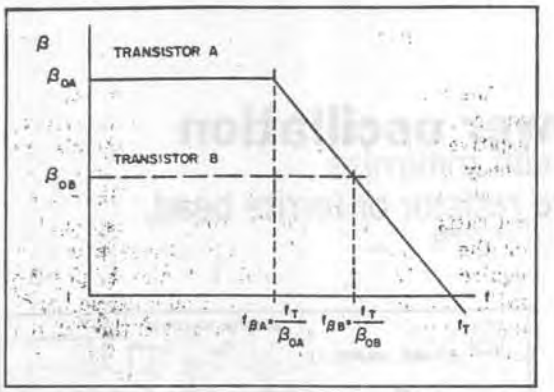
(2.) Examine the subsequent circuit conditions required for oscillation.

(3.) Use remedial techniques to prevent oscillation.

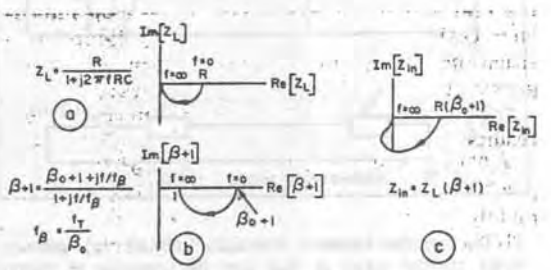
The $r_{b'e}$ and $C_{b'e}$ shown in most common transistor models can be included as part of the expression for the dependence of β (small-signal, common-emitter current gain) on frequency. However, C_{ob} is assumed to be a circuit element external to the basic transistor. If we assume that $Z_L >> r_e$ (where $r_e = 0.026/I_C$ at 25 C) and that (for the ac components) $V_{be} << V_{out}$ the expression for input impedance results:

$$Z_{in} \approx (\beta + 1)\, Z_L.$$

The stability of the emitter follower is determined by the behavior of Z_{in} with frequency. And



2. A plot of β vs frequency for two different transistors that have the same f_T shows that the high frequency gains are the same even though the low frequency gains are different.



3. The emitter-follower impedance loci plots for the load-impedance locus (a), the (β + 1) locus (b) and the input-impedance locus (c) are all basically in the fourth quadrant.

Z_{in}, in turn, depends directly on β, which varies with frequency.

Look at β as a function of frequency

If we assume that β is the current gain of the basic transistor (without C_{ob}) and that the emitter depletion-layer capacitance (C_{ib}) is absorbed into the emitter diffusion capacitance, we can approximate $\beta(f)$ with a one-pole model:

$$\beta(f) = \frac{\beta_o}{1 + j\beta_o f/f_T},$$

where β_o is the low-frequency asymptotic value of $\beta(f)$.

The transistor's beta-cutoff frequency, f_T/β_o, (also called beta corner frequency) is useful for low-frequency analysis. However, f_T is more useful than f_β in characterizing the high-frequency properties of a transistor. There are two reasons:

First, since it is the transistor design that determines f_T, all devices of a given design have similar f_T values. β_o is much more variable among transistors of a given design, leading to correspondingly large variations in f_β.

Second, most high-frequency applications of transistors are at frequencies well above f_β. Hence most transistors, regardless of their individual f_β, operate at frequencies in the $\beta \propto 1/f$ region, where all transistors of the same f_T have essentially the same β and the same variation of β with frequency (Fig. 2).

The Z_L impedance locus for the assumed R-C load (Fig. 3a) is in the fourth quadrant for $f > 0$. The locus for (β + 1) is shown in Fig. 3b. Note that the phase of (β + 1) is always lagging for $f > 0$ and is also in the fourth quadrant. In the product

$$Z_{in} = Z_L(\beta + 1),$$

the individual phase angles add, and this rotates the resulting locus clockwise. Thus, at some frequencies Z_{in} can be in the left half plane, where the real part (resistance) is negative, as in Fig. 3c.

Although this analysis is for Z_L as a parallel R-C load, the reasoning holds for any complex Z_L whose impedance (both resistive and capacitive) is in the fourth quadrant for some frequencies. The details of the loci of (β + 1) and of Z_L do not affect the qualitative conclusions because the product, $Z_L(\beta + 1)$, can be in the third quadrant regardless of deviations from this particular Z_L.

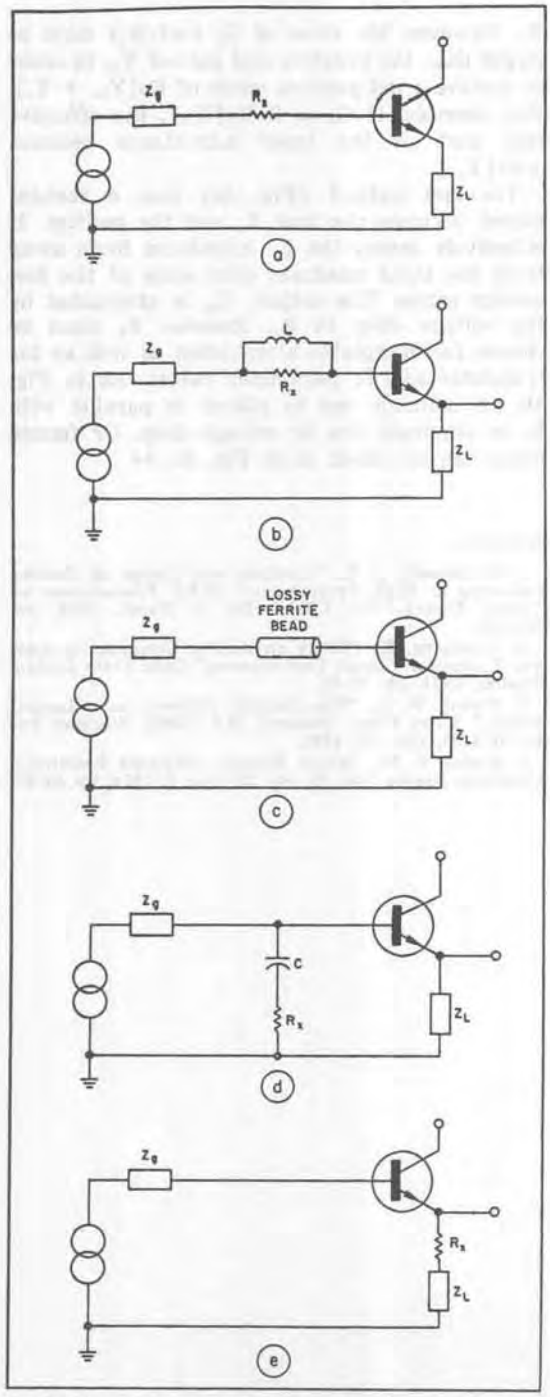
The interaction of such a Z_L with (β + 1) produces a Z_{in} whose impedance locus is in the third quadrant over some of the frequency range. Then Z_{in} has both a negative real part (negative resistance) and a negative imaginary part (capacitive reactance). These impedance polarities are important when the associated conditions that can lead to oscillation are determined.

It is tempting to model the resulting input resistance and capacitance with fixed-value components. However, both the resistance and the capacitance are functions of frequency: you can model them at only a single frequency as a fixed-value negative resistor and a fixed-value capacitor.

Check the conditions for oscillation

The total loop impedance around the equivalent base circuit in Fig. 1b is $Z = (Z_g + Z_{in})$. Because a capacitive input reactance accompanies the negative input resistance, an inductive source reactance can supply the additional element needed to make a resonant circuit. If the source resistance is equal to or less than the magnitude of the negative input resistance at the resonant frequency of the L-C resonant circuit, the circuit will oscillate as a negative-resistance oscillator.

Expressed mathematically, oscillation occurs at frequency f_o if the total loop impedance at f_o has zero net reactance ($\mathrm{Im}[Z_g + Z_{in}] = 0$) and a zero or negative net resistance ($\mathrm{Re}[Z_g + Z_{in}] \leq 0$):



4. **Five basic circuit modifications** can be used to prevent emitter-follower oscillation. The techniques are as simple as adding a resistor to the base circuit (a), adding a parallel LR circuit to the base (b), placing a ferrite bead on the base lead (c), putting a series RC circuit from the base to ground (d), or adding a series resistor to the emitter circuit (e).

$$\mathrm{Re}[Z_g] + \mathrm{Re}[Z_{in}] \leq 0 \quad (1)$$

$$\mathrm{Im}[Z_g] + \mathrm{Im}[Z_{in}] = 0 \quad (2)$$

Thus for some frequencies, an emitter follower can have a Z_{in} with both real and imaginary negative parts. Oscillations can occur in this frequency range if the negative input impedance cancels the positive external-source impedance and satisfies Eqs. 1 and 2. Since Z_{in} is negative for the frequencies of interest, these equations require $\mathrm{Re}[Z_g] \leq |\ \mathrm{Re}[Z_{in}]\ |$ and a positive $\mathrm{Im}[Z_g]$ to sustain oscillation. Under these conditions the imaginary parts cancel, and the net real part is still negative or zero.

A Z_g whose locus is in the upper half-plane can satisfy these requirements for oscillation. A simple example of this is a series L-R combination, whose locus lies in the first quadrant, with positive real and imaginary parts.

Purely sinusoidal oscillation occurs only when the real and imaginary parts of the loop impedance both exactly equal zero, a very improbable situation. In practice, the oscillation amplitude grows until one of the following occurs:

- A (sometimes strongly) nonlinear signal results.
- The circuit saturates and stops oscillation.
- The circuit enters a region where approximately linear operation is possible.

If Re[Z] is slightly greater than zero, ringing (damped oscillation) occurs in response to input excitation.

In most linear circuits slight nonlinearities that are always present limit the signal growth and sometimes produce good approximations to true sinusoids. In emitter-follower oscillations the transistor nonlinearities typically limit the oscillation amplitude to about 1 V across the load.

Typical circuit element values

The emitter-follower's negative input resistance is typically in the range of 0 to $-500\ \Omega$. A typical value for the parasitic capacitance of the load wiring is $C \leq 10$ pF. Carbon resistors have an equivalent parallel capacitance ranging from about 0.08 pF for 1/8-W resistors to about 1.6 pF for 2-W resistors. And the nonparasitic load capacitance is often much larger than 10 pF.

Parasitic base-circuit inductance, L_b, is typically between 10 and 100 nH, and wiring contributes from 8 to 40 nH/in., depending on the size and separation of the conductors, one of which may be a ground plane. Reference 4 is helpful in estimating wiring inductance.

A circuit whose net loop resistance is positive cannot sustain oscillation. Therefore, one way to prevent or eliminate oscillation is to ensure that the net loop resistance is positive at the frequencies of interest.

The simplest and most obvious method of preventing oscillation is shown in Fig. 4a; just add enough external base-circuit resistance, R_x, to overwhelm the negative real part of Z_{in}. Appropriate values of R_x range from tens of hundreds of ohms. With this method, the dc bias point may be affected because of the dc voltage drop in R_x.

In Fig. 4b an inductor is connected in parallel with the external base resistor. The dc bias is unaffected because the inductor has low dc resistance, but at high frequencies the resistor appears in series with the base to prevent oscillation.

The circuit of Fig. 4c uses the L-R method of Fig. 4b, but you construct the L by threading a lossy ferrite bead onto a circuit lead—in this case, the transistor base lead. At frequencies higher than a few hundred MHz, this method is preferable, because it is easier and because a ferrite bead of the proper material can appear as a pure resistance out to a much higher frequency than can a circuit constructed of a separate L and R. Such lossy ferrite beads are available from Ferroxcube, Stackpole, Indiana General, and others.

Another method (Fig. 4d) uses a shunt resistor, R_x, coupled to the base circuit by the series capacitor, C. Coupling occurs only at the high frequencies at which oscillation may be a problem. Dc bias is not affected by the presence of R_x. However, the value of G_x $(=1/R_x)$ must be larger than the negative real part of Y_{in} in order to achieve a net positive value of $Re[Y_{in} + Y_x]$. For example, if $G_x = 2\ Re[Y_{in}]$, the effective real part of the input admittance becomes $+Re[Y_{in}]$.

The last method (Fig. 4e) uses a resistor placed between the load Z_L and the emitter. It effectively moves the Z_L impedance locus away from the third quadrant over some of the frequency range. The output, V_o, is attenuated by the voltage drop in R_x. Resistor R_x must be chosen for acceptable attenuation as well as for transistor and Z_L parameter values. As in Fig. 4b, an inductor can be placed in parallel with R_x to eliminate the dc voltage drop. Or ferrite beads can be added, as in Fig. 4c. ■■

References

1. Kozikowski, J. L., "Analysis and Design of Emitter Followers at High Frequencies," *IEEE Transactions on Circuit Theory*, Vol. CT-11, No. 1, March, 1964, pp. 129-136.

2. Tammaru, E., "Using an Analog Computer to Analyze Transistor Circuit Performance," *Solid State Design*, October, 1964, pp. 28-36.

3. Nichol, W. S., "The Emitter Follower as a Logical Switch," Mitre Corp., Bedford, MA 01803, Working Paper W-4403, Oct. 19, 1961.

4. Rostek, P. M., "Avoid Wiring-Inductance Problems," *Electronic Design*, Vol. 22, No. 25, Dec. 6, 1974, pp. 62-65.