Application Note

APPLICATION IDEAS FOR MULTIPLYING DAC's

Digitally Controlled Gain is Useful in Filter Circuits

by John Newell

The uses of CMOS multiplying DAC's are becoming more widely known and more fully developed as more types with a wider range of resolutions and accuracies have become available and –most important – as prices have rapidly decreased*.

This family of digital-to-analog converters, sired by the AD7520 in 1973, has an important feature not possessed by many DAC types: they can work with positive or negative reference voltage (for example, an ac analog input) without switching or circuit modification, and with negligible ac feedthrough at frequencies well beyond the audio range. The analog channel has wide dynamic range.

In such applications, it is useful to think of these devices as digitally programmed analog gain (or attenuation) channels, –digitally controlled potentiometers – rather than as d/a converters with wide-range reference capability.

ATTENUATION AND GAIN

The simplest application for a multiplying DAC is in the digitally controlled attenuator shown in Figure 1. Here, if the value of the digital word, relative to full scale (fractional binary), is D, ($D = A_1 2^{-1} + A_2 2^{-2} + \ldots A_n 2^{-n}$, $A_i = 1$ or 0) then the output is

$$V_O = -D\,V_{IN} \qquad (1)$$

The number of values of gain (including zero) is 2^n, for a binary converter, 4096 in the case of the case of the AD7541.* The 8-bit AD7523* has 256 steps of gain, and the "L" version permits each to be set to within 0.1% of full scale.

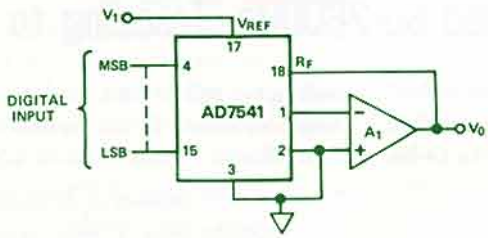

Figure 1. Digitally controlled attenuation.

In this circuit, the analog input is applied to the "reference" terminal of the ladder network, and the feedback from the output of the op amp is applied to the on-chip "feedback" application resistor, which tracks the ladder resistance.

The ladder transduces the input voltage to a current proportional to the digital word, and the feedback resistor develops the output voltage. Distortion and bandwidth are to a great extent determined by the choice of amplifier; such circuitry is well-suited to audio applications.[1]

*See pages 9 and 14.

[1] See "Audio Application Ideas for CMOS DAC's" by Walter Jung, ANALOG DIALOGUE 10-1, 1976, pp. 16-17

Gains greater than unity can be achieved by connecting resistance in series with R_F, but a wide-range trim is necessary and the tracking advantage is likely to be lost.

Another way of obtaining gains greater than unity is to apply the DAC for the inverse function. If the signal is connected to R_F, and the output is fed back to the analog (reference) input of the DAC, then the nominal transfer function is:

$$V_O = -\frac{V_{IN}}{D} \qquad D > 0 \qquad (2)$$

Gains from 1 to 4096 are attainable with the AD7541. However, like divider-connected analog multipliers, the multiplying DAC circuit has errors that are inversely proportional to the magnitude of D–including gain, offset, and response time. When the DAC is used with a high open-loop-gain, low-drift op amp, such as the AD517, a linear programmable-gain amplifier, capable of handling reasonably low-level, low-frequency data, can be built.

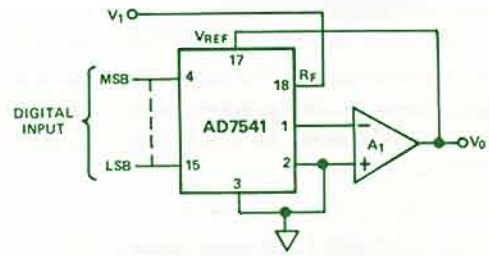

Figure 2. Digitally controlled gain.

In a data-acquisition system, simple logic (hard-wired or processor) can be used to determine the number of leading zeros in a trial conversion at unity gain and to set the gain of the amplifier for the maximum resolution of which the circuit is capable for a second conversion. Naturally, the resolution exceeds the calibration accuracy, but this may be quite in order for wide-range signals (Figure 3).

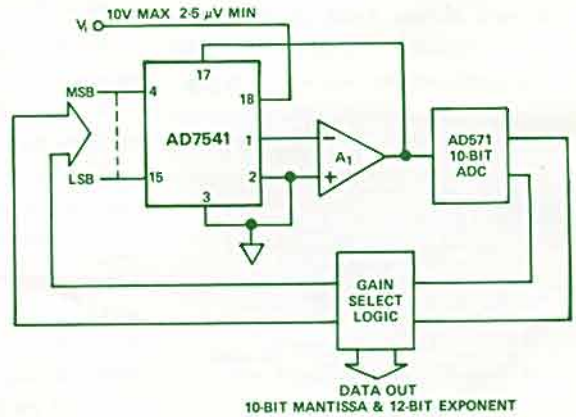

Figure 3. Ranging A-D converter.

FILTERS

It is well-known that analog multipliers can be used to program the gain of filters in response to analog voltage.[2] If the multiplier (which serves as a voltage-controlled attenuator) is replaced by a multiplying DAC (which serves as a digitally controlled attenuator), the cutoff frequency is under digital control. Figure 4 shows a first-order filter with cutoff frequency proportional to the digital number (D); both high-pass and low-pass responses are available. If $R_1 = R_2 = R_3 = R_4 = R$

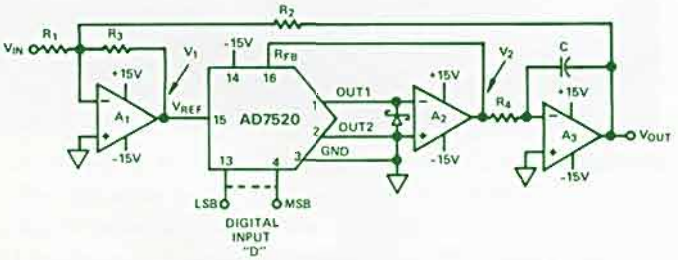

Figure 4. Digitally programmable low-pass filter.

$$V_{OUT} = \frac{D}{RC}\int V_1\,dt \equiv \frac{D}{RCp}\,V_1 \qquad (3)$$

and

$$V_1 = -(V_{IN} + V_{OUT}) \qquad (4)$$

hence,

$$V_{OUT} = -\frac{D}{RCp}V_{IN} - \frac{D}{RCp}V_{OUT} \qquad (5)$$

therefore,

$$V_{OUT} = -\frac{V_{IN}}{1 + \frac{RCp}{D}} \qquad \text{(low pass)} \qquad (6)$$

and

$$V_1 = -\frac{\frac{RCp}{D}}{1 + \frac{RCp}{D}} \qquad \text{(high pass)} \qquad (7)$$

The cutoff frequency, $f_c = \frac{D}{2\pi RC}$, is proportional to the digital input. In this example, a simplified case was chosen, in which all the external resistors are equal. In practice, however, insertion gain (or loss) may be necessary, or resistor-switched frequency ranging might be desirable. For the more-general case, the low-pass filter gain is R_2/R_1, and the cutoff frequency is

$$f_c = \frac{D\frac{R_3}{R_2}}{2\pi R_4 C} \qquad (8)$$

Note that, except for the normal minor gain trim, the DAC network resistance is not involved in the filter time constant, since the converter is connected as an attenuator, with the feedback resistance tracking the network resistance. It is possible to show a simpler-looking configuration, which saves one operational amplifier (Figure 5). However, the cost is a wide-range trim, to compensate for variation in the initial ladder resistance, and poor temperature tracking, unless the capacitor's tempco is equal and of opposite polarity to the network tempco.

[2] NONLINEAR CIRCUITS HANDBOOK, D. H. Sheingold, Ed., pp. 138-141, Analog Devices, Inc., P.O. Box 796, Norwood MA 02062, $5.95.

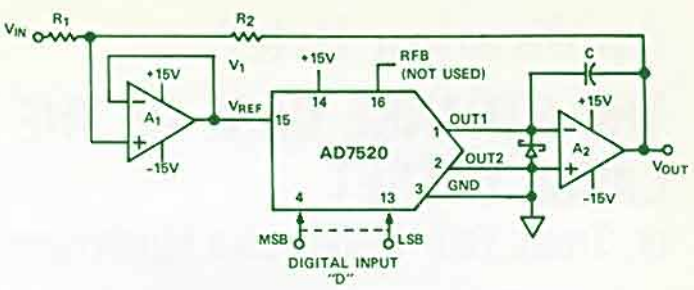

Figure 5. Programmable low-pass filter, simpler circuit.

PROGRAMMABLE TIME-DOMAIN FILTERING

It is sometimes useful to have a filter with an indicial (unit-pulse) response that can be arbitrarily adjusted in the time domain. This can be done digitally, but the cost may be excessive if the analog signals to be processed are at high frequency, and especially if the output is desired in analog form.

Figure 6 shows a way of accomplishing such filtering. A tapped analog bucket-brigade delay line (charge-coupled device) delays the signal by a length of time proportional to the clock period. The outputs of the taps are delayed versions of the input signal. If the input signal is a pulse of unit amplitude, it will be propagated from one tap to the next with a delay depending on the clock frequency and the number of elements in each segment of the line.

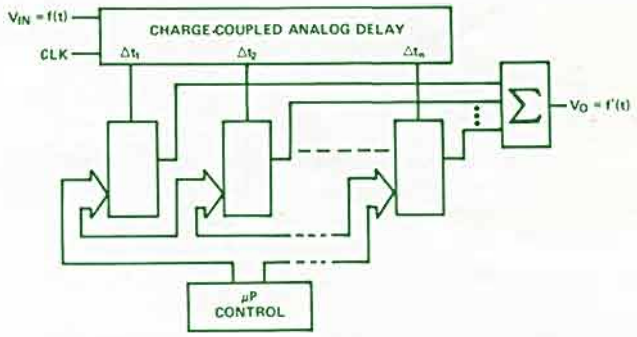

Figure 6. Programmable digital filter.

Each output is unloaded by a follower, if necessary, and applied to the analog input of a multiplying DAC. The digital input adjusts the gain of that individual tap, and the outputs of the DAC circuits are summed to provide the total response of the filter. If the input is a unit pulse, the response will simply be the responses of the taps, in order. For any other input waveform, the response of the filter will be appropriately related to the indicial response (since the system is linear), as long as the clock rate is substantially greater than twice the highest frequency present.

With this system, the filter characteristics can be changed by software, but the bandwidth for filtering can be several hundred kHz, and the process can be implemented with a low-cost microprocessor.[3]

[3] In fact, such a circuit has been successfully implemented, with a SC/MP microprocessor and AD7530's, by Con Cremin, of Telectron, Dublin, Ireland.