Analog filter can be programed digitally

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The frequency response of an analog active filter can be selected digitally, yet with the resolution and accuracy of resistive tuning and the dc stability of capacitive tuning. The filter accepts TTL inputs, permitting it to be controlled directly by a computer and making it ideal for electronically switched systems. Furthermore, this digitally programable filter is cost-competitive with mechanically switched types of filters, especially for high-order filter functions.

A simple first-order low-pass filter is drawn in (a). The corner frequency of this circuit is determined by the proportion (α) of the amplifier output voltage (V) that is applied to the feedback capacitor (C). Since applying a voltage of magnitude αV to capacitor C produces the same feedback current as applying a voltage of magnitude V to capacitor αC, the value of capacitor C is effectively multiplied by α. Therefore, the filter's corner frequency can be written as:

$$\omega_b = 1/\alpha R_f C$$

where R_f is the feedback resistor. The over-all dc gain of the circuit is unaffected by loop gain α.

The effective multiplication of capacitance C by gain α can be used to control the filter's corner frequency, as shown in (b). In this circuit, the filter's corner frequency is determined by logic inputs through a voltage-divider setup. Resistor R_a is the upper leg of the divider, while the resistance of the lower leg is selected by enabling the appropriate TTL inverter buffer. When a logic input turns on one of the buffers, the resistor associated with that buffer is shorted to ground.

Resistor R_b provides the appropriate bias voltage for the buffers. The transistor, which is wired as an emitter-follower, reduces the resistance of the voltage divider that is reflected forward in series with capacitor C. This Thevinin equivalent resistance (R_T) is divided by the current gain (β) of the emitter-follower. For the circuit to operate properly:

$$R_T/\beta \text{ must be much less than } R_i \parallel R_f$$

where R_i is the input resistor. Since the dc levels of both the buffers and the transistor are blocked by the capacitor, there is no need for any bias stabilization circuitry.

If the effects of biasing resistor R_c are neglected, programable gain α can be expressed as:

$$\alpha = 1/[1 + (R_a/R_b) + \Sigma R_a G_i]$$

where G_i represents the conductance of those resistors, R_1 through R_n, whose buffers are enabled. The filter's corner frequency now becomes:

$$\omega_b = \omega_0(K + \Sigma R_a G_i)$$

where:

$$\omega_0 = 1/R_f C$$
$$K = 1 + (R_a/R_b)$$

The filter's starting frequency—that is, the corner frequency of the filter with none of the logic buffers enabled—is equal to $K\omega_0$. And each increment above this frequency, as each logic buffer is enabled, is equal to $\omega_0 R_a G_i$. Since the effects of the enabled buffers are additive, the filter can be programed to accept either standard binary codes or a binary-coded-decimal input. For the component values cited in the figure, ω_0 is 100 radians/second, K is 2, the starting frequency is 200 rad/s, and the frequency increment is 250 rad/s.

Moreover, the programing approach that is shown here can be extended to higher-order filters through the use of either the standard biquad or state-variable filter configurations.[1,2] $\square$

REFERENCES
1. A.E. Schultz, "Active Filters Are Moving toward Standardization," Electronic Products, June 18, 1973.
2. G.E. Tobey, J.G. Graeme, L.P. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill Inc., 1971.
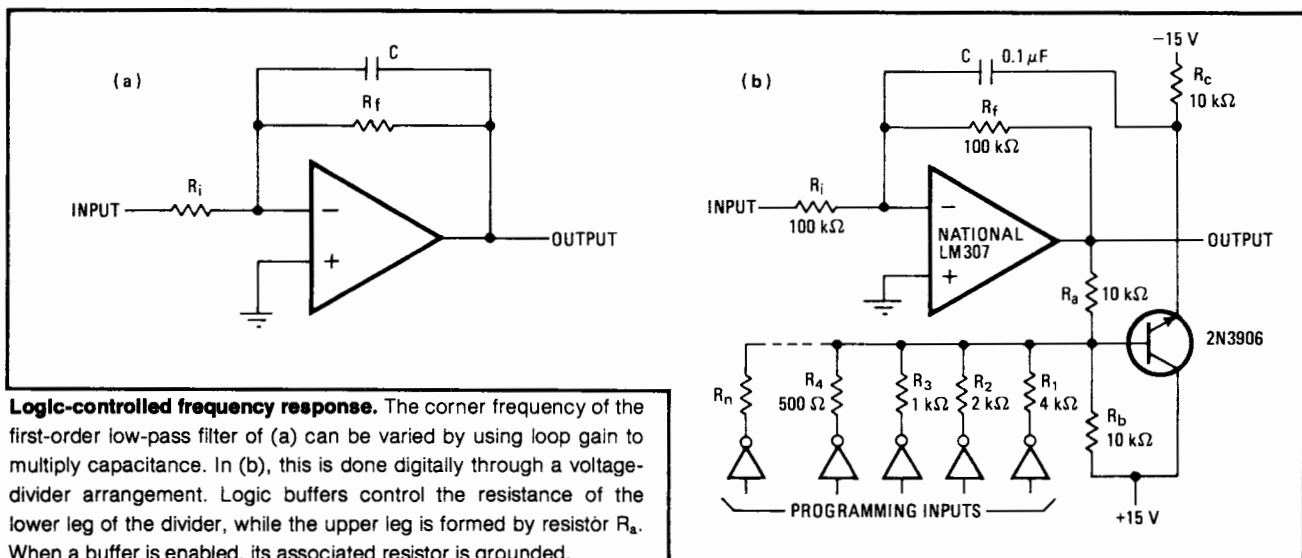
Logic-controlled frequency response. The corner frequency of the first-order low-pass filter of (a) can be varied by using loop gain to multiply capacitance. In (b), this is done digitally through a voltage-divider arrangement. Logic buffers control the resistance of the lower leg of the divider, while the upper leg is formed by resistor R_a. When a buffer is enabled, its associated resistor is grounded.