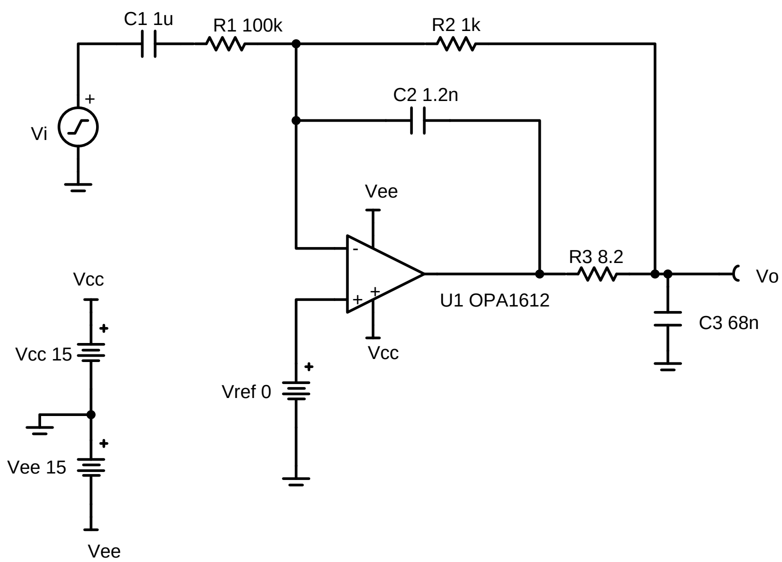
Band pass filtered inverting attenuator circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
$100mV_{pp}$	$50V_{pp}$	$1mV_{pp}$	$500mV_{pp}$	15V	–15V	0V

Design Description

This tunable band-pass attenuator reduces signal level by –40dB over the frequency range from 10Hz to 100kHz. It also allows for independent control of the DC output level. For this design, the pole frequencies were selected outside the pass band to minimize attenuation within the specified bandwidth range.



Design Notes

1. If a DC voltage is applied to V_{ref} be sure to check common mode limitations.
2. Keep R_3 as small as possible to avoid loading issues while maintaining stability.
3. Keep the frequency of the second pole in the low-pass filter (f_{p3}) at least twice the frequency of the first low-pass filter pole (f_{p2}).

Design Steps

1. Set the passband gain.

   $\text{Gain} = -\frac{R_2}{R_1} = -0.01\frac{V}{V}\,(-40\text{dB})$

   $R_1 = 100\text{k}\Omega$

   $R_2 = 0.01 \times R_1 = 1\ \text{k}\Omega$

2. Set high-pass filter pole frequency (f_{p1}) below f_l.

   $f_l = 10\text{Hz},\ f_{p1} = 2.5\ \text{Hz}$

3. Set low-pass filter pole frequency (f_{p2} and f_{p3}) above f_h.

   $f_h = 100\text{kHz}$

   $f_{p2} = 150\text{kHz}$

   $f_{p3} \geq 2 \times f_{p2} = 300\text{kHz}$

   $f_{p3} = 300\text{kHz}$

4. Calculate C_1 to set the location of f_{p1}.

   $C_1 = \frac{1}{2\pi \times R_1 \times f_{p1}} = \frac{1}{2\pi \times 100\text{k}\Omega \times 2.5\text{Hz}} = 0.636\ \mu\text{F} \approx 1\ \ \mu\text{F}$ (Standard Value)

5. Select components to set f_{p2} and f_{p3}.

   $R_3 = 8.2\Omega$ (provides stability for cap loads up to 100nF)

   $C_2 = \frac{1}{2\pi \times (R_2 + R_3) \times f_{p2}} = \frac{1}{2\pi \times 1008.2\Omega \times 150\text{kHz}}$

   $= 1052\text{pF} \approx 1200\text{pF}$ (Standard Value)

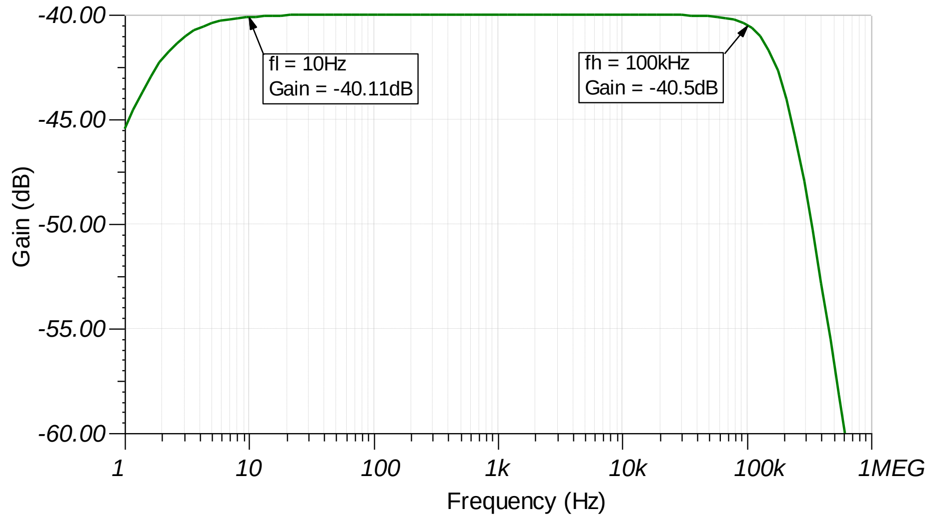
   $C_3 = \frac{1}{2\pi \times R_3 \times f_{p3}} = \frac{1}{2\pi \times 8.2\Omega \times 300\text{kHz}} = 64.7\ \text{nF} \approx 68\text{nF}$ (Standard Value)

Design Simulations

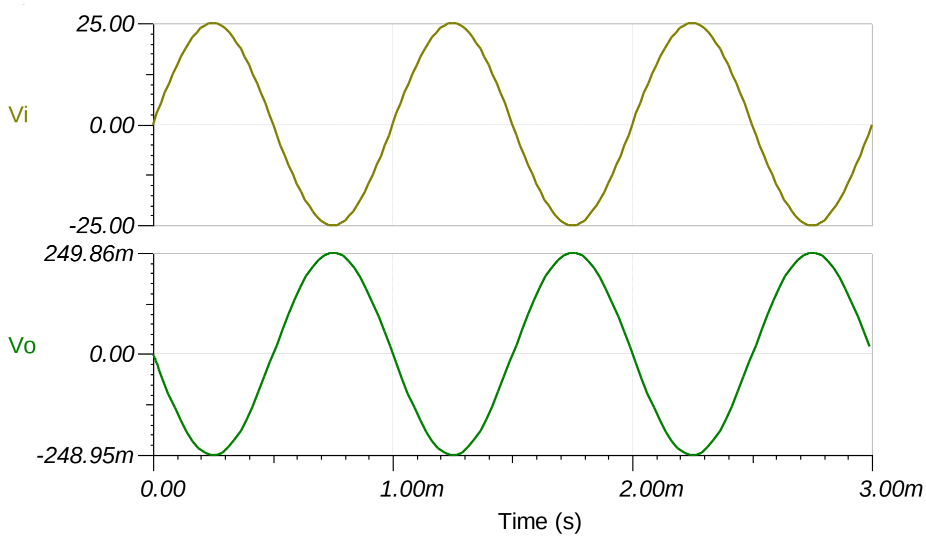
DC Simulation Results

The amplifier will pass DC voltages applied to the noninverting pin up to the common mode limitations of the op amp (±13V in this design)

AC Simulation Results



Transient Simulation Results



Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC503.

See TIPD118, www.ti.com/tool/tipd118.

Design Featured Op Amp

OPA1612	
V_{ss}	4.5V to 36V
V_{inCM}	V_{ee}+2V to V_{cc}–2V
V_{out}	V_{ee}+0.2V to V_{cc}–0.2V
V_{os}	100µV
I_q	3.6mA/Ch
I_b	60nA
UGBW	40MHz
SR	27V/µs
#Channels	1, 2
www.ti.com/product/opa1612	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5V to 36V
V_{inCM}	V_{ee}–100mV to V_{cc}–2V
V_{out}	Rail-to-rail
V_{os}	200µV
I_q	1.6mA/Ch
I_b	8pA
UGBW	10MHz
SR	10V/µs
#Channels	1, 2, 4
www.ti.com/product/opa172	

Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.