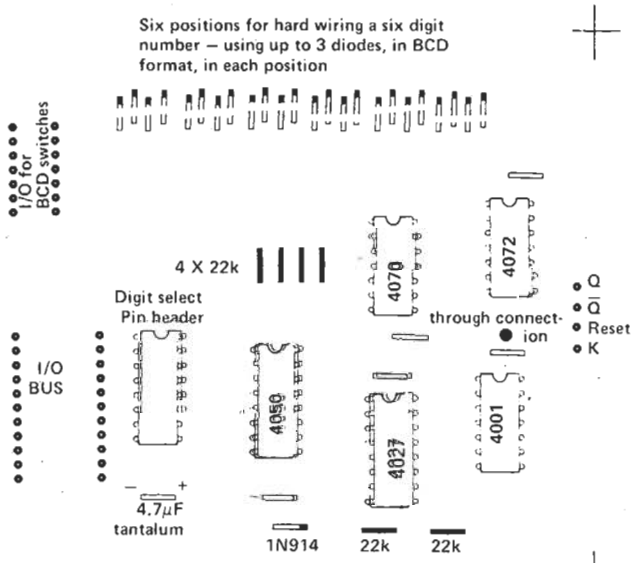
ETI TIMING MODULES:

COMPARATOR MODULE

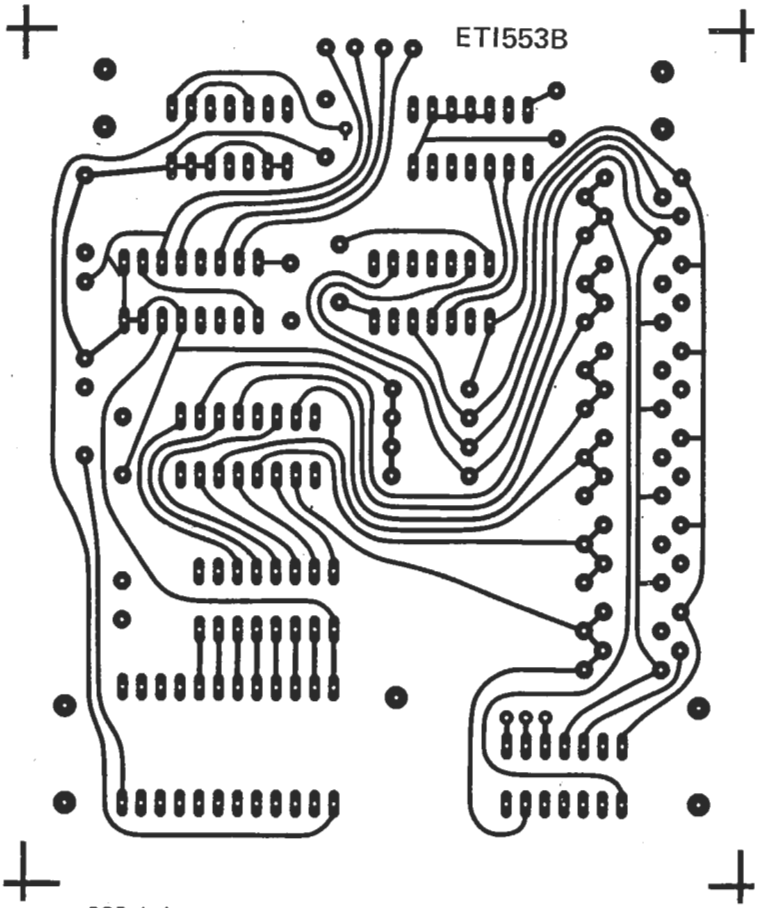
The comparator module can be used to compare a 9-digit number with the clock module data, but as drawn here we have only catered for 6 digits. The digits required are selected and buffered as in the display driving circuitry of the clock and latch modules. The outputs of the 4050 buffers are then fed via BCD switches (or hard-wired connections) and diodes to four dual input Exclusive-OR gates (1 x 4070 (1)). The other inputs are taken from the clock module inputs. The outputs of the latter are taken to a four input OR gate to form a 'difference" circuit such that at any time that the ABCD line inputs differ from the clock module SR ABCD inputs, the output of the four input OR gate will go high. This output is gated by C1, which is high during the second half



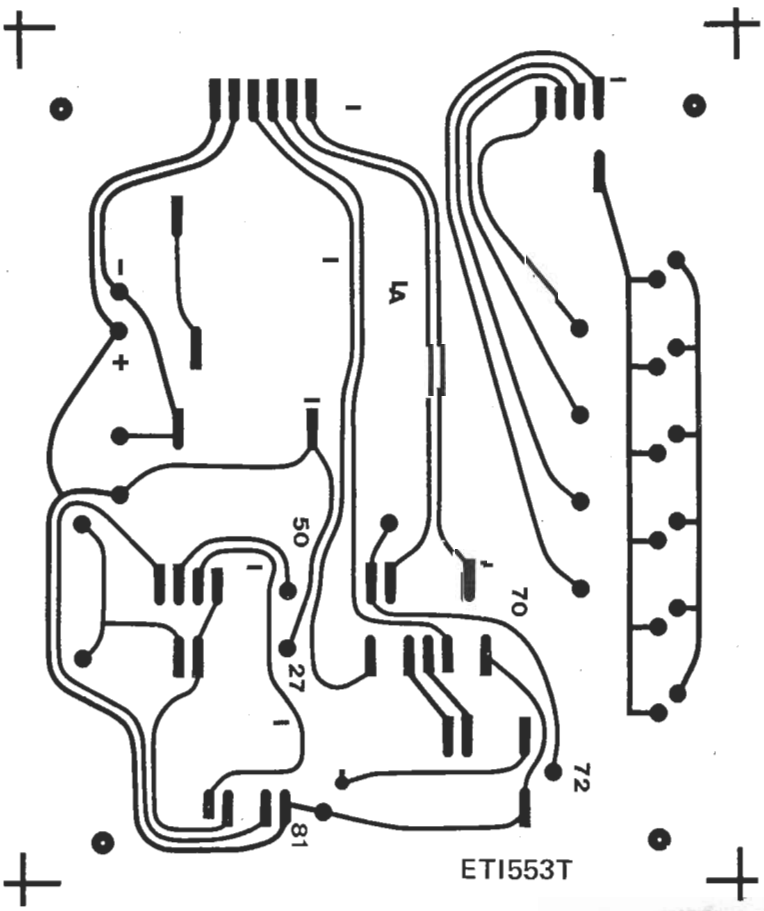
KEY

Resistors — Capacitors, all unmarked = 10nF — Diodes — Through connections from top to bottom of board.

Component layout.



PCB designs.



ETI TIMING MODULES:

COMPARATOR MODULE

of any Q time, to exclude 'difference' outputs which are due to switching times, etc.

The Q output of a J-K Flip-Flop (4027 (A)) is set to '1' half-way through Q0 time by Q0 and C1'. During one word (Q0 time to Q9 time) it will be reset if there are any differences between the numbers set by the BCD switches and the contents of the clock module (SR). If, however, a whole word passes with no differences between the two sets of data, Q will still be set halfway through the following Q0 time, and Q of Flip-Flop (B), the comparator alarm output, will be clocked high. This alarm output is cleared when power is first applied, and may be cleared or disabled by closing the 'clear' switch.

If the jumper connection J1 is made (indicated by a dotted line), when the alarm output goes high it will stay high until the middle of the next Q0 time, i.e. it will be high for one word time. If this output is connected to the clock module reset connection it will reset the clock module to zero, and leave it counting. This can be used to provide a programmed pulse generator with a range of milliseconds to hundreds of hours. Any number of digits between 1 and 9 can be used to 'set' the comparison time. Unspecified digits will be treated by the comparator as being zero's. As mentioned earlier, any number of comparator modules may be connected to one clock module.

Any enquiries about the three timing modules can be answered by Sintel, of 53a Aston Street, Oxford. Sintel can supply pcbs and components for these projects.

A final note about the clock module described last month. The 4020 first-stage divider should be selected for operation at 5.12MHz. All the Fairchild devices are suitable. ●

PARTS LISTS

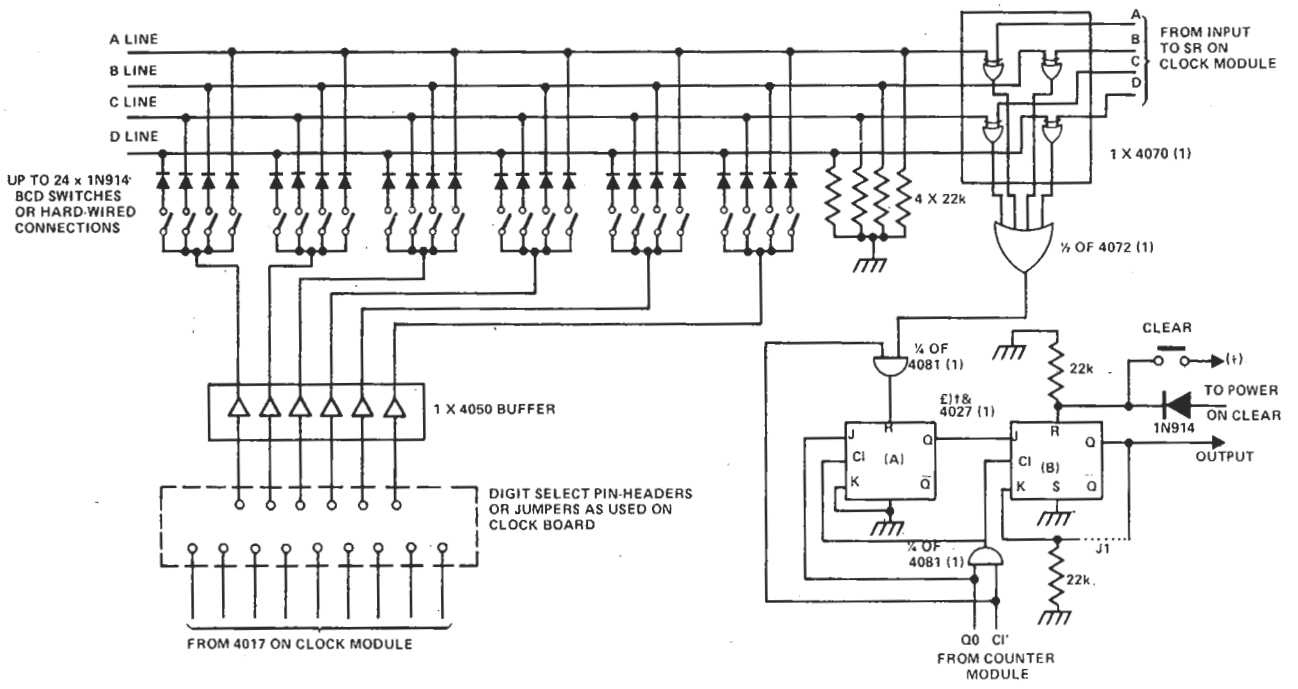
CMOS–
4001
4027
4050
4070
4072

RESISTORS–
Six 22k ¼W

CAPACITORS–
Five 10nF ceramic
one 4.7μF, tantalum

DIODES–
up to 25 x 1N914

ALSO: pcb ETI553, three 14 pin DIL sockets, two 16 pin DIL sockets, DIL 16 pin header, optional 22 pin LSI socket and plug, 20-way cable (6" or so), optional I/O plug, socket and cable for BCD switches.



Circuit diagram of the Comparator Module.