

Reset circuit reacts to fast line hits

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This circuit generates a start-up signal on power-up or a reset pulse of specified width whenever the supply voltage to any device momentarily drops below a preset value. It is therefore ideal for use in initializing microprocessor-based systems. Much faster and more reliable than most RC-type reset circuits, it will respond to power glitches of microsecond duration.

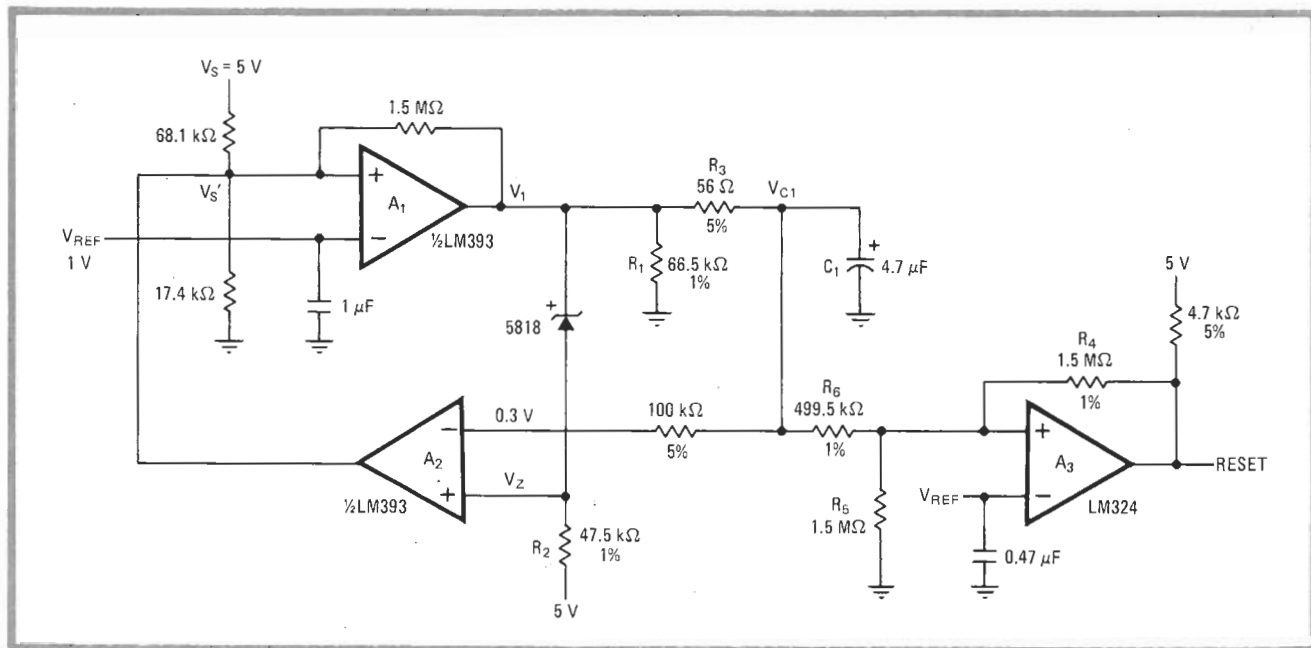
As shown, open-collector operational amplifier A_1 , working as a Schmitt trigger, compares the preset trip voltage, V_{ref} , to a preset fraction of the supply voltage, V_s . On power-up, voltage V_s' will come up before voltage V_{ref} , and A_1 will fire to enable capacitor C_1 to charge to $V_1 = [V_s' - 0.3] [R_1 / (R_1 + R_2)]$, with resistor R_1

selected to keep A_2 in its linear operating range and resistor R_3 chosen to limit the peak output current of A_1 . A_3 turns on when V_{C1} exceeds its threshold voltage, which is $V_{ref}R_5(1/R_5 + 1/R_6 + 1/R_4)$.

During a power glitch, V_s' will drop below V_{ref} , causing A_1 to go low and bringing the noninverting input of A_2 to about 0.3 volt. Open-collector comparator A_2 then goes low, in effect latching (clamping) A_1 until C_1 discharges through R_2 , whereupon the reset output at A_3 goes (active) low for a time equal to R_2C_1 .

At this time, V_{C1} drops below V_Z , and A_2 once again becomes transparent to circuit operation, thus enabling the V_s' -to- V_{ref} comparison. A_1 will then allow C_1 to recharge and bring the reset output high until the next power glitch, whereupon a reset pulse is again generated. Note that if on power-up there is any voltage on C_1 , the circuit will latch until the capacitor is completely discharged and then will allow it to charge through R_2 for the full reset time. □

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Fail-safe. Power-reset circuit provides full initialization of microprocessor-based systems for glitches lasting only microseconds. Circuit generates start-up signal on power up, then goes low for a time given by $T = R_2C_1$ when V_s' drops below user-set reference V_{ref} .